UNITED STATES SECURITIES AND EXCHANGE COMMISSION

WASHINGTON, D.C. 20549

FORM 8-K

CURRENT REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934

Date of report (Date of earliest event reported): November 4, 2013 (October 29, 2013)

FREESCALE SEMICONDUCTOR, LTD.

(Exact Name of Registrant as Specified in Charter)

Bermuda (State or Other Jurisdiction of Incorporation) 001-35184 (Commission File Number) 98-0522138 (IRS Employer Identification Number)

6501 William Cannon Drive West, Austin, Texas 78735 (Address of Principal Executive Offices, including Zip Code)

(512) 895-2000 (Registrant's telephone number, including area code)

(Former Name or Former Address, if Changed Since Last Report)

| Check the appropriate box below if the Form 8-K filing is intended to simultaneously satisfy the filing obligation of the registrant under any of the following provisions: | | |
|---|--|--|
| | Written communications pursuant to Rule 425 under the Securities Act (17 CFR 230.425) | |
| | Soliciting material pursuant to Rule 14a-12 under the Exchange Act (17 CFR 240.14a-12) | |
| | Pre-commencement communications pursuant to Rule 14d-2(b) under the Exchange Act (17 CFR 240.14d-2(b)) | |
| | Pre-commencement communications pursuant to Rule 13e-4(c) under the Exchange Act (17 CFR 240.13e-4(c)) | |
| | | |

Item 1.01 Entry into a Material Definitive Agreement.

6.000% Senior Secured Notes Due 2022

On November 1, 2013, Freescale Semiconductor, Inc. ("Freescale"), a wholly owned indirect subsidiary of Freescale Semiconductor, Ltd. (the "Company"), issued \$960 million aggregate principal amount of 6.000% Senior Secured Notes due 2022 at an issue price of 100% of the principal amount of the notes (the "Notes"), in a private placement to "qualified institutional buyers" in the United States defined in Rule 144A under the Securities Act of 1933, as amended (the "Securities Act"), and outside of the United States pursuant to Regulation S under the Securities Act. The Notes mature on January 15, 2022, and bear interest at a rate of 6.000% per annum, payable on May 15 and November 15 of each year, commencing on May 15, 2014, and at maturity.

The net proceeds of the offering, along with cash on hand, will be used to redeem \$884 million principal amount of Freescale's outstanding 9 $\frac{1}{4}$ % Senior Secured Notes due 2018 (the "9 $\frac{1}{4}$ % Notes"), representing all outstanding 9 $\frac{1}{4}$ % Notes, in accordance with the indenture governing those notes, and to pay the related premium and fees.

Indenture

The Notes were issued pursuant to an indenture, dated as of November 1, 2013 (the "Indenture"), among Freescale, certain direct and indirect parent companies and certain subsidiaries of Freescale (the "Guarantors") and Wells Fargo Bank, National Association, as trustee.

Freescale may redeem the Notes, in whole or in part, at any time prior to November 15, 2016, at a redemption price equal to 100% of the principal amount of the Notes, plus accrued and unpaid interest to the redemption date, plus the applicable "make-whole" premium, as described in the Indenture. Freescale may redeem the Notes, in whole or in part, at any time on or after November 15, 2016, at a redemption price equal to 100% of the principal amount of the Notes, plus accrued and unpaid interest to the redemption date, plus a premium declining over time as set forth in the Indenture. In addition, at any time on or prior to November 15, 2016, Freescale may redeem up to 35% of the aggregate principal amount of the Notes with the proceeds of certain equity offerings, as described in the Indenture. If Freescale experiences certain change of control events, Note holders may require it to repurchase all or part of their Notes at 101% of the principal amount of the Notes, plus accrued and unpaid interest to the repurchase date.

The Indenture contains covenants that, among other things, restrict the ability of Freescale, certain parent guarantors and restricted subsidiaries to, among other things, incur or guarantee additional indebtedness or issue preferred stock; pay dividends and make other restricted payments; incur restrictions on the payment of dividends or other distributions from restricted subsidiaries; create or incur certain liens; make certain investments; transfer or sell assets; engage in transactions with affiliates; and merge or consolidate with other companies or transfer all or substantially all of its assets. These covenants are subject to a number of other limitations and exceptions set forth in the Indenture.

The Indenture also provides for customary events of default, including failure to pay any principal or interest when due, failure to comply with covenants and cross acceleration provisions. In the case of an event of default arising from specified events of bankruptcy or insolvency, all outstanding Notes will become due and payable immediately without further action or notice. If any other event of default under the Indenture occurs or is continuing, the trustee or holders of at least 30% in aggregate principal amount of the then outstanding Notes may declare all of the Notes to be due and payable immediately.

The description of the Notes and the Indenture contained in this Current Report on Form 8-K is qualified in its entirety by reference to the complete text of the Indenture, a copy of which is filed herewith as Exhibit 4.1 which is incorporated herein by reference.

Security Agreements

The Notes are secured by a security agreement, dated November 1, 2013, by and among Freescale, the Guarantors party thereto and Citibank, N.A., in its capacity as collateral agent for the holders of the Notes (the "Security Agreement"). The Notes are also secured by an intellectual property security agreement, dated November 1, 2013, by and among Freescale, the Guarantors party thereto and Citibank, N.A., in its capacity as collateral agent for the holders of the Notes (the "IP Security Agreement").

The description of the Security Agreement and the IP Security Agreement contained in this Current Report on Form 8-K is qualified in its entirety by reference to the complete text of such agreements, copies of which are filed herewith as Exhibits 10.1 and 10.2, respectively each of which is incorporated herein by reference.

Item 2.03 Creation of a Direct Financial Obligation or an Obligation under an Off-Balance Sheet Arrangement of a Registrant.

The information set forth under Item 1.01 above is incorporated by reference into this Item 2.03.

Item 5.02 Departure of Directors or Certain Officers; Election of Directors; Appointment of Certain Officers; Compensatory Arrangements of Certain Officers

(d) On October 29, 2013, the Company's Board of Directors (the "Board") appointed Joanne M. Maguire to fill a vacancy on the Board and the Company's Audit and Legal Committee effective as of November 4, 2013.

The Board has determined that Ms. Maguire is an "independent director" in accordance with the New York Stock Exchange listing standards, Securities and Exchange Commission rules and the Company's Corporate Governance Guidelines. As an independent director, Ms. Maguire will receive (i) a grant of restricted share units with a value equal to \$175,000 under the Freescale Semiconductor Holdings 2011 Omnibus Incentive Plan upon her appointment to the Board and annually each year thereafter, which vests fully on the first anniversary of the date of grant, and (ii) an annual cash retainer of \$60,000 to be paid in advance in equal installments at the beginning of each quarter. Ms. Maguire will also be reimbursed for expenses related to her service on the Board.

Ms. Maguire has no relationships or transactions with the Company which are required to be disclosed pursuant to Item 404(a) of Regulation S-K.

(e) On October 29, 2013, the Compensation and Leadership Committee of the Company adopted the forms of Performance Restricted Share Unit Award Agreement (Senior Management) (the "PRSU Award Agreement"), Nonqualified Stock Option Agreement (Senior Management) (the "NQSO Award Agreement") and Restricted Share Unit Award Agreement (Senior Management) (the "RSU Award Agreement" and collectively, the "Award Agreements") to be used for grants under the Freescale Semiconductor Holdings 2011 Omnibus Incentive Plan to certain senior executives of the Company. The following description of the Award Agreements is qualified in its entirety by reference to the Award Agreements, copies of which are filed as Exhibits 10.3, 10.4 and 10.5 and are incorporated by reference.

The PRSU Award Agreement provides for an award of a target number of restricted share units based on the Company's achievement of specified performance goals based on total shareholder return over a three year period relative to a peer group. Common shares are delivered to the participant only if the performance goals have been achieved and certified by the Compensation and Leadership Committee, and the participant has become vested in the restricted share units. To the extent the applicable performance goals have been achieved, participants will be entitled to receive from 0 to 1.5 (the "share delivery factor") common shares for each restricted share unit under the PRSU Award Agreement. As soon as practicable following the last day of the performance period but no later than January 31 in the year following the end of the three year performance period, the Compensation and Leadership Committee will certify the extent to which the performance goals have been achieved and the corresponding share delivery factor. Subject to the participant's continued employment, or except as otherwise provided in the PRSU Award Agreement, the restricted share units delivered under the PRSU Award Agreement, if any, will vest on the date the Compensation and Leadership Committee certifies that the performance goals have been achieved. Under the terms of the PRSU Award Agreement, upon termination due to death or disability after the first anniversary of

the date of grant, the award will become vested for a prorated portion of restricted share units based on the number of days elapsed from the grant date with a deemed share delivery factor of 1.0. In the event of a change in control, the performance period will terminate on the date of the change in control and the actual total shareholder return for the performance period will be used to calculate the share delivery factor for the award.

The NQSO Award Agreement and RSU Award Agreement generally provide for vesting of 25% of the applicable award on each of the first, second, third and fourth anniversaries of the date of grant, subject to the participant's continued employment. Upon termination of employment due to death or disability, awards under the NQSO Award Agreement and RSU Award Agreement will become vested for an additional number of shares equal to the number of shares that would have vested on the next anniversary of the date of grant if the participant had remained employed until such date. Vested options under the NQSO Award Agreement are exercisable at any time before the earliest to occur of: (i) the seventh anniversary of the date of grant, (ii) twelve months following the date of termination of employment due to retirement, death or disability, (iii) ninety days following termination of employment for any reason other than cause or due to retirement, death or disability or (iv) immediately upon notification of termination of employment for cause. Under the RSU Award Agreement, participants will receive one common share of the Company for each vested restricted share unit as soon as practicable following the applicable vesting date.

Each of the Award Agreements provides that in the event the participant's employment is terminated by the Company without cause or by the participant for good reason, in each case within twelve months of a change in control, all unvested awards will become immediately vested. For purposes of the Award Agreements, the definition of "good reason" is the definition contained in the participant's employment agreement, or absent an employment agreement, the definition contained in the Award Agreements are not assumed or substituted under the terms of the Award Agreements in connection with a change in control, all unvested portions of the awards will become vested immediately upon the occurrence of the change in control.

The Award Agreements also contain covenants regarding confidential information, non-solicitation and non-competition that are effective following termination. In the case of the RSU and PRSU Award Agreements, if a participant breaches any of these covenants during the two year period following the date of termination, the participant will be required to immediately repay the Company the fair market value of shares acquired pursuant to the award on any vesting date within a three year period prior to termination. In the case of the Option Award Agreement, if a participant breaches any of these covenants during the two year period following the date of termination, any vested portion of the award will be forfeited and the participant will be required to immediately repay the Company any gain (defined as the difference between the exercise price and the fair market value on the date of exercise) resulting from the exercise of an option within the three year period prior to termination or after termination.

Item 8.01 Other Events.

On November 1, 2013, in connection with the closing of the previously announced offering of the Notes, Freescale delivered to the holders of its 9 $\frac{1}{4}$ % Notes notice that it will redeem \$884 million principal amount of the 9 $\frac{1}{4}$ % Notes, representing all outstanding 9 $\frac{1}{4}$ % Notes. The redemption date is December 2, 2013 (the "Redemption Date"). The redemption price for the 9 $\frac{1}{4}$ % Notes is 100% of the outstanding aggregate principal amount of the 9 $\frac{1}{4}$ % Notes being redeemed, plus the Applicable Premium (as defined in the Indenture dated April 13, 2010 governing the 9 $\frac{1}{4}$ % Notes) as of, and accrued and unpaid interest up to, but not including, the Redemption Date. The Notes shall be redeemed in accordance with the procedures of The Depository Trust Company. Because all the outstanding 9 $\frac{1}{4}$ % Notes are to be redeemed, the entire outstanding amount of 9 $\frac{1}{4}$ % Notes held by each Holder, even if not a multiple of \$1,000, shall be redeemed.

Additionally, on October 29, 2013, the Board, upon the recommendation of the Compensation and Leadership Committee, adopted share ownership guidelines to cover independent members of the Board. The guidelines provide that the independent members of the Board must retain 100% of their vested shares until they accumulate a minimum share ownership of a number of shares equal to the quotient of (1) an amount equal to five times the annual cash retainer for service on the Board (excluding retainers for chair service, except for the additional compensation given to the Chairman of the Board), divided by (2) the average of the closing prices on the last trading day of each month in the prior year.

Cautionary Note Regarding Forward-Looking Statements

This Periodic Report on Form 8-K includes forward-looking statements within the meaning of the Private Securities Litigation Reform Act of 1995. These statements relate to the redemption of senior secured notes by Freescale and other statements that are not historical fact. Although we believe the assumptions upon which these forward-looking statements are based are reasonable, any of these assumptions could prove to be inaccurate and the forward-looking statements based on these assumptions could be incorrect. Actual results and trends in the future may differ materially from those suggested or implied by the forward-looking statements depending on a variety of factors. Some of these factors include market conditions and such other risk factors as may be discussed in Freescale Semiconductor, Ltd.'s filings with the Securities and Exchange Commission. We undertake no obligation to update any information contained in this Periodic Report on Form 8-K.

Item 9.01 Financial Statements and Exhibits.

(d) Exhibits.

| Exhibit No. | <u>Description</u> |
|----------------|--|
| 4.1 | Indenture, dated as of November 1, 2013, by and among Freescale, the Guarantors named therein and Wells Fargo Bank, National Association, as Trustee, governing the Notes. |
| 4.2 | Form of 6.000% Senior Secured Note (included as Exhibit A to Exhibit 4.1). |
| 10.1 | Security Agreement, dated November 1, 2013, by and among Freescale, the Guarantors party thereto and Citibank, N.A., in its capacity as collateral agent for the holders of the Notes. |
| 10.2 | Intellectual Property Security Agreement, dated November 1, 2013, by and among Freescale, the Guarantors party thereto and Citibank, N.A., in its capacity as collateral agent for the holders of the Notes. |
| 10.3 | Freescale Semiconductor Holdings 2011 Omnibus Incentive Plan Form Performance Restricted Share Unit Award Agreement (Senior Management). |
| 10.4 | Freescale Semiconductor Holdings 2011 Omnibus Incentive Plan Form Nonqualified Stock Option Agreement (Senior Management). |
| 10.5 | Freescale Semiconductor Holdings 2011 Omnibus Incentive Plan Form Restricted Share Unit Award Agreement (Senior Management). |

SIGNATURES

Pursuant to the requirements of the Securities Exchange Act of 1934, the registrant has duly caused this report to be signed on its behalf by the undersigned hereunto duly authorized.

FREESCALE SEMICONDUCTOR, LTD.

/s/ Dathan C. Voelter By: Name: Dathan C. Voelter

Title: Assistant Secretary

Date: November 4, 2013

Exhibit Index

| Exhibit Number | Description |
|----------------|---|
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| 10.4 | Freescale Semiconductor Holdings 2011 Omnibus Incentive Plan Form Nonqualified Stock Option Agreement (Section 16 Officer) |
| 10.5 | Freescale Semiconductor Holdings 2011 Omnibus Incentive Plan Form Restricted Share Unit Award Agreement (Section 16 Officer) |

INDENTURE

Dated as of November 1, 2013

Among

FREESCALE SEMICONDUCTOR, INC.,

the Guarantors listed herein

and

WELLS FARGO BANK, NATIONAL ASSOCIATION, as Trustee

6.000% SENIOR SECURED NOTES DUE 2022

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EXHIBITS

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| | |

INDENTURE, dated as of November 1, 2013, among Freescale Semiconductor, Inc., a Delaware corporation, and the Guarantors (as defined herein) listed on the signature pages hereto and Wells Fargo Bank, National Association, as Trustee.

WITNESSETH

WHEREAS, the Issuer (as defined herein) has duly authorized the creation of an issue of \$960,000,000 aggregate principal amount of the Issuer's 6.000% senior secured notes due 2022 (the "Initial Notes");

WHEREAS, the Issuer and each of the Guarantors has duly authorized the execution and delivery of this Indenture.

NOW, THEREFORE, the Issuer, the Guarantors and the Trustee agree as follows for the benefit of each other and for the equal and ratable benefit of the Holders of the Notes.

ARTICLE I

DEFINITIONS

SECTION 1.01. Definitions.

"144A Global Note" means a Global Note substantially in the form of Exhibit A hereto bearing the Global Note Legend and the Private Placement Legend and deposited with or on behalf of, and registered in the name of, the Depositary or its nominee that will be issued in a denomination equal to the outstanding principal amount of the applicable series of Notes sold in reliance on Rule 144A.

"300 Millimeter R&D Expenses" means, with respect to any period, the amount of research and development expenses of Holdings III and its Restricted Subsidiaries for such period, on a consolidated basis, relating to any 300 millimeter or larger wafer fabrication alliance or arrangement of Holdings III or any of its Restricted Subsidiaries other than the strategic alliance relating to the manufacturing of 300 millimeter wafers in Crolles, France in existence on the Transaction Date (any such alliance or arrangement, a "300 Millimeter Arrangement"); provided, that the amount of such research and development expenses with respect to any such 300 Millimeter Arrangement constituting 300 Millimeter R&D Expenses for such period for purposes hereof shall not exceed the greater of (i) the amount of any negative EBITDA with respect to such 300 Millimeter Arrangement for such period and (ii) the amount of any Equalization Payments with respect to such 300 Millimeter Arrangement for such period.

"300 Millimeter Asset Sale" means any sale of any assets of Holdings III or any Restricted Subsidiary relating to the Issuer's alliance with respect to the 300 millimeter wafer fabrication in Crolles, France; provided that no asset sale shall constitute a 300 Millimeter Asset Sale to the extent that, after giving effect to such asset sale, the aggregate amount of 300 Millimeter Asset Sale Proceeds with respect to all 300 Millimeter Asset Sales shall exceed \$500 million.

"300 Millimeter Asset Sale Proceeds" means the aggregate cash proceeds received by Holdings III or any of its Restricted Subsidiaries in respect of any 300 Millimeter Asset Sale, including any cash received upon the sale or other disposition of any Designated Non-cash Consideration received in any 300 Millimeter Asset Sale, net of the direct costs relating to such 300 Millimeter Asset Sale and the sale or disposition of such Designated Non-cash Consideration, including legal, accounting and investment banking fees, and brokerage and sales commissions, any relocation expenses incurred as a result thereof, taxes paid or payable as a result thereof (after taking into account any available tax credits or deductions and any tax sharing arrangements), amounts required to be applied to the repayment of principal, premium, if any, and interest on Senior Indebtedness required to be paid as a result of such transaction and any deduction of appropriate amounts to be provided by Holdings III or any of its Restricted Subsidiaries after such sale or other disposition thereof, including pension and other post-employment benefit liabilities and liabilities related to environmental matters or against any indemnification obligations associated with such transaction.

- "Acquired Indebtedness" means, with respect to any specified Person,
- (1) Indebtedness of any other Person existing at the time such other Person is merged with or into or became a Restricted Subsidiary of such specified Person, including Indebtedness incurred in connection with, or in contemplation of, such other Person merging with or into or becoming a Restricted Subsidiary of such specified Person, and
 - (2) Indebtedness secured by a Lien encumbering any asset acquired by such specified Person.
 - "Acquisition" means the transactions contemplated by the Transaction Agreement.

"Additional First Lien Debt" means the Notes (including Guarantees of the Notes), the Existing Secured Notes (including Guarantees of the Existing Secured Notes) and any indebtedness of the Issuer (other than indebtedness constituting Senior Credit Facilities Obligations) secured by the Collateral on a <u>pari passu</u> basis (but without regard to control of remedies) with the Senior Credit Facilities Obligations; <u>provided</u>, <u>however</u>, that (i) such indebtedness is permitted to be incurred, secured and guaranteed on such basis by each First Lien Debt Document and (ii) the representative for the holders of such indebtedness is, in the case of the Collateral Agent, a party to the Intercreditor Agreement, or in the case of any Additional First Lien Debt entered into after the Issue Date, shall have become party to the Intercreditor Agreement.

- "Additional First Lien Debt Collateral Documents" means the Collateral Documents relating to the Notes and each other agreement, instrument or other document entered into in favor of the representative for any class of Secured Parties under any class of Additional First Lien Debt for the purposes of securing such Additional First Lien Debt Obligations.
- "Additional First Lien Debt Documents" means, with respect to any class of Additional First Lien Debt, the promissory notes, indentures, Additional First Lien Debt Collateral Documents or other operative agreements evidencing or governing such Additional First Lien Debt Obligations, as the same may be amended, restated, supplemented or otherwise modified from time to time.
- "Additional First Lien Debt Obligations" means, with respect to any class of Additional First Lien Debt, (a) all principal of and interest (including, without limitation, any interest which accrues after the commencement of any case, proceeding or other action relating to the bankruptcy, insolvency or reorganization of the Issuer, whether or not allowed or allowable as a claim in any such proceeding) payable with respect to such Additional First Lien Debt, (b) all other amounts payable to the related Additional First Lien Debt Parties under the related Additional First Lien Debt Documents and (c) any renewals, extensions or refinancings of the foregoing, provided that in the case of this clause (c), the representative in respect of such class has executed and delivered a joinder agreement in compliance with the Intercreditor Agreement.
- "Additional First Lien Debt Parties" means, with respect to any class of Additional First Lien Debt, the holders of such Indebtedness from time to time, any trustee or agent therefor under any related Additional First Lien Debt Documents, and the beneficiaries of each indemnification obligation undertaken by the Issuer or any obligor under any related Additional First Lien Debt Documents.
- "Additional Notes" means additional Notes (other than the Initial Notes) issued from time to time under this Indenture in accordance with Sections 2.01 and 4.09 hereof.
- "Affiliate" of any specified Person means any other Person directly or indirectly controlling or controlled by or under direct or indirect common control with such specified Person. For purposes of this definition, "control" (including, with correlative meanings, the terms "controlling," "controlled by" and "under common control with"), as used with respect to any Person, shall mean the possession, directly or indirectly, of the power to direct or cause the direction of the management or policies of such Person, whether through the ownership of voting securities, by agreement or otherwise.

"Agent" means any Registrar or Paying Agent.

- "Applicable Authorized Representative" shall have the meaning set forth in the Intercreditor Agreement.
- "Applicable Currency Equivalent" means, with respect to any monetary amount in a currency other than U.S. dollars, at any time for the determination thereof, the amount of U.S. dollars obtained by converting such foreign currency involved in such computation into U.S. dollars, at the spot rate for the purchase of U.S. dollars, with the applicable foreign currency as quoted by Reuters at approximately 10:00 A.M. (New York time) on the date that is two Business Days prior to such determination.
 - "Applicable Premium" means, with respect to any Note on any Redemption Date, the greater of:
 - (1) 1.0% of the principal amount of such Note; and
 - (2) the excess, if any, of (a) the present value at such Redemption Date of (i) the redemption price of such Note at November 15, 2016 (such redemption price being set forth in Section 3.07(d) hereof) plus (ii) all required interest payments due on such Note through November 15, 2016 (excluding accrued but unpaid interest to the Redemption Date), computed using a discount rate equal to the Treasury Rate as of such Redemption Date plus 50 basis points; over (b) the principal amount of such Note.

The Applicable Premium shall be calculated, or caused to be calculated, by the Issuer. The Issuer shall deliver such calculation to the Trustee prior to the applicable Redemption Date, and the Trustee shall not be responsible for such calculation.

"<u>Applicable Procedures</u>" means, with respect to any transfer or exchange of or for beneficial interests in any Global Note, the rules and procedures of the Depositary that apply to such transfer or exchange.

"Asset Sale" means:

- (1) the sale, conveyance, transfer or other disposition, whether in a single transaction or a series of related transactions, of property or assets (including by way of a Sale and Lease-Back Transaction) of Holdings III or any of its Restricted Subsidiaries (each referred to in this definition as a "disposition"); or
- (2) the issuance or sale of Equity Interests of any Restricted Subsidiary (other than Preferred Stock of Restricted Subsidiaries issued in compliance with Section 4.09 hereof), whether in a single transaction or a series of related transactions;

in each case, other than:

(a) any disposition of Cash Equivalents or Investment Grade Securities or obsolete or worn out equipment in the ordinary course of business or any disposition of inventory or goods (or other assets) no longer used in the ordinary course of business;

- (b) the disposition of all or substantially all of the assets of Holdings III or the Issuer in a manner permitted pursuant to the provisions described under Section 5.01 hereof or any disposition that constitutes a Change of Control pursuant to this Indenture;
 - (c) the making of any Restricted Payment or Permitted Investment that is permitted to be made, and is made, under Section 4.07 hereof;
- (d) any disposition of assets or issuance or sale of Equity Interests of any Restricted Subsidiary in any transaction or series of related transactions with an aggregate fair market value of less than \$50.0 million;
- (e) any disposition of property or assets by Holdings III or a Restricted Subsidiary of Holdings III, or the issuance of securities by a Restricted Subsidiary of Holdings III, in either case, to Holdings III or another Restricted Subsidiary of Holdings III;
- (f) to the extent allowable under Section 1031 of the Internal Revenue Code of 1986, any exchange of like property (excluding any boot thereon) for use in a Similar Business;
 - (g) the lease, assignment or sub-lease of any real or personal property in the ordinary course of business;
 - (h) any issuance or sale of Equity Interests in, or Indebtedness or other securities of, an Unrestricted Subsidiary;
 - (i) foreclosures, condemnation or any similar action on assets or the granting of Liens not prohibited by this Indenture;
- (j) sales of accounts receivable, or participations therein, or Securitization Assets or related assets in connection with any Qualified Securitization Facility;
- (k) any financing transaction with respect to property built or acquired by Holdings III or any Restricted Subsidiary after the Issue Date, including Sale and Lease-Back Transactions and asset securitizations permitted by this Indenture;
- (l) the sale or discount of inventory, accounts receivable or notes receivable in the ordinary course of business or the conversion of accounts receivable to notes receivable;
- (m) the licensing or sub-licensing of intellectual property or other general intangibles in the ordinary course of business, other than the licensing of intellectual property on a long-term basis;
- (n) the licensing or sub-licensing of intellectual property or other general intangibles on a long-term basis in the ordinary course or business and which do not materially interfere with the business of Holdings III and its Subsidiaries, taken as a whole;

- (o) any surrender or waiver of contract rights or the settlement, release or surrender of contract rights or other litigation claims in the ordinary course of business; and
 - (p) any 300 Millimeter Asset Sale.
- "Authorized Person" of the Issuer or any other Person means the person or persons authorized to act on behalf of such entity by its chief executive officer, president, chief operating officer, chief financial officer or any vice president (or the equivalent of any of the foregoing) or its Board of Directors or any other governing body of such entity.
 - "Bankruptcy Law" means Title 11, U.S. Code or any similar federal or state law for the relief of debtors.
 - "Business Day" means each day which is not a Legal Holiday.
 - "Capital Stock" means:
 - (1) in the case of a corporation, corporate stock;
 - (2) in the case of an association or business entity, any and all shares, interests, participations, rights or other equivalents (however designated) of corporate stock;
 - (3) in the case of a partnership or limited liability company, partnership or membership interests (whether general or limited); and
 - (4) any other interest or participation that confers on a Person the right to receive a share of the profits and losses of, or distributions of assets of, the issuing Person.
- "<u>Capitalized Lease Obligation</u>" means, at the time any determination thereof is to be made, the amount of the liability in respect of a capital lease that would at such time be required to be capitalized and reflected as a liability on a balance sheet (excluding the footnotes thereto) prepared in accordance with GAAP.

"<u>Capitalized Software Expenditures</u>" shall mean, for any period, the aggregate of all expenditures (whether paid in cash or accrued as liabilities) by a Person and its Restricted Subsidiaries during such period in respect of licensed or purchased software or internally developed software and software enhancements that, in conformity with GAAP, are or are required to be reflected as capitalized costs on the consolidated balance sheet of a Person and its Restricted Subsidiaries.

"Cash Equivalents" means:

- (1) United States dollars;
- (2) (a) pounds sterling, euros or any national currency of any participating member state of the EMU; or
- (b) in the case of any Foreign Subsidiary that is a Restricted Subsidiary, such local currencies held by them from time to time in the ordinary course of business:
- (3) securities issued or directly and fully and unconditionally guaranteed or insured by the U.S. government or any agency or instrumentality thereof the securities of which are unconditionally guaranteed as a full faith and credit obligation of such government with maturities of 24 months or less from the date of acquisition;
- (4) certificates of deposit, time deposits and eurodollar time deposits with maturities of one year or less from the date of acquisition, bankers' acceptances with maturities not exceeding one year and overnight bank deposits, in each case with any domestic or foreign commercial bank having capital and surplus of not less than \$500.0 million in the case of U.S. banks and \$100.0 million (or the U.S. dollar equivalent as of the date of determination) in the case of non-U.S. banks;
- (5) repurchase obligations for underlying securities of the types described in clauses (3), (4) and (8) entered into with any financial institution meeting the qualifications specified in clause (4) above;
- (6) commercial paper rated at least P-1 by Moody's or at least A-1 by S&P and in each case maturing within 24 months after the date of creation thereof and Indebtedness or Preferred Stock issued by Persons with a rating of "A" or higher from S&P or "A2" or higher from Moody's with maturities of 24 months or less from the date of acquisition;
- (7) marketable short-term money market and similar securities having a rating of at least P-2 or A-2 from either Moody's or S&P, respectively (or, if at any time neither Moody's nor S&P shall be rating such obligations, an equivalent rating from another Rating Agency) and in each case maturing within 24 months after the date of creation or acquisition thereof;
- (8) readily marketable direct obligations issued by any state, commonwealth or territory of the United States or any political subdivision or taxing authority thereof having an Investment Grade Rating from either Moody's or S&P with maturities of 24 months or less from the date of acquisition;

- (9) readily marketable direct obligations issued by any foreign government or any political subdivision or public instrumentality thereof, in each case having an Investment Grade Rating from either Moody's or S&P with maturities of 24 months or less from the date of acquisition;
- (10) Investments with average maturities of 12 months or less from the date of acquisition in money market funds rated AAA- (or the equivalent thereof) or better by S&P or Aaa3 (or the equivalent thereof) or better by Moody's; and
 - (11) investment funds investing 90% of their assets in securities of the types described in clauses (1) through (10) above.

Notwithstanding the foregoing, Cash Equivalents shall include amounts denominated in currencies other than those set forth in clauses (1) and (2) above, <u>provided</u> that such amounts are converted into any currency listed in clauses (1) and (2) as promptly as practicable and in any event within ten Business Days following the receipt of such amounts.

At any time at which the value, calculated in accordance with GAAP, of all investments of Holdings III and its Restricted Subsidiaries that were deemed, when made, to be Cash Equivalents in accordance with clauses (1) through (11) above exceeds the Indebtedness of Holdings III and its Restricted Subsidiaries, "Cash Equivalents" shall also mean any investment (a "Qualifying Investment") that satisfies the following two conditions: (a) the Qualifying Investment is of a type described in clauses (1) through (11) of this definition, but has an effective maturity (whether by reason of final maturity, a put option or, in the case of an asset-backed security, an average life) of five years and one month or less from the date of such Qualifying Investment (notwithstanding any provision contained in such clauses (1) through (10) requiring a shorter maturity); and (b) the weighted average effective maturity of such Qualifying Investment and all other investments that were made as Qualifying Investments in accordance with this paragraph, does not exceed two years from the date of such Qualifying Investment.

"Change of Control" means the occurrence of any of the following:

- (1) the sale, lease or transfer, in one or a series of related transactions, of all or substantially all of the assets of Holdings III and its Subsidiaries, taken as a whole, to any Person other than a Permitted Holder; or
- (2) Holdings III becomes aware of (by way of a report or any other filing pursuant to Section 13(d) of the Exchange Act, proxy, vote, written notice or otherwise) the acquisition by any Person or group (within the meaning of Section 13(d)(3) or Section 14(d)(2) of the Exchange Act, or any successor provision), including any group acting for the purpose of acquiring, holding or disposing of securities (within the meaning of Rule 13d-5(b)(1) under the Exchange Act), other than one or more Permitted Holders, in a single transaction or in a related series of transactions, by way of merger, amalgamation,

consolidation or other business combination or purchase of beneficial ownership (within the meaning of Rule 13d-3 under the Exchange Act, or any successor provision) of 50% or more of the total voting power of the Voting Stock of Holdings III (directly or through the acquisition of voting power of Voting Stock of any of Holdings III's direct or indirect parent companies).

"Clearstream" means Clearstream Banking, Société Anonyme.

"Collateral" means all assets and properties subject to Liens created pursuant to any Collateral Document to secure any Obligation under the Notes.

"Collateral Agent" means Citibank, N.A., in its capacity as collateral agent for the Trustee and the Holders under the Security Agreement, and any successor thereof.

"Collateral Documents" means collectively, the Senior Credit Agreement Collateral Documents, the Additional First Lien Debt Collateral Documents and the Intercreditor Agreement.

"Consolidated Depreciation and Amortization Expense" means with respect to any Person for any period, the total amount of depreciation and amortization expense, including the amortization of deferred financing fees or costs and Capitalized Software Expenditures of such Person and its Restricted Subsidiaries for such period on a consolidated basis and otherwise determined in accordance with GAAP.

"Consolidated Interest Expense" means, with respect to any Person for any period, without duplication, the sum of:

(1) consolidated interest expense of such Person and its Restricted Subsidiaries for such period, to the extent such expense was deducted (and not added back) in computing Consolidated Net Income (including (a) amortization of original issue discount resulting from the issuance of Indebtedness at less than par, (b) all commissions, discounts and other fees and charges owed with respect to letters of credit or bankers acceptances, (c) non-cash interest payments (but excluding any non-cash interest expense attributable to the movement in the mark to market valuation of Hedging Obligations or other derivative instruments pursuant to GAAP), (d) the interest component of Capitalized Lease Obligations, and (e) net payments, if any made (less net payments, if any, received), pursuant to interest rate Hedging Obligations with respect to Indebtedness, and excluding (t) any expense resulting from the discounting of any Indebtedness in connection with the application of purchase accounting in connection with the Transaction or any acquisition, (u) penalties and interest relating to taxes, (v) any "additional interest" with respect to the Existing Senior Notes, the Existing Senior Subordinated Notes or other securities, (w) amortization of deferred financing fees, debt issuance costs, commissions, fees and expenses, (x) any expensing of bridge, commitment and other financing fees, (y) commissions, discounts, yield and other fees and charges (including any interest expense) related to any Qualified Securitization Facility and (z) any accretion of accrued interest on discounted liabilities); plus

- (2) consolidated capitalized interest of such Person and its Restricted Subsidiaries for such period, whether paid or accrued; less
- (3) interest income for such period.

For purposes of this definition, interest on a Capitalized Lease Obligation shall be deemed to accrue at an interest rate reasonably determined by such Person to be the rate of interest implicit in such Capitalized Lease Obligation in accordance with GAAP.

- "Consolidated Net Income" means, with respect to any Person for any period, the aggregate of the Net Income of such Person and its Restricted Subsidiaries for such period, on a consolidated basis, and otherwise determined in accordance with GAAP; provided, that, without duplication,
 - (1) any after-tax effect of extraordinary, non-recurring or unusual gains or losses (less all fees and expenses relating thereto) or expenses (including relating to the Transaction or any multi-year strategic initiatives), severance, relocation costs and curtailments or modifications to pension and post-retirement employee benefit plans shall be excluded,
 - (2) the Net Income for such period shall not include the cumulative effect of a change in accounting principles and changes as a result of the adoption or modification of accounting policies during such period,
 - (3) any net after-tax gains or losses on disposal of disposed, abandoned or discontinued operations shall be excluded,
 - (4) any after-tax effect of gains or losses (less all fees and expenses relating thereto) attributable to asset dispositions or abandonments or the sale or other disposition of any Capital Stock of any Person other than in the ordinary course of business shall be excluded,
 - (5) the Net Income for such period of any Person that is not a Subsidiary, or is an Unrestricted Subsidiary, or that is accounted for by the equity method of accounting, shall be excluded; <u>provided</u> that Consolidated Net Income of Holdings III shall be increased by the amount of dividends or distributions or other payments that are actually paid in cash (or to the extent converted into cash) to Holdings III or a Restricted Subsidiary thereof in respect of such period,
 - (6) solely for the purpose of determining the amount available for Restricted Payments under clause (3)(A) of Section 4.07(a) hereof, the Net Income for such period of any Restricted Subsidiary (other than any Guarantor) shall be excluded to the extent that the declaration or payment of dividends or

similar distributions by that Restricted Subsidiary of its Net Income is not at the date of determination permitted without any prior governmental approval (which has not been obtained) or, directly or indirectly, by the operation of the terms of its charter or any agreement, instrument, judgment, decree, order, statute, rule, or governmental regulation applicable to that Restricted Subsidiary or its stockholders, unless such restriction with respect to the payment of dividends or similar distributions has been legally waived, <u>provided</u> that Consolidated Net Income of Holdings III will be increased by the amount of dividends or other distributions or other payments actually paid in cash (or to the extent converted into cash) to Holdings III or a Restricted Subsidiary thereof in respect of such period, to the extent not already included therein,

- (7) effects of adjustments (including the effects of such adjustments pushed down to Holdings III and its Restricted Subsidiaries) in the inventory, property and equipment, software, goodwill, other intangible assets, in-process research and development, deferred revenue and debt line items in such Person's consolidated financial statements pursuant to GAAP resulting from the application of purchase accounting in relation to the Transaction or any consummated acquisition or the amortization or write-off of any amounts thereof, net of taxes, shall be excluded,
- (8) any after-tax effect of income (loss) from the early extinguishment of (i) Indebtedness, (ii) Hedging Obligations or (iii) other derivative instruments shall be excluded,
- (9) any impairment charge or asset write-off or write-down, including impairment charges or asset write-offs or write-downs related to intangible assets, long-lived assets, investments in debt and equity securities or as a result of a change in law or regulation, in each case, pursuant to GAAP, and the amortization of intangibles arising pursuant to GAAP shall be excluded,
- (10) any non-cash compensation charge or expense including any such charge arising from the grants of stock appreciation or similar rights, stock options, restricted stock or other rights shall be excluded,
- (11) any fees and expenses incurred during such period, or any amortization thereof for such period, in connection with any acquisition, Investment, Asset Sale, issuance or repayment of Indebtedness, issuance of Equity Interests, refinancing transaction or amendment or modification of any debt instrument (in each case, including any such transaction consummated prior to the Issue Date and any such transaction undertaken but not completed) and any charges or non-recurring merger costs incurred during such period as a result of any such transaction shall be excluded,
 - (12) [intentionally omitted]; and

- (13) the following items shall be excluded:
- (a) any net unrealized gain or loss (after any offset) resulting in such period from Hedging Obligations and the application of Statement of Financial Accounting Standards No. 133; and
- (b) any net unrealized gain or loss (after any offset) resulting in such period from currency translation gains or losses including those (i) related to currency remeasurements of Indebtedness and (ii) resulting from hedge agreements for currency exchange risk.

In addition, to the extent not already included in the Consolidated Net Income of such Person and its Restricted Subsidiaries, notwithstanding anything to the contrary in the foregoing, Consolidated Net Income shall include the amount of proceeds received from business interruption insurance and reimbursements of any expenses and charges that are covered by indemnification or other reimbursement provisions in connection with any Permitted Investment or any sale, conveyance, transfer or other disposition of assets permitted under this Indenture.

Notwithstanding the foregoing, for the purpose of Section 4.07 hereof only (other than clause (3)(D) of Section 4.07(a) hereof), there shall be excluded from Consolidated Net Income any income arising from any sale or other disposition of Restricted Investments made by Holdings III and its Restricted Subsidiaries, any repurchases and redemptions of Restricted Investments from Holdings III and its Restricted Subsidiaries, any repayments of loans and advances which constitute Restricted Investments by Holdings III or any of its Restricted Subsidiaries, any sale of the stock of an Unrestricted Subsidiary or any distribution or dividend from an Unrestricted Subsidiary, in each case only to the extent such amounts increase the amount of Restricted Payments permitted under clause (3)(D) of Section 4.07(a) hereof.

"Consolidated Secured Debt Ratio" as of any date of determination means, the ratio of (1) Consolidated Total Indebtedness of Holdings III and its Restricted Subsidiaries that is secured by Liens as of the end of the most recent fiscal quarter for which internal financial statements are available immediately preceding the date on which such event for which such calculation is being made shall occur to (2) Holdings III's EBITDA for the most recently ended four full fiscal quarters for which internal financial statements are available immediately preceding the date on which such event for which such calculation is being made shall occur, in each case with such pro forma adjustments to Consolidated Total Indebtedness and EBITDA as are appropriate and consistent with the pro forma adjustment provisions set forth in the definition of Fixed Charge Coverage Ratio.

"Consolidated Total Indebtedness" means, as at any date of determination, an amount equal to the sum of (1) the aggregate amount of all outstanding Indebtedness of Holdings III and its Restricted Subsidiaries on a consolidated basis consisting of Indebtedness for borrowed money, Obligations in respect of Capitalized Lease

Obligations and debt obligations evidenced by promissory notes and similar instruments (and excluding, for the avoidance of doubt, all obligations relating to Qualified Securitization Facilities) and (2) the aggregate amount of all outstanding Disqualified Stock of Holdings III and all Preferred Stock of its Restricted Subsidiaries on a consolidated basis, with the amount of such Disqualified Stock and Preferred Stock equal to the greater of their respective voluntary or involuntary liquidation preferences and maximum fixed repurchase prices, in each case determined on a consolidated basis in accordance with GAAP. For purposes hereof, the "maximum fixed repurchase price" of any Disqualified Stock or Preferred Stock that does not have a fixed repurchase price shall be calculated in accordance with the terms of such Disqualified Stock or Preferred Stock as if such Disqualified Stock or Preferred Stock were purchased on any date on which Consolidated Total Indebtedness shall be required to be determined pursuant to this Indenture, and if such price is based upon, or measured by, the fair market value of such Disqualified Stock or Preferred Stock, such fair market value shall be determined reasonably and in good faith by Holdings III.

"Contingent Obligations" means, with respect to any Person, any obligation of such Person guaranteeing any leases, dividends or other obligations that do not constitute Indebtedness ("primary obligations") of any other Person (the "primary obligor") in any manner, whether directly or indirectly, including, without limitation, any obligation of such Person, whether or not contingent,

- (1) to purchase any such primary obligation or any property constituting direct or indirect security therefor,
- (2) to advance or supply funds
 - (a) for the purchase or payment of any such primary obligation, or
- (b) to maintain working capital or equity capital of the primary obligor or otherwise to maintain the net worth or solvency of the primary obligor, or
- (3) to purchase property, securities or services primarily for the purpose of assuring the owner of any such primary obligation of the ability of the primary obligor to make payment of such primary obligation against loss in respect thereof.

"Corporate Trust Office of the Trustee" shall be at the address of the Trustee specified in Section 13.01 hereof or such other address as to which the Trustee may give notice to the Holders and the Issuer.

"Credit Facilities" means, with respect to Holdings III or any of its Restricted Subsidiaries, one or more debt facilities, including the Senior Credit Facilities, or other financing arrangements (including, without limitation, commercial paper facilities or indentures) providing for revolving credit loans, term loans, letters of credit

or other long-term indebtedness, including any notes, mortgages, guarantees, collateral documents, instruments and agreements executed in connection therewith, and any amendments, supplements, modifications, extensions, renewals, restatements or refundings thereof and any indentures or credit facilities or commercial paper facilities that replace, refund or refinance any part of the loans, notes, other credit facilities or commitments thereunder, including any such replacement, refunding or refinancing facility or indenture that increases the amount permitted to be borrowed thereunder or alters the maturity thereof (provided that such increase in borrowings is permitted under Section 4.09 hereof) or adds Restricted Subsidiaries as additional borrowers or guarantors thereunder and whether by the same or any other agent, lender or group of lenders.

"Custodian" means the Trustee, as custodian with respect to the Notes, each in global form, or any successor entity thereto.

"Default" means any event that is, or with the passage of time or the giving of notice or both would be, an Event of Default.

"<u>Definitive Note</u>" means a certificated Note registered in the name of the Holder thereof and issued in accordance with Section 2.06(c) hereof, substantially in the form of <u>Exhibit A</u> hereto except that such Note shall not bear the Global Note Legend and shall not have the "Schedule of Exchanges of Interests in the Global Note" attached thereto.

"<u>Depositary</u>" means, with respect to the Notes issuable or issued in whole or in part in global form, any Person specified in Section 2.03 hereof as the Depositary with respect to the Notes, and any and all successors thereto appointed as Depositary hereunder and having become such pursuant to the applicable provision of this Indenture.

"<u>Designated Non-cash Consideration</u>" means the fair market value of non-cash consideration received by Holdings III or a Restricted Subsidiary in connection with an Asset Sale that is so designated as Designated Non-cash Consideration pursuant to an Officer's Certificate, setting forth the basis of such valuation, executed by the principal financial officer of Holdings III, less the amount of cash or Cash Equivalents received in connection with a subsequent sale of or collection on such Designated Non-cash Consideration.

"<u>Designated Preferred Stock</u>" means Preferred Stock of Holdings III or any parent corporation thereof (in each case other than Disqualified Stock) that is issued for cash (other than to a Restricted Subsidiary or an employee stock ownership plan or trust established by Holdings III or any of its Subsidiaries) and is so designated as Designated Preferred Stock, pursuant to an Officer's Certificate executed by the principal financial officer of Holdings III or the applicable parent corporation thereof, as the case may be, on the issuance date thereof, the cash proceeds of which are excluded from the calculation set forth in clause (3) of Section 4.07(a) hereof.

"<u>Directing Agent</u>" means Citibank, N.A., as the agent for the collateral agents under the Senior Credit Facilities Documents, the collateral agent under the Collateral Documents relating to the Existing Secured Notes, the Collateral Agent and each additional Authorized Representative (as defined in the Intercreditor Agreement) from time to time party to the Intercreditor Agreement, and any successor thereof or replacement agent appointed in accordance with the terms of the Intercreditor Agreement.

"Disqualified Stock" means, with respect to any Person, any Capital Stock of such Person which, by its terms, or by the terms of any security into which it is convertible or for which it is putable or exchangeable, or upon the happening of any event, matures or is mandatorily redeemable (other than solely as a result of a change of control or asset sale) pursuant to a sinking fund obligation or otherwise, or is redeemable at the option of the holder thereof (other than solely as a result of a change of control or asset sale), in whole or in part, in each case prior to the date 91 days after the earlier of the maturity date of the Notes or the date the Notes are no longer outstanding; provided, that if such Capital Stock is issued to any plan for the benefit of employees of Holdings III or its Subsidiaries or by any such plan to such employees, such Capital Stock shall not constitute Disqualified Stock solely because it may be required to be repurchased by Holdings III or its Subsidiaries in order to satisfy applicable statutory or regulatory obligations.

"Domestic Subsidiary" means any Subsidiary that is organized under the laws of the United States, any state thereof or the District of Columbia.

- "EBITDA" means, with respect to any Person for any period, the Consolidated Net Income of such Person for such period
- (1) increased (without duplication) by the following, in each case to the extent deducted in determining Consolidated Net Income for such period:
- (a) provision for taxes based on income or profits or capital, including, without limitation, state, franchise and similar taxes (such as the Pennsylvania capital tax and Texas margin tax) and foreign withholding taxes of such Person paid or accrued during such period deducted (and not added back) in computing Consolidated Net Income; <u>plus</u>
- (b) Fixed Charges of such Person for such period (including (x) net losses or Hedging Obligations or other derivative instruments entered into for the purpose of hedging interest rate risk, (y) bank fees and (z) costs of surety bonds in connection with financing activities, plus amounts excluded from Consolidated Interest Expense as set forth in clauses (1)(t) through (z) in the definition thereof) to the extent the same were deducted (and not added back) in calculating such Consolidated Net Income; plus

- (c) Consolidated Depreciation and Amortization Expense of such Person for such period to the extent the same were deducted (and not added back) in computing Consolidated Net Income; <u>plus</u>
- (d) any expenses or charges (other than depreciation or amortization expense) related to any Equity Offering, Permitted Investment, acquisition, disposition, recapitalization or the incurrence of Indebtedness permitted to be incurred by this Indenture (including a refinancing thereof) (whether or not successful), including (i) such fees, expenses or charges related to the offering of the Notes, the Existing Senior Notes, the Existing Senior Subordinated Notes and the Credit Facilities and (ii) any amendment or other modification of the Notes, the Existing Secured Notes, the Existing Senior Notes, the Existing Senior Subordinated Notes and the Credit Facilities and, in each case, deducted (and not added back) in computing Consolidated Net Income; plus
- (e) the amount of any restructuring charges, integration costs or other business optimization expenses (including cost and expenses relating to inventory optimization programs, wafer fabrication facility closures and new systems design and implementation costs) or reserves deducted (and not added back) in such period in computing Consolidated Net Income, including any one-time costs incurred in connection with acquisitions after the Measurement Date, and costs related to the closure and/or consolidation of facilities; <u>plus</u>
- (f) any other non-cash charges, including any write offs or write downs reducing Consolidated Net Income for such period (<u>provided</u> that if any such non-cash charges represent an accrual or reserve for potential cash items in any future period, the cash payment in respect thereof in such future period shall be subtracted from EBITDA to such extent, and excluding amortization of a prepaid cash item that was paid in a prior period); <u>plus</u>
- (g) the amount of any minority interest expense consisting of Subsidiary income attributable to minority equity interests of third parties in any non-Wholly Owned Subsidiary deducted (and not added back) in such period in calculating Consolidated Net Income; <u>plus</u>
 - (h) [intentionally omitted]; plus
- (i) the amount of net cost savings projected by Holdings III in good faith to be realized as a result of specified actions taken or initiated during or prior to such period (calculated on a <u>pro forma</u> basis as though such cost savings had been realized on the first day of such period), net of the amount of actual benefits realized during such period from such

actions; <u>provided</u> that (x) such cost savings are reasonably identifiable and factually supportable, (y) such actions are taken no later than 36 months after the Measurement Date and (z) the aggregate amount of cost savings added pursuant to this clause (i) shall not exceed \$200 million for any four consecutive quarter period (which adjustments may be incremental to <u>pro forma</u> cost savings adjustments made pursuant to the definition of "Fixed Charge Coverage Ratio"); <u>plus</u>

- (j) the amount of loss on sale of receivables, Securitization Assets and related assets to the Securitization Subsidiary in connection with a Qualified Securitization Facility; <u>plus</u>
- (k) any costs or expense incurred by Holdings III or a Restricted Subsidiary pursuant to any management equity plan or stock option plan or any other management or employee benefit plan or agreement or any stock subscription or shareholder agreement, to the extent that such cost or expenses are funded with cash proceeds contributed to the capital of Holdings III or net cash proceeds of an issuance of Equity Interest of Holdings III (other than Disqualified Stock) solely to the extent that such net cash proceeds are excluded from the calculation set forth in clause (3) of Section 4.07(a) hereof; plus
- (l) cash receipts (or any netting arrangements resulting in reduced cash expenditures) not representing EBITDA or Net Income in any period to the extent non-cash gains relating to such income were deducted in the calculation of EBITDA pursuant to clause (2) below for any previous period and not added back; plus
 - (m) any net loss from disposed or discontinued operations; plus
 - (n) interest income or investment earnings on retiree medical and intellectual property, royalty or license receivables; plus
- (o) 300 Millimeter R&D Expenses to the extent that the amount of such 300 Millimeter R&D Expenses could have been made as investments under clause (18) of the definition of "Permitted Investments";
- (2) decreased by (without duplication) by the following, in each case to the extent included in determining Consolidated Net Income for such period:
 - (a) non-cash gains increasing Consolidated Net Income of such Person for such period, excluding any non-cash gains to the extent they represent the reversal of an accrual or reserve for a potential cash item that reduced EBITDA in any prior period and any non-cash gains with respect to cash actually received in a prior period so long as such cash did not increase EBITDA in such prior period; <u>plus</u>

- (b) any net income from disposed or discontinued operations; and
- (3) increased or decreased by (without duplication), as applicable, any adjustments resulting from the application of FASB Interpretation No. 45 (Guarantees).
 - "EMU" means economic and monetary union as contemplated in the Treaty on European Union.
- "Equalization Payment" means, with respect to any period for any 300 Millimeter Arrangement, the payment made by Holdings III or any of its Restricted Subsidiaries in respect of its applicable share, determined pursuant to the terms of such 300 Millimeter Arrangement, of the depreciation and amortization expenses or charges in respect of capital expenditures made with respect to such 300 Millimeter Arrangement for such period that are recorded as research and development expenses of, but do not otherwise constitute Consolidated Depreciation and Amortization Expense of, Holdings III and its Restricted Subsidiaries on a consolidated basis for such period.
- "Equity Interests" means Capital Stock and all warrants, options or other rights to acquire Capital Stock, but excluding any debt security that is convertible into, or exchangeable for, Capital Stock.
- "<u>Equity Offering</u>" means any public or private sale of common stock or Preferred Stock of Holdings III or any of its direct or indirect parent companies (excluding Disqualified Stock), other than:
 - (1) public offerings with respect to Holdings III's or any direct or indirect parent company's common stock registered on Form S-4 or Form S-8;
 - (2) issuances to any Subsidiary of Holdings III; and
 - (3) any such public or private sale that constitutes an Excluded Contribution.
 - "euro" means the single currency of participating member states of the EMU.
 - "Euroclear" means Euroclear S.A./N.V., as operator of the Euroclear system.
 - "Exchange Act" means the Securities Exchange Act of 1934, as amended, and the rules and regulations of the SEC promulgated thereunder.
 - "Excluded Assets" means certain items of property, as provided in the Collateral Documents relating to the Notes.

- "Excluded Contribution" means net cash proceeds, marketable securities or Qualified Proceeds received by Holdings III from
- (1) contributions to its common equity capital, and
- (2) the sale (other than to a Subsidiary of Holdings III or to any management equity plan or stock option plan or any other management or employee benefit plan or agreement of Holdings III) of Capital Stock (other than Disqualified Stock and Designated Preferred Stock) of Holdings III,

in each case designated as Excluded Contributions pursuant to an officer's certificate executed by the principal financial officer of Holdings III on the date such capital contributions are made or the date such Capital Stock is sold, as the case may be, which are excluded from the calculation set forth in clause (3) of Section 4.07(a) hereof.

"Excluded Proceeds" has the meaning specified in the definition of "Net Proceeds."

"Existing Secured Notes" means the Issuer's (a) 9 $\frac{1}{4}$ % Senior Secured Notes due 2018 issued pursuant to the Indenture dated as of April 13, 2010, among the Issuer, the Guarantors listed therein and the Bank of New York Mellon Trust Company, N.A., as Trustee and (b) 5.000% Senior Secured Notes due 2021 issued pursuant to the Indenture dated as of May 21, 2013 among the Issuer, the Guarantors listed therein and the Bank of New York Mellon Trust Company, N.A., as Trustee, in the case of the 9 $\frac{1}{4}$ % Senior Secured Notes due 2018 to the extent no redemption notice has been issued therefor on the Issue Date or not redeemed with the proceeds of the Notes within 45 days of the Issue Date.

"Existing Senior Notes" means (a) the Issuer's Senior Floating Rate Notes due 2014 issued pursuant to the Indenture dated as of December 1, 2006, among the Issuer, the Guarantors listed therein and The Bank of New York Mellon, as Trustee, (b) the Issuer's 10 ¾% Senior Notes due 2020 issued pursuant to the Indenture, dated as of September 30, 2010, among the Issuer, the Guarantors listed therein and The Bank of New York Mellon Trust Company, N.A., as Trustee, and (c) the Issuer's 8.05% Senior Notes due 2020 issued pursuant to the Indenture, dated as of June 10, 2011, among the Issuer, the Guarantors listed therein and The Bank of New York Mellon Trust Company, N.A., as Trustee.

"Existing Senior Subordinated Notes" means the Issuer's 10 1/8% Senior Subordinated Notes due 2016 issued pursuant to the Indenture dated as of December 1, 2006, among the Issuer, the Guarantors listed therein and The Bank of New York Mellon as Trustee.

"fair market value" means, with respect to any asset or liability, the fair market value of such asset or liability as determined by Holdings III in good faith; provided that if the fair market value is equal to or exceeds \$100.0 million, such determination shall be made by the board of directors of Holdings III in good faith.

"<u>First Lien</u>" means the liens on the Collateral in favor of the Secured Parties under the Collateral Documents relating to the Notes and the other Secured Parties under the other Collateral Documents.

"First Lien Debt Documents" means the Intercreditor Agreement, the Senior Credit Facilities Documents and any Additional First Lien Debt Documents.

"First Lien Obligations" means the Senior Credit Agreement Obligations and any Additional First Lien Debt Obligations.

"Fixed Charge Coverage Ratio" means, with respect to any Person for any period, the ratio of EBITDA of such Person for such period to the Fixed Charges of such Person for such period. In the event that Holdings III or any Restricted Subsidiary incurs, assumes, guarantees, redeems, retires or extinguishes any Indebtedness (other than Indebtedness incurred under any revolving credit facility unless such Indebtedness has been permanently repaid and has not been replaced) or issues or redeems Disqualified Stock or Preferred Stock subsequent to the commencement of the period for which the Fixed Charge Coverage Ratio is being calculated but prior to or simultaneously with the event for which the calculation of the Fixed Charge Coverage Ratio is made (the "Fixed Charge Coverage Ratio Calculation Date"), then the Fixed Charge Coverage Ratio shall be calculated giving pro forma effect to such incurrence, assumption, guarantee, redemption, retirement or extinguishment of Indebtedness, or such issuance or redemption of Disqualified Stock or Preferred Stock, as if the same had occurred at the beginning of the applicable four-quarter period.

For purposes of making the computation referred to above, Investments, acquisitions, dispositions, mergers, amalgamations, consolidations and disposed operations (as determined in accordance with GAAP) that have been made by Holdings III or any of its Restricted Subsidiaries during the four-quarter reference period or subsequent to such reference period and on or prior to or simultaneously with the Fixed Charge Coverage Ratio Calculation Date shall be calculated on a <u>pro forma</u> basis assuming that all such Investments, acquisitions, dispositions, mergers, amalgamations, consolidations and disposed operations (and the change in any associated fixed charge obligations and the change in EBITDA resulting therefrom) had occurred on the first day of the four-quarter reference period. If since the beginning of such period any Person that subsequently became a Restricted Subsidiary or was merged with or into Holdings III or any of its Restricted Subsidiaries since the beginning of such period shall have made any Investment, acquisition, disposition, merger, amalgamation, consolidation or disposed operation that would have required adjustment pursuant to this definition, then the Fixed Charge Coverage Ratio shall be calculated giving <u>pro forma</u> effect thereto for such period as if such Investment, acquisition, disposition, merger, consolidation or disposed operation had occurred at the beginning of the applicable four-quarter period.

For purposes of this definition, whenever <u>pro forma</u> effect is to be given to a transaction, Investment, acquisition, disposition, merger, amalgamation or consolidation (including the Transaction) and the amount of income or earnings relating thereto, the <u>pro forma</u> calculations shall be made in good faith by a responsible financial or accounting officer of Holdings III (and may include, for the avoidance of doubt, cost savings and operating expense reductions resulting from such Investment, acquisition, merger, amalgamation or consolidation (including the Transaction) which is being given <u>pro forma</u> effect that have been or are expected to be realized). If any Indebtedness bears a floating rate of interest and is being given <u>pro forma</u> effect, the interest on such Indebtedness shall be calculated as if the rate in effect on the Fixed Charge Coverage Ratio Calculation Date had been the applicable rate for the entire period (taking into account any Hedging Obligations applicable to such Indebtedness). Interest on a Capitalized Lease Obligation shall be deemed to accrue at an interest rate reasonably determined by a responsible financial or accounting officer of Holdings III to be the rate of interest implicit in such Capitalized Lease Obligation in accordance with GAAP. For purposes of making the computation referred to above, interest on any Indebtedness under a revolving credit facility computed on a <u>pro forma</u> basis shall be computed based upon the average daily balance of such Indebtedness during the applicable period except as set forth in the first paragraph of this definition. Interest on Indebtedness that may optionally be determined at an interest rate based upon a factor of a prime or similar rate, a eurocurrency interbank offered rate, or other rate, shall be deemed to have been based upon the rate actually chosen, or, if none, then based upon such optional rate chosen as Holdings III may designate.

"Fixed Charges" means, with respect to any Person for any period, the sum of, without duplication:

- (1) Consolidated Interest Expense of such Person for such period;
- (2) all cash dividends or other distributions paid (excluding items eliminated in consolidation) on any series of Preferred Stock during such period; and
- (3) all cash dividends or other distributions paid (excluding items eliminated in consolidation) on any series of Disqualified Stock during such period.

"Foreign Acquisition Co." means a direct Subsidiary of Holdings III or Holdings IV formed after the Issue Date as a holding company for the Transferred Foreign Subsidiaries and other Foreign Subsidiaries of Holdings III that are not Subsidiaries of Holdings V and (a) that provides a Guarantee and (b) all of whose stock shall be pledged by Holdings III or Holdings IV, as applicable, to secure the Obligations under this Indenture and the Notes, which Foreign Acquisition Co. shall be organized under the laws of Hungary, Luxembourg, The Netherlands, Iceland, Bermuda, Barbados, Mauritius, the British Virgin Islands, Malta, Cyprus or such other jurisdiction requested by Holdings III and reasonably acceptable to the Administrative Agent under the Senior Credit Facilities.

"Foreign Reorganization" means the transfer of any Foreign Subsidiary of the Issuer or any transfer of any assets or property of any Foreign Subsidiary of the Issuer to Foreign Acquisition Co. or any Subsidiary thereof; provided that such transferred Foreign Subsidiary and any Person who holds such transferred assets or property (in each case, a "Transferred Foreign Subsidiary.") shall become a Guarantor of the Obligations under this Indenture and the Notes and Foreign Acquisition Co., shall pledge or cause to be pledged 100% of the Equity Interests of such Transferred Foreign Subsidiary to secure the Obligations under this Indenture and the Notes.

"<u>Foreign Subsidiary</u>" means, with respect to any Person, any Restricted Subsidiary of such Person that is not organized or existing under the laws of the United States, any state thereof, the District of Columbia, or any territory thereof and any Restricted Subsidiary of such Foreign Subsidiary.

"GAAP" means generally accepted accounting principles in the United States which are in effect on the Transaction Date.

"Global Note Legend" means the legend set forth in Section 2.06(f)(ii) hereof, which is required to be placed on all Global Notes issued under this Indenture.

"Global Notes" means, individually and collectively, each of the Restricted Global Notes and the Unrestricted Global Notes, substantially in the form of Exhibit A hereto, issued in accordance with Section 2.01, 2.06(b) or 2.06(d) hereof.

"Government Securities" means securities that are:

- (1) direct obligations of the United States of America for the timely payment of which its full faith and credit is pledged; or
- (2) obligations of a Person controlled or supervised by and acting as an agency or instrumentality of the United States of America the timely payment of which is unconditionally guaranteed as a full faith and credit obligation by the United States of America,

which, in either case, are not callable or redeemable at the option of the issuers thereof, and shall also include a depository receipt issued by a bank (as defined in Section 3(a)(2) of the Securities Act), as custodian with respect to any such Government Securities or a specific payment of principal of or interest on any such Government Securities held by such custodian for the account of the holder of such depository receipt; provided that (except as required by law) such custodian is not authorized to make any deduction from the amount payable to the holder of such depository receipt from any amount received by the custodian in respect of the Government Securities or the specific payment of principal of or interest on the Government Securities evidenced by such depository receipt.

- "guarantee" means a guarantee (other than by endorsement of negotiable instruments for collection in the ordinary course of business), direct or indirect, in any manner (including letters of credit and reimbursement agreements in respect thereof), of all or any part of any Indebtedness or other obligations.
 - "Guarantee" means the guarantee by any Guarantor of the Issuer's Obligations under this Indenture and the Notes.
- "Guarantor" means the Parent Guarantors and each Subsidiary of Holdings III, if any, that Guarantees the Notes in accordance with the terms of this Indenture.
- "Hedging Obligations" means, with respect to any Person, the obligations of such Person under any interest rate swap agreement, interest rate cap agreement, interest rate collar agreement, commodity swap agreement, commodity cap agreement, commodity collar agreement, foreign exchange contract, currency swap agreement or similar agreement providing for the transfer or mitigation of interest rate or currency risks either generally or under specific contingencies.
 - "Holder" means the Person in whose name a Note is registered on the Registrar's books.
 - "Holdings II" means Freescale Semiconductor Holdings II, Ltd., a Bermuda exempted company limited by shares, and its successors.
 - "Holdings III" means Freescale Semiconductor Holdings III, Ltd., a Bermuda exempted company limited by shares, and its successors.
 - "Holdings IV" means Freescale Semiconductor Holdings IV, Ltd., a Bermuda exempted company limited by shares, and its successors.
 - "Holdings V" means Freescale Semiconductor Holdings V, Inc., a Delaware corporation.
 - "Indebtedness" means, with respect to any Person, without duplication:
 - (1) any indebtedness (including principal and premium) of such Person, whether or not contingent:
 - (a) in respect of borrowed money;
 - (b) evidenced by bonds, notes, debentures or similar instruments or letters of credit or bankers' acceptances (or, without duplication, reimbursement agreements in respect thereof);
 - (c) representing the balance deferred and unpaid of the purchase price of any property (including Capitalized Lease Obligations), except

- (i) any such balance that constitutes an obligation in respect of a commercial letter of credit, a trade payable or similar obligation to a trade creditor, in each case accrued in the ordinary course of business and (ii) any earn-out obligations until such obligation becomes a liability on the balance sheet of such Person in accordance with GAAP and if not paid after becoming due and payable;
 - (d) representing any Hedging Obligations; or
- (e) during a Suspension Period only, obligations of the lessee for rental payments in respect of Sale and Lease-Back Transactions in an amount equal to the present value of such obligations during the remaining term of the lease using a discount rate equal to the rate of interest implicit in such transaction determined in accordance with GAAP,

if and to the extent that any of the foregoing Indebtedness (other than letters of credit and Hedging Obligations) would appear as a liability upon a balance sheet (excluding the footnotes thereto) of such Person prepared in accordance with GAAP; <u>provided</u>, that Indebtedness of any direct or indirect parent of Holdings III appearing upon the balance sheet of Holdings III solely by reason of push-down accounting under GAAP shall be excluded.

- (2) to the extent not otherwise included, any obligation by such Person to be liable for, or to pay, as obligor, guarantor or otherwise, on the obligations of the type referred to in clause (1) of a third Person (whether or not such items would appear upon the balance sheet of such obligor or guarantor), other than by endorsement of negotiable instruments for collection in the ordinary course of business; and
- (3) to the extent not otherwise included, the obligations of the type referred to in clause (1) of a third Person secured by a Lien on any asset owned by such first Person, whether or not such Indebtedness is assumed by such first Person;

<u>provided</u>, that notwithstanding the foregoing, Indebtedness shall be deemed not to include (a) Contingent Obligations incurred in the ordinary course of business or (b) obligations under or in respect of Qualified Securitization Facilities.

"Indenture" means this Indenture, as amended or supplemented from time to time.

"<u>Independent Financial Advisor</u>" means an accounting, appraisal, investment banking firm or consultant to Persons engaged in Similar Businesses of nationally recognized standing that is, in the good faith judgment of Holdings III, qualified to perform the task for which it has been engaged.

"Indirect Participant" means a Person who holds a beneficial interest in a Global Note through a Participant.

"Intellectual Property Security Agreement" means the intellectual property security agreement dated on or about the Issue Date, among the Issuer, Holdings V, SigmaTel, the subsidiaries of Holdings III from time to time party thereto and Citibank, N.A., as Collateral Agent, as amended, supplemented, modified, extended, renewed or restated from time to time.

"Intercreditor Agreement" means the Intercreditor Agreement dated February 19, 2010 among the Directing Agent, the collateral agent under the Collateral Documents relating to the Existing Secured Notes, and the collateral agent under the Senior Credit Facilities Documents, the collateral agent under the Incremental Credit Agreement Document (as defined in the Intercreditor Agreement) and each additional and authorized representative from time to time party thereto, as amended and supplemented by the Joinder Agreement to the Intercreditor Agreement, dated on the Issue Date, by the Collateral Agent, and as further amended, supplemented, modified, extended, renewed or restated from time to time.

"Initial Notes" as defined in the recitals hereto.

"Initial Purchasers" means J.P. Morgan Securities LLC, Credit Suisse Securities (USA) LLC, Barclays Capital Inc., Citigroup Global Markets Inc., Deutsche Bank Securities Inc., Goldman, Sachs & Co. and Morgan Stanley & Co. LLC.

"Interest Payment Date" means May 15 and November 15 of each year to stated maturity.

"Investment Grade Rating" means a rating equal to or higher than Baa3 (or the equivalent) by Moody's and BBB- (or the equivalent) by S&P, or an equivalent rating by any other Rating Agency.

"Investment Grade Securities" means:

- (1) securities issued or directly and fully guaranteed or insured by the United States government or any agency or instrumentality thereof (other than Cash Equivalents);
- (2) debt securities or debt instruments with an Investment Grade Rating, but excluding any debt securities or instruments constituting loans or advances among Holdings III and its Subsidiaries;
- (3) investments in any fund that invests exclusively in investments of the type described in clauses (1) and (2) which fund may also hold immaterial amounts of cash pending investment or distribution; and
 - (4) corresponding instruments in countries other than the United States customarily utilized for high quality investments.

"Investments" means, with respect to any Person, all investments by such Person in other Persons (including Affiliates) in the form of loans (including guarantees), advances or capital contributions (excluding accounts receivable, trade credit, advances to customers, commission, travel and similar advances to officers and employees, in each case made in the ordinary course of business), purchases or other acquisitions for consideration of Indebtedness, Equity Interests or other securities issued by any other Person and investments that are required by GAAP to be classified on the balance sheet (excluding the footnotes) of Holdings III in the same manner as the other investments included in this definition to the extent such transactions involve the transfer of cash or other property. For purposes of the definition of "Unrestricted Subsidiary" and Section 4.07 hereof:

- (1) "Investments" shall include the portion (proportionate to Holdings III's equity interest in such Subsidiary) of the fair market value of the net assets of a Subsidiary of Holdings III at the time that such Subsidiary is designated an Unrestricted Subsidiary; <u>provided</u>, that upon a redesignation of such Subsidiary as a Restricted Subsidiary, Holdings III shall be deemed to continue to have a permanent "Investment" in an Unrestricted Subsidiary in an amount (if positive) equal to:
 - (a) Holdings III's "Investment" in such Subsidiary at the time of such redesignation; less
 - (b) the portion (proportionate to Holdings III's Equity Interest in such Subsidiary) of the fair market value of the net assets of such Subsidiary at the time of such redesignation; and
 - (2) any property transferred to or from an Unrestricted Subsidiary shall be valued at its fair market value at the time of such transfer.

The amount of any Investment outstanding at any time shall be the original cost of such Investment, reduced by any dividend, distribution, interest payment, return of capital, repayment or other amount received in cash by Holdings III or a Restricted Subsidiary in respect of such Investment.

"Investors" means The Blackstone Group, The Carlyle Group, Permira funds advised by Permira Advisers LLC, Texas Pacific Group and, if applicable, each of their respective Affiliates and funds or partnerships managed by any of them or their respective Affiliates but not including, however, any portfolio companies of any of the foregoing.

"Issue Date" means November 1, 2013.

- "Issuer" means Freescale Semiconductor, Inc., a Delaware corporation (and not any of its Subsidiaries), and its successors.
- "Issuer Order" means a written request or order signed on behalf of the Issuer by an Officer of the Issuer, who must be the principal executive officer, the principal financial officer, the treasurer or the principal accounting officer of the Issuer, and delivered to the Trustee.
- "<u>Legal Holiday</u>" means a Saturday, a Sunday or a day on which commercial banking institutions are not required to be open in the State of New York.
- "Lien" means, with respect to any asset, any mortgage, lien (statutory or otherwise), pledge, hypothecation, charge, security interest, preference, priority or encumbrance of any kind in respect of such asset, whether or not filed, recorded or otherwise perfected under applicable law, including any conditional sale or other title retention agreement, any lease in the nature thereof, any option or other agreement to sell or give a security interest in and any filing of or agreement to give any financing statement under the Uniform Commercial Code (or equivalent statutes) of any jurisdiction; provided that in no event shall an operating lease be deemed to constitute a Lien.
- "Material Domestic Subsidiary." means, at any date of determination, each of Holdings III's Domestic Subsidiaries other than Holdings V and the Issuer (a) whose total assets at the last day of the most recent test period were equal to or greater than 5% of at such date or (b) whose gross revenues for such test period were equal to or greater than 5% of the consolidated gross revenues of Holdings III and the Restricted Subsidiaries for such period, determined in accordance with GAAP.
- "Material Foreign Subsidiary" means, at any date of determination, each of Holdings III's Foreign Subsidiaries other than Holdings IV (a) whose total assets at the last day of the most recent test period were equal to or greater than 5% of the Total Assets of Holdings III and the Restricted Subsidiaries at such date or (b) whose gross revenues for such test period were equal to or greater than 5% of the consolidated gross revenues of Holdings III and the Restricted Subsidiaries for such period, in each case determined in accordance with GAAP.
 - "Material Real Property" means any real property owned by the Issuer or any Secured Guarantor with a book value in excess of \$25,000,000.
 - "Measurement Date" means September 30, 2010.
 - "Moody's" means Moody's Investors Service, Inc. and any successor to its rating agency business.
- "Mortgage" means collectively, the deeds of trust, trust deeds, hypothecs and mortgages made by the Secured Guarantors in favor or for the benefit of the Collateral Agent on behalf of the Secured Parties under the Collateral Documents relating to the Notes in form and substance reasonably satisfactory to the Collateral Agent and Trustee, and any other mortgages executed and delivered pursuant to this Indenture, as amended, supplemented, modified, extended, renewed or restated from time to time.

"Net Income" means, with respect to any Person, the net income (loss) of such Person, determined in accordance with GAAP and before any reduction in respect of Preferred Stock dividends.

"Net Proceeds" means the aggregate cash proceeds received by Holdings III or any of its Restricted Subsidiaries in respect of any Asset Sale, including any cash received upon the sale or other disposition of any Designated Non-cash Consideration received in any Asset Sale, net of the direct costs relating to such Asset Sale and the sale or disposition of such Designated Non-cash Consideration, including legal, accounting and investment banking fees, and brokerage and sales commissions, any relocation expenses incurred as a result thereof, taxes paid or payable as a result thereof (after taking into account any available tax credits or deductions and any tax sharing arrangements), amounts required to be applied to the repayment of principal, premium, if any, and interest on Senior Indebtedness required (other than required by clause (1) of Section 4.10(b) hereof) to be paid as a result of such transaction and any deduction of appropriate amounts to be provided by Holdings III or any of its Restricted Subsidiaries as a reserve in accordance with GAAP against any liabilities associated with the asset disposed of in such transaction and retained by Holdings III or any of its Restricted Subsidiaries after such sale or other disposition thereof, including pension and other post-employment benefit liabilities and liabilities related to environmental matters or against any indemnification obligations associated with such transaction; provided that net proceeds in an aggregate amount of up to \$500,000,000 (the "Excluded Proceeds") shall not constitute Net Proceeds so long as such net proceeds are, within 60 days following receipt thereof, applied to repay the Existing Senior Subordinated Notes, the Existing Senior Notes or other unsecured Indebtedness in respect of borrowed money, or Refinancing Indebtedness of any of the foregoing (and to correspondingly reduce commitments with respect thereto) (provided that to the extent not so applied within such period, such net proceeds shall constitute Net Proceeds for all purpos

"Non-U.S. Person" means a Person who is not a U.S. Person.

"Notes" means the Initial Notes and more particularly means any Note authenticated and delivered under this Indenture. For all purposes of this Indenture, the term "Notes" shall also include any Additional Notes that may be issued under a supplemental indenture. For purposes of this Indenture, all references to Notes to be issued or authenticated upon transfer, replacement or exchange shall be deemed to refer to Notes.

"Obligations" means any principal, interest (including any interest accruing on or subsequent to the filing of a petition in bankruptcy, reorganization or similar proceeding at the rate provided for in the documentation with respect thereto, whether or not such interest is an allowed claim under applicable state, federal or foreign

law), penalties, fees, indemnifications, reimbursements (including reimbursement obligations with respect to letters of credit and banker's acceptances), damages and other liabilities, and guarantees of payment of such principal, interest, penalties, fees, indemnifications, reimbursements, damages and other liabilities, payable under the documentation governing any Indebtedness.

"Offering Memorandum" means the confidential offering memorandum, dated October 28, 2013, relating to the sale of the Initial Notes.

"Officer" means the Chairman of the Board, the Chief Executive Officer, the President, any Executive Vice President, Senior Vice President or Vice President, the Treasurer or the Secretary of any Person. Unless otherwise indicated, Officer shall refer to an Officer of Holdings III.

"Officer's Certificate" means a certificate signed on behalf of a Person by an Officer of such Person, who must be the principal executive officer, the principal financial officer, the treasurer or the principal accounting officer of such Person, that meets the requirements set forth in this Indenture.

"Old Notes" means the 6.875% Senior Notes due 2011 issued by the Issuer and the 7.125% Notes due 2014 issued by the Issuer.

"Opinion of Counsel" means a written opinion from legal counsel who is acceptable to the Trustee. The counsel may be an employee of or counsel to Holdings III, the Issuer or the Trustee.

"Parent" means Freescale Semiconductor Holdings, Ltd., a Bermuda exempted company limited by shares, and its successors.

"Parent Guarantors" means Parent, Holdings II, Holdings III, Holdings IV and Holdings V.

"Participant" means, with respect to the Depositary a Person who has an account with the Depositary (and, with respect to DTC, shall include Euroclear and Clearstream).

"<u>Permitted Asset Swap</u>" means the substantially concurrent purchase and sale or exchange of Related Business Assets or a combination of Related Business Assets and cash or Cash Equivalents between Holdings III or any of its Restricted Subsidiaries and another Person; <u>provided</u>, that any cash or Cash Equivalents received must be applied in accordance with Section 4.10 hereof.

"<u>Permitted Holders</u>" means each of the Investors and members of management of Holdings III or its direct or indirect parent companies on the Transaction Date who are holders of Equity Interests of Holdings III (or any of its direct or indirect parent companies) and any group (within the meaning of Section 13(d)(3) or Section 14(d)(2) of the Exchange Act or any successor provision) of which any of the

foregoing are members; <u>provided</u>, that, in the case of such group and without giving effect to the existence of such group or any other group, such Investors and members of management, collectively, have beneficial ownership of more than 50% of the total voting power of the Voting Stock of Holdings III or any of its direct or indirect parent companies.

"Permitted Investments" means:

- (1) any Investment in Holdings III or any of its Restricted Subsidiaries;
- (2) any Investment in cash and Cash Equivalents or Investment Grade Securities;
- (3) any Investment by Holdings III or any of its Restricted Subsidiaries in a Person that is engaged in a Similar Business if as a result of such Investment:
 - (a) such Person becomes a Restricted Subsidiary; or
 - (b) such Person, in one transaction or a series of related transactions, is merged, amalgamated or consolidated with or into, or transfers or conveys substantially all of its assets to, or is liquidated into, Holdings III or a Restricted Subsidiary,

and, in each case, any Investment held by such Person; <u>provided</u>, that such Investment was not acquired by such Person in contemplation of such acquisition, merger, consolidation or transfer;

- (4) any Investment in securities or other assets not constituting cash, Cash Equivalents or Investment Grade Securities and received in connection with an Asset Sale made pursuant to the provisions described under Section 4.10 hereof or any other disposition of assets not constituting an Asset Sale;
 - (5) any Investment existing on the Measurement Date;
 - (6) any Investment acquired by Holdings III or any of its Restricted Subsidiaries:
 - (a) in exchange for any other Investment or accounts receivable held by Holdings III or any such Restricted Subsidiary in connection with or as a result of a bankruptcy, workout, reorganization or recapitalization of the issuer of such other Investment or accounts receivable (including any trade creditor or customer); or
 - (b) as a result of a foreclosure by Holdings III or any of its Restricted Subsidiaries with respect to any secured Investment or other transfer of title with respect to any secured Investment in default;

- (7) Hedging Obligations permitted under clause (10) of Section 4.09(b) hereof;
- (8) any Investment in a Similar Business having an aggregate fair market value, taken together with all other Investments made pursuant to this clause (8) after the Measurement Date that are at that time outstanding, not to exceed 3.5% of Total Assets at the time of such Investment (with the fair market value of each Investment being measured at the time made and without giving effect to subsequent changes in value);
- (9) Investments the payment for which consists of Equity Interests (exclusive of Disqualified Stock) of Holdings III, or any of its direct or indirect parent companies; <u>provided</u>, that such Equity Interests will not increase the amount available for Restricted Payments under clause (3) of Section 4.07(a) hereof;
 - (10) guarantees of Indebtedness permitted under Section 4.09 hereof;
- (11) any transaction to the extent it constitutes an Investment that is permitted and made in accordance with the provisions of Section 4.11(b) hereof (except transactions described in clauses (2), (5) and (9) of Section 4.11(b) hereof);
 - (12) Investments consisting of purchases and acquisitions of inventory, supplies, material or equipment;
- (13) additional Investments having an aggregate fair market value, taken together with all other Investments made pursuant to this clause (13) after the Measurement Date that are at that time outstanding (without giving effect to the sale of an Unrestricted Subsidiary to the extent the proceeds of such sale do not consist of cash or marketable securities), not to exceed 4.0% of Total Assets at the time of such Investment (with the fair market value of each Investment being measured at the time made and without giving effect to subsequent changes in value);
- (14) Investments in or relating to a Securitization Subsidiary that, in the good faith determination of Holdings III are necessary or advisable to effect any Qualified Securitization Facility or any repurchase obligation in connection therewith;
 - (15) advances to, or guarantees of Indebtedness of, employees not in excess of \$25.0 million outstanding at any one time, in the aggregate;
- (16) loans and advances to officers, directors and employees for business-related travel expenses, moving expenses and other similar expenses, in each case incurred in the ordinary course of business or consistent with past practices or to fund such Person's purchase of Equity Interests of Holdings III or any direct or indirect parent company thereof;

- (17) advances, loans or extensions of trade credit in the ordinary course of business by Holdings III or any of its Restricted Subsidiaries; and
- (18) Investments in or with respect to the Issuer's jointly funded alliance with respect to the 300 millimeter wafer fabrication in Crolles, France, as in effect on the Issue Date, and any amendment, modification or restructuring thereof, or any successor or replacement alliance or arrangement with respect thereto, or any additional alliance or arrangement with respect to 300 millimeter or larger wafer fabrication (in each case whether or not located in Crolles, France); provided that the aggregate fair market value of any such Investments in any calendar year shall not exceed an amount equal to:
 - (a) \$150.0 million, with unused amounts in any calendar year being carried over to succeeding calendar years subject to a maximum carryover of \$250.0 million; plus
 - (b) the amount of 300 Millimeter Asset Sale Proceeds received during such calendar year, with unused 300 Millimeter Asset Sale Proceeds in any calendar year being carried over to succeeding calendar years without any maximum carryover amount; <u>provided</u> that the aggregate amount of Investments made pursuant to this clause (b) shall not exceed \$500.0 million; minus
 - (c) the amount of 300 Millimeter R&D Expenses incurred during such calendar year that is added back to Consolidated Net Income of Holdings III with respect to such calendar year in arriving at EBITDA of Holdings III with respect to such calendar year (including with respect to such calendar year reducing the amounts available under the immediately preceding clauses (a) and (b), as applicable, for carryovers to succeeding calendar years).

"Permitted Liens" means, with respect to any Person:

(1) pledges or deposits by such Person under workmen's compensation laws, unemployment insurance laws or similar legislation, or good faith deposits in connection with bids, tenders, contracts (other than for the payment of Indebtedness) or leases to which such Person is a party, or deposits to secure public or statutory obligations of such Person or deposits of cash or U.S. government bonds to secure surety or appeal bonds to which such Person is a party, or deposits as security for contested taxes or import duties or for the payment of rent, in each case incurred in the ordinary course of business:

- (2) Liens imposed by law, such as carriers', warehousemen's and mechanics' Liens, in each case for sums not yet overdue for a period of more than 30 days or being contested in good faith by appropriate proceedings or other Liens arising out of judgments or awards against such Person with respect to which such Person shall then be proceeding with an appeal or other proceedings for review if adequate reserves with respect thereto are maintained on the books of such Person in accordance with GAAP;
- (3) Liens for taxes, assessments or other governmental charges not yet overdue for a period of more than 30 days or payable or subject to penalties for nonpayment or which are being contested in good faith by appropriate proceedings diligently conducted, if adequate reserves with respect thereto are maintained on the books of such Person in accordance with GAAP;
- (4) Liens in favor of issuers of performance and surety bonds or bid bonds or with respect to other regulatory requirements or letters of credit issued pursuant to the request of and for the account of such Person in the ordinary course of its business;
- (5) minor survey exceptions, minor encumbrances, easements or reservations of, or rights of others for, licenses, rights-of-way, sewers, electric lines, telegraph and telephone lines and other similar purposes, or zoning or other restrictions as to the use of real properties or Liens incidental, to the conduct of the business of such Person or to the ownership of its properties which were not incurred in connection with Indebtedness and which do not in the aggregate materially adversely affect the value of said properties or materially impair their use in the operation of the business of such Person;
 - (6) Liens securing Credit Facilities Obligations permitted to be incurred pursuant to clause (1) of Section 4.09(b);
- (7) Liens securing Credit Facilities Obligations permitted to be incurred pursuant to Section 4.09; <u>provided</u> that at the time of incurrence, and after giving <u>proforma</u> effect thereto, the Consolidated Secured Debt Ratio would be no greater than 3.25 to 1.00;
- (8) Liens securing the Notes, any Guarantee of the Notes and other Obligations under the Notes and this Indenture (other than any Additional Notes, any Guarantees of any Additional Notes or other Obligations under any Additional Notes);
- (9) Liens securing the Existing Secured Notes, any Guarantee of the Existing Secured Notes and other obligations under the Existing Secured Notes, and the indenture governing the Existing Secured Notes (other than any Existing Secured Notes issued after the Issue Date, any Guarantees of any Existing Secured Notes issued after the Issue Date or other Obligations under any Existing Secured Notes issued after the Issue Date);

- (10) Liens securing Indebtedness permitted to be incurred pursuant to clause (4) or (12)(b) of Section 4.09(b) hereof;
- (11) Liens existing on the Issue Date (including the Liens granted pursuant to Section 7.06 hereof);
- (12) Liens on property or shares of stock or other assets of a Person at the time such Person becomes a Subsidiary; <u>provided</u>, that such Liens are not created or incurred in connection with, or in contemplation of, such other Person becoming such a Subsidiary; <u>provided</u>, <u>further</u>, that such Liens may not extend to any other property or other assets owned by Holdings III or any of its Restricted Subsidiaries;
- (13) Liens on property or other assets at the time Holdings III or a Restricted Subsidiary acquired the property or such other assets, including any acquisition by means of a merger, amalgamation or consolidation with or into Holdings III or any of its Restricted Subsidiaries; <u>provided</u>, that such Liens are not created or incurred in connection with, or in contemplation of, such acquisition; <u>provided</u>, <u>further</u>, that the Liens may not extend to any other property owned by Holdings III or any of its Restricted Subsidiaries;
- (14) Liens securing Indebtedness or other obligations of a Restricted Subsidiary owing to Holdings III or another Restricted Subsidiary permitted to be incurred in accordance with the Section 4.09;
- (15) Liens securing Hedging Obligations so long as related Indebtedness is, and is permitted to be under this Indenture, secured by a Lien on the same property securing such Hedging Obligations;
- (16) Liens on specific items of inventory or other goods and proceeds of any Person securing such Person's obligations in respect of bankers' acceptances issued or created for the account of such Person to facilitate the purchase, shipment or storage of such inventory or other goods;
- (17) leases, subleases, licenses or sublicenses granted to others in the ordinary course of business which do not materially interfere with the ordinary conduct of the business of Holdings III or any of its Restricted Subsidiaries and do not secure any Indebtedness;
- (18) Liens arising from Uniform Commercial Code financing statement filings regarding operating leases entered into by Holdings III and its Restricted Subsidiaries in the ordinary course of business;

- (19) Liens in favor of Holdings III, the Issuer or any Subsidiary Guarantor;
- (20) Liens on equipment of Holdings III or any of its Restricted Subsidiaries granted in the ordinary course of business to Holdings III's clients;
- (21) Liens on accounts receivable, Securitization Assets and related assets incurred in connection with a Qualified Securitization Facility;
- (22) Liens to secure any refinancing, refunding, extension, renewal or replacement (or successive refinancing, refunding, extensions, renewals or replacements) as a whole, or in part, of any Indebtedness secured by any Lien referred to in the foregoing clauses (10), (11), (12) and (13); provided, that (a) such new Lien shall be limited to all or part of the same property that secured the original Lien (plus improvements on such property), and (b) the Indebtedness secured by such Lien at such time is not increased to any amount greater than the sum of (i) the outstanding principal amount or, if greater, committed amount of the Indebtedness described under clauses (10), (11), (12) and (13) at the time the original Lien became a Permitted Lien under this Indenture, and (ii) an amount necessary to pay any fees and expenses, including premiums, related to such refinancing, refunding, extension, renewal or replacement;
 - (23) deposits made in the ordinary course of business to secure liability to insurance carriers;
- (24) other Liens securing obligations incurred in the ordinary course of business which obligations do not exceed \$65.0 million at any one time outstanding;
- (25) Liens securing judgments for the payment of money not constituting an Event of Default under clause (5) under Section 6.01 hereof so long as such Liens are adequately bonded and any appropriate legal proceedings that may have been duly initiated for the review of such judgment have not been finally terminated or the period within which such proceedings may be initiated has not expired;
- (26) Liens in favor of customs and revenue authorities arising as a matter of law to secure payment of customs duties in connection with the importation of goods in the ordinary course of business;
- (27) Liens (i) of a collection bank arising under Section 4-210 of the Uniform Commercial Code on items in the course of collection, (ii) attaching to commodity trading accounts or other commodity brokerage accounts incurred in the ordinary course of business, and (iii) in favor of banking institutions arising as a matter of law encumbering deposits (including the right of set-off) and which are within the general parameters customary in the banking industry;

- (28) Liens deemed to exist in connection with Investments in repurchase agreements permitted under Section 4.09 hereof; <u>provided</u> that such Liens do not extend to any assets other than those that are the subject of such repurchase agreement;
- (29) Liens encumbering reasonable customary initial deposits and margin deposits and similar Liens attaching to commodity trading accounts or other brokerage accounts incurred in the ordinary course of business and not for speculative purposes;
- (30) Liens that are contractual rights of set-off (i) relating to the establishment of depository relations with banks not given in connection with the issuance of Indebtedness, (ii) relating to pooled deposit or sweep accounts of Holdings III or any of its Restricted Subsidiaries to permit satisfaction of overdraft or similar obligations incurred in the ordinary course of business of Holdings III and its Restricted Subsidiaries or (iii) relating to purchase orders and other agreements entered into with customers of Holdings III or any of its Restricted Subsidiaries in the ordinary course of business;
- (31) Liens securing obligations owed by Holdings III or any Restricted Subsidiary to any lender under the Senior Credit Facilities or any Affiliate of such a lender in respect of any overdraft and related liabilities arising from treasury, depository and cash management services or any automated clearing house transfers of funds;
- (32) Liens securing Indebtedness the proceeds of which are used to develop or construct new facilities (or any improvements to existing facilities) or equipment (or any improvements to existing equipment) designed primarily for the purpose of air or water pollutions control; <u>provided</u> that such Indebtedness is permitted to be incurred by the terms of this Indenture and such Liens do not extend to any assets of Holdings III or its Restricted Subsidiaries other than the assets acquired or improved with the proceeds of the Indebtedness secured by such Lien; and
- (33) any encumbrance or restriction (including put and call arrangements) with respect to capital stock of any joint venture or similar arrangement pursuant to any joint venture or similar agreement.

For purposes of this definition, the term "Indebtedness" shall be deemed to include interest on such Indebtedness.

"<u>Person</u>" means any individual, corporation, limited liability company, partnership, joint venture, association, joint stock company, trust, unincorporated organization, government or any agency or political subdivision thereof or any other entity.

- "Preferred Stock" means any Equity Interest with preferential rights of payment of dividends or upon liquidation, dissolution, or winding up.
- "Private Placement Legend" means the legend set forth in Section 2.06(f)(i) hereof to be placed on all Notes issued under this Indenture, except where otherwise permitted by the provisions of this Indenture.
 - "QIB" means a "qualified institutional buyer" as defined in Rule 144A.
- "Qualified Proceeds" means the fair market value of assets that are used or useful in, or Capital Stock of any Person engaged in, a Similar Business.
- "Qualified Securitization Facility" means any Securitization Facility (a) constituting a securitization financing facility that meets the following conditions: (1) the board of directors of Holdings III shall have determined in good faith that such Securitization Facility (including financing terms, covenants, termination events and other provisions) is in the aggregate economically fair and reasonable to Holdings III and the applicable Securitization Subsidiary, (2) all sales and/or contributions of Securitization Assets and related assets to the applicable Securitization Subsidiary are made at fair market value (as determined in good faith by Holdings III) and (3) the financing terms, covenants, termination events and other provisions thereof shall be market terms (as determined in good faith by Holdings III) or (b) constituting a receivables financing facility.
- "Rating Agencies" means Moody's and S&P or if Moody's or S&P or both shall not make a rating on the Notes publicly available, a nationally recognized statistical rating agency or agencies, as the case may be, selected by the Issuer which shall be substituted for Moody's or S&P or both, as the case may be.
- "Record Date" for the interest payable on any applicable Interest Payment Date means the May 1 or November 1 (whether or not a Business Day) immediately preceding such Interest Payment Date.
 - "Regulation S" means Regulation S promulgated under the Securities Act.
 - "Regulation S Global Note" means a Regulation S Temporary Global Note or Regulation S Permanent Global Note, as applicable.
- "Regulation S Permanent Global Note" means a permanent Global Note in the form of Exhibit A hereto, bearing the Global Note Legend and the Private Placement Legend and deposited with or on behalf of and registered in the name of the Depositary or its nominee, issued in a denomination equal to the outstanding principal amount of the Regulation S Temporary Global Note of the applicable series upon expiration of the Restricted Period.
- "Regulation S Temporary Global Note" means a temporary Global Note in the form of Exhibit A hereto, bearing the Global Note Legend, the Private Placement

Legend and the Regulation S Temporary Global Note Legend and deposited with or on behalf of and registered in the name of the Depositary or its nominee, issued in a denomination equal to the outstanding principal amount of the Notes of the applicable series initially sold in reliance on Rule 903.

"Regulation S Temporary Global Note Legend" means the legend set forth in Section 2.06(f)(iii) hereof.

"Related Business Assets" means assets (other than cash or Cash Equivalents) used or useful in a Similar Business, <u>provided</u> that any assets received by Holdings III or a Restricted Subsidiary in exchange for assets transferred by Holdings III or a Restricted Subsidiary shall not be deemed to be Related Business Assets if they consist of securities of a Person, unless upon receipt of the securities of such Person, such Person would become a Restricted Subsidiary.

"Responsible Officer" means, when used with respect to the Trustee, any officer within the corporate trust department of the Trustee, including any vice president, assistant vice president, assistant secretary, assistant treasurer, trust officer or any other officer of the Trustee who customarily performs functions similar to those performed by the Persons who at the time shall be such officers, respectively, or to whom any corporate trust matter is referred because of such Person's knowledge of and familiarity with the particular subject and who shall have direct responsibility for the administration of this Indenture.

"Restricted Definitive Note" means a Definitive Note bearing, or that is required to bear, the Private Placement Legend.

"Restricted Global Note" means a Global Note bearing, or that is required to bear, the Private Placement Legend.

"Restricted Investment" means an Investment other than a Permitted Investment.

"Restricted Parent Guarantor" means Holdings III, Holdings IV and Holdings V.

"Restricted Period" means the 40-day distribution compliance period as defined in Regulation S.

"Restricted Subsidiary" means, at any time, Holdings IV, Holdings V, the Issuer and any other direct or indirect Subsidiary of Holdings III (including any Foreign Subsidiary) that is not then an Unrestricted Subsidiary; provided, that upon an Unrestricted Subsidiary ceasing to be an Unrestricted Subsidiary, such Subsidiary shall be included in the definition of "Restricted Subsidiary" if it is then a Subsidiary of Holdings III.

"Rule 144" means Rule 144 promulgated under the Securities Act.

- "Rule 144A" means Rule 144A promulgated under the Securities Act.
- "Rule 903" means Rule 903 promulgated under the Securities Act.
- "Rule 904" means Rule 904 promulgated under the Securities Act.
- "S&P" means Standard & Poor's Rating Services, and any successor to its rating agency business.
- "Sale and Lease-Back Transaction" means any arrangement providing for the leasing by Holdings III or any of its Restricted Subsidiaries of any real or tangible personal property, which property has been or is to be sold or transferred by Holdings III or such Restricted Subsidiary to a third Person in contemplation of such leasing.
 - "SEC" means the U.S. Securities and Exchange Commission.
- "Secured Guarantors" means the Restricted Parent Guarantors, the Domestic Subsidiary Guarantors and the Foreign Subsidiary Guarantors providing secured Guarantees.
 - "Secured Indebtedness" means any Indebtedness of Holdings III or any of its Restricted Subsidiaries secured by a Lien.
 - "Secured Parties" means the Senior Credit Agreement Secured Parties and the Additional First Lien Debt Parties.
 - "Securities Act" means the Securities Act of 1933, as amended, and the rules and regulations of the SEC promulgated thereunder.
- "Securitization Assets" means the accounts receivable, royalty or other revenue streams and other rights to payment related to the Specified Contract Rights subject to a Qualified Securitization Facility that is a securitization financing facility (and not a receivables financing facility) and the proceeds thereof.
- "Securitization Facility" means any of one or more receivables or securitization financing facilities as amended, supplemented, modified, extended, renewed, restated or refunded from time to time, the Obligations of which are non-recourse (except for customary representations, warranties, covenants and indemnities made in connection with such facilities) to Holdings III or any of its Restricted Subsidiaries (other than a Securitization Subsidiary) pursuant to which Holdings III or any of its Restricted Subsidiaries sells or grants a security interest in its accounts receivable or Securitization Assets or assets related thereto to either (a) a Person that is not a Restricted Subsidiary or (b) a Securitization Subsidiary that in turn sells its accounts receivable to a Person that is not a Restricted Subsidiary.
- "Securitization Fees" means distributions or payments made directly or by means of discounts with respect to any participation interest issued or sold in connection with, and other fees paid to a Person that is not a Securitization Subsidiary in connection with, any Qualified Securitization Financing.

- "Securitization Subsidiary" means any Subsidiary formed for the purpose of, and that solely engages only in one or more Qualified Securitization Facilities and other activities reasonably related thereto.
- "Security Agreement" means the security agreement dated as of November 1, 2013, among the Issuer, Holdings IV, SigmaTel, the subsidiaries of Holdings III from time to time party thereto and Citibank, N.A., as Collateral Agent, as amended, supplemented, modified, extended, renewed or restated from time to time.
- "Senior Credit Agreement Collateral Agent" means Citibank, N.A., in its capacity as the collateral agent for the Senior Credit Agreement Secured Parties under the Senior Credit Agreement Collateral Documents, and any successor thereof.
- "Senior Credit Agreement Collateral Documents" means the security agreement, the intellectual property security agreement, the mortgages, the security agreement supplements and each other agreement, instrument or other document entered into in favor of the administrative agent under the Senior Credit Facilities Documents, the Senior Credit Agreement Collateral Agent or any of the other Senior Credit Agreement Secured Parties for purposes of securing the Senior Credit Agreement Obligations.
 - "Senior Credit Agreement Obligations" has the meaning assigned to the term "Obligations" in the Senior Credit Facilities.
 - "Senior Credit Agreement Secured Parties" has the meaning assigned to the term "Secured Parties" in the Senior Credit Facilities.
- "Senior Credit Facilities" means the Credit Facilities entered into as of the Measurement Date by and among the Issuer, Holdings III, the lenders party thereto in their capacities as lenders thereunder and Citibank, N.A., as Administrative Agent, including any guarantees, collateral documents, instruments and agreements executed in connection therewith, and any amendments, supplements, modifications, extensions, renewals, restatements, refundings or refinancings thereof and any indentures or credit facilities or commercial paper facilities with banks or other institutional lenders or investors that replace, refund or refinance any part of the loans, notes, other credit facilities or commitments thereunder, including any such replacement, refunding or refinancing facility or indenture that increases the amount borrowable thereunder or alters the maturity thereof (provided that such increase in borrowings is permitted under Section 4.09 hereof).

"Senior Credit Facilities Documents" means the Senior Credit Facilities, any promissory notes issued to any Lender (as defined in the Senior Credit Facilities) pursuant to the Senior Credit Facilities, the Senior Credit Agreement Collateral Documents and each other Loan Document (as defined in the Senior Credit Facilities), as the same may be amended, restated, supplemented or otherwise modified from time to time.

"Senior Indebtedness" means:

- (1) all Indebtedness of the Issuer or any Guarantor outstanding under the Senior Credit Facilities, the Existing Secured Notes and the related Guarantees, the Notes and related Guarantees and the Existing Senior Notes and related Guarantees (including interest accruing on or after the filing of any petition in bankruptcy or similar proceeding or for reorganization of the Issuer or any Guarantor (at the rate provided for in the documentation with respect thereto, regardless of whether or not a claim for post-filing interest is allowed in such proceedings)), and any and all other fees, expense reimbursement obligations, indemnification amounts, penalties, and other amounts (whether existing on the Issue Date or thereafter created or incurred) and all obligations of the Issuer or any Guarantor to reimburse any bank or other Person in respect of amounts paid under letters of credit, acceptances or other similar instruments;
- (2) all Hedging Obligations (and guarantees thereof) owing to a Lender (as defined in the Senior Credit Facilities) or any Affiliate of such Lender (or any Person that was a Lender or an Affiliate of such Lender at the time the applicable agreement giving rise to such Hedging Obligation was entered into), <u>provided</u> that such Hedging Obligations are permitted to be incurred under the terms of this Indenture;
- (3) any other Indebtedness of the Issuer or any Guarantor permitted to be incurred under the terms of this Indenture, unless the instrument under which such Indebtedness is incurred expressly provides that it is on a parity with or subordinated in right of payment to the Existing Senior Subordinated Notes or any related Guarantee; and
 - (4) all Obligations with respect to the items listed in the preceding clauses (1), (2) and (3);

provided, that Senior Indebtedness shall not include:

- (a) any obligation of such Person to Holdings III or any of its Subsidiaries;
- (b) any liability for federal, state, local or other taxes owed or owing by such Person;
- (c) any accounts payable or other liability to trade creditors arising in the ordinary course of business;

- (d) any Indebtedness or other Obligation of such Person which is subordinate or junior in any respect to any other Indebtedness or other Obligation of such Person; or
 - (e) that portion of any Indebtedness which at the time of incurrence is incurred in violation of this Indenture.
- "SigmaTel" means SigmaTel, LLC, a Delaware limited liability company.
- "<u>Significant Subsidiary</u>" means any Restricted Subsidiary that would be a "significant subsidiary" as defined in Article 1, Rule 1-02 of Regulation S-X, promulgated pursuant to the Securities Act, as such regulation is in effect on the Issue Date.
- "Similar Business" means any business conducted or proposed to be conducted by Holdings III and its Restricted Subsidiaries on the Issue Date and any reasonable extension thereof or any business that is similar, reasonably related, incidental or ancillary thereto.
- "Specified Contract Rights" means certain intellectual property licenses, agreements or other contracts giving rise to not more than \$100 million of annual accounts receivable, royalty or other intellectual property revenue streams or other rights to payment.
- "<u>Specified Foreign Subsidiaries</u>" means each Material Foreign Subsidiary that is not a direct or indirect Subsidiary of Holdings V, each Transferred Foreign Subsidiary and, after its formation, Foreign Acquisition Co.
 - "Subordinated Indebtedness" means, with respect to the Notes,
 - (1) any Indebtedness of the Issuer which is by its terms subordinated in right of payment to the Notes, and
 - (2) any Indebtedness of any Guarantor which is by its terms subordinated in right of payment to the Guarantee of such entity of the Notes.
 - "Subsidiary" means, with respect to any Person:
 - (1) any corporation, association, or other business entity (other than a partnership, joint venture, limited liability company or similar entity) of which more than 50% of the total voting power of shares of Capital Stock entitled (without regard to the occurrence of any contingency) to vote in the election of directors, managers or trustees thereof is at the time of determination owned or controlled, directly or indirectly, by such Person or one or more of the other Subsidiaries of that Person or a combination thereof or is consolidated under GAAP with such Person at such time; and

- (2) any partnership, joint venture, limited liability company or similar entity of which
- (x) more than 50% of the capital accounts, distribution rights, total equity and voting interests or general or limited partnership interests, as applicable, are owned or controlled, directly or indirectly, by such Person or one or more of the other Subsidiaries of that Person or a combination thereof whether in the form of membership, general, special or limited partnership or otherwise, and
 - (y) such Person or any Restricted Subsidiary of such Person is a controlling general partner or otherwise controls such entity.

"Subsidiary Guarantor" means each Guarantor other than the Parent Guarantors.

"<u>Total Assets</u>" means the total assets of Holdings III and its Restricted Subsidiaries, determined on a consolidated basis in accordance with GAAP, as shown on the most recent balance sheet of Holdings III or such other Person as may be expressly stated.

"Transaction" means the transactions contemplated by the Transaction Agreement, the tender offer and consent solicitation relating to the Old Notes, the issuance of Existing Senior Notes and the Existing Senior Subordinated Notes and borrowings under the Senior Credit Facilities as in effect on the Transaction Date.

"<u>Transaction Agreement</u>" means the Agreement and Plan of Merger, dated as of September 15, 2006 by and among the Issuer, Firestone Acquisition Corporation and Firestone Holdings LLC, as in effect on the Transaction Date.

"Transaction Date" means December 1, 2006.

"Transferred Foreign Subsidiary" has the meaning specified in the definition of "Foreign Reorganization."

"Treasury Rate" means, as of any Redemption Date, the yield to maturity as of such Redemption Date of United States Treasury securities with a constant maturity (as compiled and published in the most recent Federal Reserve Statistical Release H.15 (519) that has become publicly available at least two Business Days prior to the Redemption Date (or, if such Statistical Release is no longer published, any publicly available source of similar market data)) most nearly equal to the period from the Redemption Date to November 15, 2016; <u>provided</u>, that if the period from the Redemption Date to such date is less than one year, the weekly average yield on actually traded United States Treasury securities adjusted to a constant maturity of one year will be used.

"<u>Trustee</u>" means Wells Fargo Bank, National Association, as trustee, until a successor replaces it in accordance with the applicable provisions of this Indenture and thereafter means the successor serving hereunder.

"Uniform Commercial Code" means the New York Uniform Commercial Code as in effect from time to time.

"Unrestricted Definitive Note" means one or more Definitive Notes that do not bear and are not required to bear the Private Placement Legend.

"<u>Unrestricted Global Note</u>" means a permanent Global Note, substantially in the form of <u>Exhibit A</u> attached hereto that bears the Global Note Legend and that has the "Schedule of Exchanges of Interests in the Global Note" attached thereto, and that is deposited with or on behalf of and registered in the name of the Depositary, representing Notes that do not bear the Private Placement Legend.

"Unrestricted Subsidiary" means:

- (1) any Subsidiary of Holdings III which at the time of determination is an Unrestricted Subsidiary (as designated by Holdings III, as provided below); and
 - (2) any Subsidiary of an Unrestricted Subsidiary.

Holdings III may designate any Subsidiary of Holdings III (including any existing Subsidiary and any newly acquired or newly formed Subsidiary but excluding the Issuer and any Subsidiary of Holdings III as to which the Issuer is a Subsidiary) to be an Unrestricted Subsidiary unless such Subsidiary or any of its Subsidiaries owns any Equity Interests or Indebtedness of, or owns or holds any Lien on, any property of, Holdings III or any Subsidiary of Holdings III (other than solely any Subsidiary of the Subsidiary to be so designated); provided that

- (1) any Unrestricted Subsidiary must be an entity of which the Equity Interests entitled to cast at least a majority of the votes that may be cast by all Equity Interests having ordinary voting power for the election of directors or Persons performing a similar function are owned, directly or indirectly, by Holdings III;
 - (2) such designation complies with Section 4.07 hereof; and
 - (3) each of:
 - (a) the Subsidiary to be so designated; and
 - (b) its Subsidiaries

has not at the time of designation, and does not thereafter, create, incur, issue, assume, guarantee or otherwise become directly or indirectly liable with respect to any Indebtedness pursuant to which the lender has recourse to any of the assets of Holdings III or any Restricted Subsidiary.

Holdings III may designate any Unrestricted Subsidiary to be a Restricted Subsidiary; <u>provided</u> that, immediately after giving effect to such designation, no Default shall have occurred and be continuing and either:

- (1) Holdings III could incur at least \$1.00 of additional Indebtedness pursuant to the Fixed Charge Coverage Test described in Section 4.09(a) hereof: or
- (2) the Fixed Charge Coverage Ratio for Holdings III and its Restricted Subsidiaries would be equal to or greater than such ratio for Holdings III and its Restricted Subsidiaries immediately prior to such designation, in each case on a <u>pro forma</u> basis taking into account such designation.

Any such designation by Holdings III shall be notified by Holdings III to the Trustee by promptly filing with the Trustee a copy of the resolution of the board of directors of Holdings III or any committee thereof giving effect to such designation and an Officer's Certificate certifying that such designation complied with the foregoing provisions.

"<u>U.S. Dollar Equivalent</u>" means, with respect to any monetary amount in a currency other than U.S. dollars, at any time for the determination thereof, the amount of U.S. dollars obtained by converting such foreign currency involved in such computation into U.S. dollars at the spot rate for the purchase of U.S. dollars with the applicable foreign currency as quoted by Reuters at approximately 10:00 A.M. (New York City time) on such date of determination (or if no such quote is available on such date, on the immediately preceding Business Day for which such a quote is available).

"U.S. Person" means a U.S. person as defined in Rule 902(k) under the Securities Act.

"<u>Voting Stock</u>" of any Person as of any date means the Capital Stock of such Person that is at the time entitled to vote in the election of the board of directors of such Person.

"<u>Weighted Average Life to Maturity</u>" means, when applied to any Indebtedness, Disqualified Stock or Preferred Stock, as the case may be, at any date, the quotient obtained by dividing:

(1) the sum of the products of the number of years from the date of determination to the date of each successive scheduled principal payment of such Indebtedness or redemption or similar payment with respect to such Disqualified Stock or Preferred Stock multiplied by the amount of such payment; by

(2) the sum of all such payments.

"Wholly-Owned Subsidiary" means, with respect to a Subsidiary of any Person, a Subsidiary of such Person, 100% of the outstanding Equity Interests of which (other than directors' qualifying shares) shall at the time be owned by such Person or by one or more Wholly-Owned Subsidiaries of such Person.

SECTION 1.02. Other Definitions.

| | Defined |
|----------------------------------|---------------|
| Term | in Section |
| "Acceptable Commitment" | 4.10 |
| "Affiliate Transaction" | 4.11 |
| "Asset Sale Offer" | 4.10 |
| "Authentication Order" | 2.02 |
| "Change of Control Offer" | 4.14 |
| "Change of Control Payment" | 4.14 |
| "Change of Control Payment Date" | 4.14 |
| "Covenant Defeasance" | 8.03 |
| "Covenant Suspension Event" | 4.16 |
| "DTC" | 2.03 |
| "Event of Default" | 6.01 |
| "Excess Proceeds" | 4.10 |
| "Excluded Assets" | 11.02 |
| "Fixed Charge Coverage Test" | 4.09 |
| "Foreign Payor" | 4.05 |
| "incur" | 4.09 |
| "Initial Lien" | 4.12 |
| "Legal Defeasance" | 8.02 |
| "Note Register" | 2.03 |
| "Offer Amount" | 3.09 |
| "Offer Period" | 3.09 |
| "Paying Agent" | 2.03 |
| "Purchase Date" | 3.09 |
| "Redemption Date" | 3.07 |
| "Refinancing Indebtedness" | 4.09 |
| "Refunding Capital Stock" | 4.07 |
| "Registrar" | 2.03 |
| "Relevant Taxing Jurisdiction" | 4.05 |
| "Restricted Payments" | 4.07 |
| "Reversion Date" | 4.16 |
| "Second Commitment" | 4.10 |
| "Successor Company" | 5.01 |
| "Successor Guarantor" | 5.01 |

| | Defined |
|--------------------------|---------|
| | in |
| <u>Term</u> | Section |
| "Successor Person" | 5.01 |
| "Suspended Covenants" | 4.16 |
| "Suspension Date" | 4.16 |
| "Suspension Period" | 4.16 |
| "Taxes" | 4.05 |
| "Treasury Capital Stock" | 4.07 |

SECTION 1.03. Rules of Construction. Unless the context otherwise requires:

- (a) a term has the meaning assigned to it;
- (b) an accounting term not otherwise defined has the meaning assigned to it in accordance with GAAP;
- (c) "or" is not exclusive;
- (d) "including" means including without limitation;
- (e) words in the singular include the plural, and in the plural include the singular;
- (f) "will" shall be interpreted to express a command;
- (g) provisions apply to successive events and transactions;
- (h) references to sections of, or rules under, the Securities Act shall be deemed to include substitute, replacement or successor sections or rules adopted by the SEC from time to time;
- (i) unless the context otherwise requires, any reference to an "Article," "Section" or "clause" refers to an Article, Section or clause, as the case may be, of this Indenture; and
- (j) the words "herein," "hereof" and "hereunder" and other words of similar import refer to this Indenture as a whole and not any particular Article, Section, clause or other subdivision.

SECTION 1.04. Acts of Holders.

(a) Any request, demand, authorization, direction, notice, consent, waiver or other action provided by this Indenture to be given or taken by Holders may be embodied in and evidenced by one or more instruments of substantially similar tenor

signed by such Holders in person or by an agent duly appointed in writing. Except as herein otherwise expressly provided, such action shall become effective when such instrument or instruments or record or both are delivered to the Trustee and, where it is hereby expressly required, to the Issuer. Proof of execution of any such instrument or of a writing appointing any such agent, or the holding by any Person of a Note, shall be sufficient for any purpose of this Indenture and (subject to Section 7.01) conclusive in favor of the Trustee and the Issuer, if made in the manner provided in this Section 1.04.

- (b) The fact and date of the execution by any Person of any such instrument or writing may be proved by the affidavit of a witness of such execution or by the certificate of any notary public or other officer authorized by law to take acknowledgments of deeds, certifying that the individual signing such instrument or writing acknowledged to him the execution thereof. Where such execution is by or on behalf of any legal entity other than an individual, such certificate or affidavit shall also constitute proof of the authority of the Person executing the same. The fact and date of the execution of any such instrument or writing, or the authority of the Person executing the same, may also be proved in any other manner that the Trustee deems sufficient.
 - (c) The ownership of Notes shall be proved by the Note Register.
- (d) Any request, demand, authorization, direction, notice, consent, waiver or other action by the Holder of any Note shall bind every future Holder of the same Note and the Holder of every Note issued upon the registration of transfer thereof or in exchange therefor or in lieu thereof, in respect of any action taken, suffered or omitted by the Trustee, the Collateral Agent or the Issuer in reliance thereon, whether or not notation of such action is made upon such Note.
- (e) The Issuer may set a record date for purposes of determining the identity of Holders entitled to give any request, demand, authorization, direction, notice, consent, waiver or take any other act, or to vote or consent to any action by vote or consent authorized or permitted to be given or taken by Holders.
- (f) Without limiting the foregoing, a Holder entitled to take any action hereunder with regard to any particular Note may do so with regard to all or any part of the principal amount of such Note or by one or more duly appointed agents, each of which may do so pursuant to such appointment with regard to all or any part of such principal amount. Any notice given or action taken by a Holder or its agents with regard to different parts of such principal amount pursuant to this paragraph shall have the same effect as if given or taken by separate Holders of each such different part.
- (g) Without limiting the generality of the foregoing, a Holder, including DTC, may make, give or take, by a proxy or proxies duly appointed in writing, any request, demand, authorization, direction, notice, consent, waiver or other action provided in this Indenture to be made, given or taken by Holders, and DTC may provide its proxy to the beneficial owners of interests in any such Global Note through such depositary's standing instructions and customary practices.

(h) The Issuer may fix a record date for the purpose of determining the Persons who are beneficial owners of interests in any Global Note held by DTC entitled under the procedures of such depositary to make, give or take, by a proxy or proxies duly appointed in writing, any request, demand, authorization, direction, notice, consent, waiver or other action provided in this Indenture to be made, given or taken by Holders. If such a record date is fixed, the Holders on such record date or their duly appointed proxy or proxies, and only such Persons, shall be entitled to make, give or take such request, demand, authorization, direction, notice, consent, waiver or other action, whether or not such Holders remain Holders after such record date. No such request, demand, authorization, direction, notice, consent, waiver or other action shall be valid or effective if made, given or taken more than 90 days after such record date.

ARTICLE II

THE NOTES

SECTION 2.01. Form and Dating; Terms.

- (a) <u>General</u>. The Notes and the Trustee's certificate of authentication shall be substantially in the form of <u>Exhibit A</u> hereto. The Notes may have notations, legends or endorsements required by law, stock exchange rules or usage. Each Note shall be dated the date of its authentication. The Notes shall be in minimum denominations of \$2,000 and integral multiples of \$1,000 in excess thereof.
- (b) <u>Global Notes</u>. Notes issued in global form shall be substantially in the form of <u>Exhibit A</u> hereto (including the Global Note Legend thereon and the "Schedule of Exchanges of Interests in the Global Note" attached thereto). Notes issued in definitive form shall be substantially in the form of <u>Exhibit A</u> hereto (but without the Global Note Legend thereon and without the "Schedule of Exchanges of Interests in the Global Note" attached thereto). Each Global Note shall represent such of the outstanding Notes as shall be specified in the "Schedule of Exchanges of Interests in the Global Note" attached thereto and each shall provide that it shall represent up to the aggregate principal amount of Notes from time to time endorsed thereon and that the aggregate principal amount of outstanding Notes represented thereby may from time to time be reduced or increased, as applicable, to reflect exchanges and redemptions. Any endorsement of a Global Note to reflect the amount of any increase or decrease in the aggregate principal amount of outstanding Notes represented thereby shall be made by the Trustee or the Custodian, at the direction of the Trustee, in accordance with instructions given by the Holder thereof as required by Section 2.06 hereof.
- (c) <u>Temporary Global Notes</u>. Notes offered and sold in reliance on Regulation S shall be issued initially in the form of the Regulation S Temporary Global Note, which shall be deposited on behalf of the purchasers of the Notes represented thereby with the Custodian and registered in the name of the Depositary or the nominee of the Depositary for the accounts of designated agents holding on behalf of Euroclear or Clearstream, duly executed by the Issuer and authenticated by the Trustee as hereinafter provided. The Restricted Period shall be terminated upon the receipt by the Trustee of:

(i) a written certificate from the Depositary, together with copies of certificates from Euroclear and Clearstream certifying that they have received certification of non-United States beneficial ownership of 100% of the aggregate principal amount of each Regulation S Temporary Global Note (except to the extent of any beneficial owners thereof who acquired an interest therein during the Restricted Period pursuant to another exemption from registration under the Securities Act and who shall take delivery of a beneficial ownership interest in a 144A Global Note bearing a Private Placement Legend, all as contemplated by Section 2.06(b) hereof); and

(ii) an Officer's Certificate from the Issuer.

Following the termination of the Restricted Period, beneficial interests in each Regulation S Temporary Global Note shall be exchanged for beneficial interests in a Regulation S Permanent Global Note of the same series pursuant to the Applicable Procedures. Simultaneously with the authentication of the corresponding Regulation S Permanent Global Note, the Trustee shall cancel the corresponding Regulation S Temporary Global Note. The aggregate principal amount of a Regulation S Temporary Global Note and a Regulation S Permanent Global Note may from time to time be increased or decreased by adjustments made on the records of the Trustee and the Depositary or its nominee, as the case may be, in connection with transfers of interest as hereinafter provided.

(d) <u>Terms</u>. The aggregate principal amount of Notes that may be authenticated and delivered under this Indenture is unlimited.

The terms and provisions contained in the Notes shall constitute, and are hereby expressly made, a part of this Indenture and the Issuer, the Guarantors and the Trustee, by their execution and delivery of this Indenture, expressly agree to such terms and provisions and to be bound thereby. However, to the extent any provision of any Note conflicts with the express provisions of this Indenture, the provisions of this Indenture shall govern and be controlling.

The Notes shall be subject to repurchase by the Issuer pursuant to an Asset Sale Offer as provided in Section 4.10 hereof or a Change of Control Offer as provided in Section 4.14 hereof. The Notes shall not be redeemable, other than as provided in Article 3 hereof.

Additional Notes ranking <u>pari passu</u> with the Initial Notes may be created and issued from time to time by the Issuer without notice to or consent of the Holders and shall be consolidated with and form a single class with the Initial Notes and shall have the same terms as to status, redemption or otherwise as the Initial Notes; <u>provided</u> that the Issuer's ability to issue Additional Notes shall be subject to the Issuer's compliance with Section 4.09 hereof. Any Additional Notes shall be issued with the benefit of an indenture supplemental to this Indenture.

SECTION 2.02. Execution and Authentication. At least one Officer of the Issuer shall execute the Notes on behalf of the Issuer by manual or facsimile signature.

If an Officer of the Issuer whose signature is on a Note no longer holds that office at the time the Trustee authenticates the Note, the Note shall nevertheless be valid.

A Note shall not be entitled to any benefit under this Indenture or be valid or obligatory for any purpose until authenticated substantially in the form of Exhibit A attached hereto by the manual signature of the Trustee. The signature shall be conclusive evidence that the Note has been duly authenticated and delivered under this Indenture.

On the Issue Date, the Trustee shall, upon receipt of an Issuer Order (an "<u>Authentication Order</u>"), authenticate and deliver the Initial Notes. In addition, at any time, from time to time, the Trustee shall upon an Authentication Order authenticate and deliver any Additional Notes for an aggregate principal amount specified in such Authentication Order for such Additional Notes issued or increased hereunder.

The Trustee may appoint an authenticating agent acceptable to the Issuer to authenticate Notes. An authenticating agent may authenticate Notes whenever the Trustee may do so. Each reference in this Indenture to authentication by the Trustee includes authentication by such agent. An authenticating agent has the same rights as an Agent to deal with Holders or an Affiliate of the Issuer.

SECTION 2.03. <u>Registrar and Paying Agent.</u> (a) The Issuer shall maintain (i) an office or agency where Notes may be presented for registration of transfer or for exchange ("<u>Registrar</u>") and (ii) an office or agency where Notes may be presented for payment ("<u>Paying Agent</u>"). The Registrar shall keep a register of the Notes ("<u>Note Register</u>") and of their transfer and exchange. The Issuer may appoint one or more co-registrars and one or more additional paying agents. The term "<u>Registrar</u>" includes any co-registrar, and the term "<u>Paying Agent</u>" includes any additional paying agents. The Issuer initially appoints the Trustee as Paying Agent. The Issuer may change any Paying Agent or Registrar without prior notice to any Holder. The Issuer shall notify the Trustee in writing of the name and address of any Agent not a party to this Indenture. If the Issuer fails to appoint or maintain another entity as Registrar or Paying Agent, the Trustee shall, to the extent that it is capable, act as such. The Issuer or any of its domestic Subsidiaries may act as Paying Agent or Registrar.

- (b) The Issuer initially appoints The Depository Trust Company ("DTC") to act as Depositary with respect to the Global Notes representing the Notes.
 - (c) The Issuer initially appoints the Trustee to act as the Registrar for the Notes.

SECTION 2.04. <u>Paying Agent to Hold Money in Trust.</u> The Issuer shall require each Paying Agent other than the Trustee to agree in writing that the Paying Agent shall hold in trust for the benefit of Holders or the Trustee all money held by the Paying Agent for the payment of principal and premium, if any, or interest on the Notes, and will notify the Trustee of any default by the Issuer in making any such payment. While any such default continues, the Trustee may require a Paying Agent to pay all money held by it to the Trustee. The Issuer at any time may require a Paying Agent to pay all money held by it to the Trustee. Upon payment over to the Trustee, the Paying Agent (if other than the Issuer or a Subsidiary) shall have no further liability for the money. If the Issuer or a Subsidiary acts as Paying Agent, it shall segregate and hold in a separate trust fund for the benefit of the Holders all money held by it as Paying Agent. Upon any bankruptcy or reorganization proceedings relating to the Issuer, the Trustee shall serve as Paying Agent for the Notes.

SECTION 2.05. <u>Holder Lists</u>. The Trustee shall preserve in as current a form as is reasonably practicable the most recent list available to it of the names and addresses of all Holders. If the Trustee is not the Registrar, the Issuer shall furnish to the Trustee at least five Business Days before each Interest Payment Date and at such other times as the Trustee may request in writing, a list in such form and as of such date as the Trustee may reasonably require of the names and addresses of the Holders of Notes.

SECTION 2.06. Transfer and Exchange.

(a) <u>Transfer and Exchange of Global Notes.</u> Except as otherwise set forth in this Section 2.06, a Global Note may be transferred, in whole and not in part, only to another nominee of the Depositary or to a successor thereto or a nominee of such successor thereto. A beneficial interest in a Global Note may not be exchanged for a Definitive Note of the same series unless (A) the Depositary (x) notifies the Issuer that it is unwilling or unable to continue as Depositary for such Global Note or (y) has ceased to be a clearing agency registered under the Exchange Act, and, in either case, a successor Depositary is not appointed by the Issuer within 120 days or (B) there shall have occurred and be continuing a Default with respect to the Notes. Upon the occurrence of any of the preceding events in (A) above, Definitive Notes delivered in exchange for any Global Note of the same series or beneficial interests therein will be registered in the names, and issued in any approved denominations, requested by or on behalf of the Depositary (in accordance with its customary procedures). Global Notes also may be exchanged or replaced, in whole or in part, as provided in Sections 2.07 and 2.10 hereof. Every Note authenticated and delivered in exchange for, or in lieu of, a Global Note of the same series or any portion thereof, pursuant to this Section 2.06 or Section 2.07 or 2.10 hereof, shall be authenticated and delivered in the form of, and shall be, a Global Note, except for Definitive Notes issued subsequent to any of the preceding events in (A) or (B) above and pursuant to Section 2.06(c) hereof. A Global Note may be transferred and exchanged as provided in Section 2.06(b) or (c) hereof.

- (b) <u>Transfer and Exchange of Beneficial Interests in the Global Notes.</u> The transfer and exchange of beneficial interests in the Global Notes shall be effected through the Depositary in accordance with the provisions of this Indenture and the Applicable Procedures. Beneficial interests in the Restricted Global Notes shall be subject to restrictions on transfer comparable to those set forth herein to the extent required by the Securities Act. Transfers of beneficial interests in the Global Notes also shall require compliance with either subparagraph (i) or (ii) below, as applicable, as well as one or more of the other following subparagraphs, as applicable:
 - (i) <u>Transfer of Beneficial Interests in the Same Global Note.</u> Beneficial interests in any Restricted Global Note may be transferred to Persons who take delivery thereof in the form of a beneficial interest in the same Restricted Global Note in accordance with the transfer restrictions set forth in the Private Placement Legend; <u>provided</u>, that prior to the expiration of the Restricted Period, transfers of beneficial interests in the Regulation S Temporary Global Note may not be made to a U.S. Person or for the account or benefit of a U.S. Person other than pursuant to Rule 144A. Beneficial interests in any Unrestricted Global Note may be transferred to Persons who take delivery thereof in the form of a beneficial interest in an Unrestricted Global Note. No written orders or instructions shall be required to be delivered to the Registrar to effect the transfers described in this Section 2.06(b) (i).
 - (ii) All Other Transfers and Exchanges of Beneficial Interests in Global Notes. In connection with all transfers and exchanges of beneficial interests that are not subject to Section 2.06(b)(i) hereof, the transferor of such beneficial interest must deliver to the Registrar either (A) (1) a written order from a Participant or an Indirect Participant given to the Depositary in accordance with the Applicable Procedures directing the Depositary to credit or cause to be credited a beneficial interest in another Global Note in an amount equal to the beneficial interest to be transferred or exchanged and (2) instructions given in accordance with the Applicable Procedures containing information regarding the Participant account to be credited with such increase or (B) (1) a written order from a Participant or an Indirect Participant given to the Depositary in accordance with the Applicable Procedures directing the Depositary to cause to be issued a Definitive Note of the same series in an amount equal to the beneficial interest to be transferred or exchanged and (2) instructions given by the Depositary to the Registrar containing information regarding the Person in whose name such Definitive Note shall be registered to effect the transfer or exchange referred to in (1) above; provided that in no event shall Definitive Notes be issued upon the transfer or exchange of beneficial interests in a Regulation S Temporary Global Note prior to (A) the expiration of the Restricted Period and (B) the receipt by the Registrar of any certificates required pursuant to Rule 903. Upon satisfaction of all of the requirements for transfer or exchange of beneficial interests in Global Notes contained in this Indenture and the Notes or otherwise applicable under the Securities Act, the Trustee shall adjust the principal amount of the relevant Global Note(s) pursuant to Section 2.06(g) hereof.

- (iii) <u>Transfer of Beneficial Interests to Another Restricted Global Note.</u> A beneficial interest in any Restricted Global Note may be transferred to a Person who takes delivery thereof in the form of a beneficial interest in another Restricted Global Note if the transfer complies with the requirements of Section 2.06(b)(ii) hereof and the Registrar receives the following:
 - (A) if the transferee will take delivery in the form of a beneficial interest in a 144A Global Note, then the transferor must deliver a certificate in the form of Exhibit B hereto, including the certifications in item (1) thereof; or
 - (B) if the transferee will take delivery in the form of a beneficial interest in a Regulation S Global Note, then the transferor must deliver a certificate in the form of Exhibit B hereto, including the certifications in item (2) thereof.
- (iv) <u>Transfer and Exchange of Beneficial Interests in a Restricted Global Note for Beneficial Interests in an Unrestricted Global Note.</u> A beneficial interest in any Restricted Global Note may be exchanged by any holder thereof for a beneficial interest in an Unrestricted Global Note or transferred to a Person who takes delivery thereof in the form of a beneficial interest in an Unrestricted Global Note if the exchange or transfer complies with the requirements of Section 2.06(b)(ii) hereof and the Registrar receives the following:
 - (A) if the holder of such beneficial interest in a Restricted Global Note proposes to exchange such beneficial interest for a beneficial interest in an Unrestricted Global Note of the same series, a certificate from such Holder substantially in the form of <u>Exhibit C</u> hereto, including the certifications in item (1)(a) thereof; or
 - (B) if the holder of such beneficial interest in a Restricted Global Note proposes to transfer such beneficial interest to a Person who shall take delivery thereof in the form of a beneficial interest in an Unrestricted Global Note of the same series, a certificate from such holder in the form of Exhibit B hereto, including the certifications in item (4) thereof;

and, in each such case, if the Registrar so requests or if the Applicable Procedures so require, an Opinion of Counsel in form reasonably acceptable to the Registrar to the effect that such exchange or transfer is in compliance with the Securities Act and that the restrictions on transfer contained herein and in the Private Placement Legend are no longer required in order to maintain compliance with the Securities Act.

If any such transfer is effected pursuant to this paragraph (iv) at a time when an Unrestricted Global Note has not yet been issued, the Issuer shall issue and, upon receipt of an Authentication Order in accordance with Section 2.02 hereof, the Trustee shall authenticate one or more Unrestricted Global Notes in an aggregate principal amount equal to the aggregate principal amount of beneficial interests transferred pursuant to this paragraph (iv).

Beneficial interests in an Unrestricted Global Note cannot be exchanged for, or transferred to Persons who take delivery thereof in the form of, a beneficial interest in a Restricted Global Note.

- (c) Transfer or Exchange of Beneficial Interests for Definitive Notes.
- (i) <u>Beneficial Interests in Restricted Global Notes to Restricted Definitive Notes.</u> If any holder of a beneficial interest in a Restricted Global Note proposes to exchange such beneficial interest for a Restricted Definitive Note or to transfer such beneficial interest to a Person who takes delivery thereof in the form of a Restricted Definitive Note, then, upon the occurrence of any of the events in subsection (A) of Section 2.06(a) hereof and receipt by the Registrar of the following documentation:
 - (A) if the holder of such beneficial interest in a Restricted Global Note proposes to exchange such beneficial interest for a Restricted Definitive Note, a certificate from such holder substantially in the form of <u>Exhibit C</u> hereto, including the certifications in item (2)(a) thereof;
 - (B) if such beneficial interest is being transferred to a QIB in accordance with Rule 144A, a certificate substantially in the form of Exhibit B hereto, including the certifications in item (1) thereof;
 - (C) if such beneficial interest is being transferred to a Non-U.S. Person in an offshore transaction in accordance with Rule 903 or Rule 904, a certificate substantially in the form of <u>Exhibit B</u> hereto, including the certifications in item (2) thereof;
 - (D) if such beneficial interest is being transferred pursuant to an exemption from the registration requirements of the Securities Act in accordance with Rule 144, a certificate substantially in the form of <u>Exhibit B</u> hereto, including the certifications in item (3)(a) thereof;
 - (E) if such beneficial interest is being transferred to the Issuer or any of its Restricted Subsidiaries, a certificate substantially in the form of Exhibit B hereto, including the certifications in item (3)(b) thereof; or
 - (F) if such beneficial interest is being transferred pursuant to an effective registration statement under the Securities Act, a certificate substantially in the form of Exhibit B hereto, including the certifications in item (3)(c) thereof,

the Trustee shall cause the aggregate principal amount of the applicable Global Note to be reduced accordingly pursuant to Section 2.06(g) hereof, and the Issuer shall execute and the Trustee shall authenticate and mail to the Person designated in the instructions a Definitive Note in the applicable principal amount. Any Definitive Note issued in exchange for a beneficial interest in a Restricted Global Note pursuant to this Section 2.06(c) shall be registered in such name or names and in such authorized denomination or denominations as the holder of such beneficial interest shall instruct the Registrar through instructions from the Depositary and the Participant or Indirect Participant. The Trustee shall mail such Definitive Notes to the Persons in whose names such Notes are so registered. Any Definitive Note issued in exchange for a beneficial interest in a Restricted Global Note pursuant to this Section 2.06(c)(i) shall bear the Private Placement Legend and shall be subject to all restrictions on transfer contained therein.

- (ii) Beneficial Interests in Regulation S Temporary Global Note to Definitive Notes. Notwithstanding Sections 2.06(c)(i)(A) and (C) hereof, a beneficial interest in the Regulation S Temporary Global Note may not be exchanged for a Definitive Note or transferred to a Person who takes delivery thereof in the form of a Definitive Note prior to (A) the expiration of the Restricted Period and (B) the receipt by the Registrar of any certificates required pursuant to Rule 903(b)(3)(ii)(B) of the Securities Act, except in the case of a transfer pursuant to an exemption from the registration requirements of the Securities Act other than Rule 903 or Rule 904.
- (iii) Beneficial Interests in Restricted Global Notes to Unrestricted Definitive Notes. A holder of a beneficial interest in a Restricted Global Note may exchange such beneficial interest for an Unrestricted Definitive Note or may transfer such beneficial interest to a Person who takes delivery thereof in the form of an Unrestricted Definitive Note only upon the occurrence of any of the events in subsection (A) of Section 2.06(a) hereof and if the Registrar receives the following:
 - (A) if the holder of such beneficial interest in a Restricted Global Note proposes to exchange such beneficial interest for an Unrestricted Definitive Note, a certificate from such holder substantially in the form of <u>Exhibit C</u> hereto, including the certifications in item (1)(b) thereof; or
 - (B) if the holder of such beneficial interest in a Restricted Global Note proposes to transfer such beneficial interest to a Person who shall take delivery thereof in the form of an Unrestricted Definitive Note, a certificate from such holder substantially in the form of <u>Exhibit B</u> hereto, including the certifications in item (4) thereof;

and, in each such case, if the Registrar so requests or if the Applicable Procedures so require, an Opinion of Counsel in form reasonably acceptable to the Registrar to the effect that such exchange or transfer is in compliance with the Securities Act and that the restrictions on transfer contained herein and in the Private Placement Legend are no longer required in order to maintain compliance with the Securities Act.

- (iv) Beneficial Interests in Unrestricted Global Notes to Unrestricted Definitive Notes. If any holder of a beneficial interest in an Unrestricted Global Note proposes to exchange such beneficial interest for a Definitive Note or to transfer such beneficial interest to a Person who takes delivery thereof in the form of a Definitive Note, then, upon the occurrence of any of the events in subsection (A) of Section 2.06(a) hereof and satisfaction of the conditions set forth in Section 2.06(b)(ii) hereof, the Trustee shall cause the aggregate principal amount of the applicable Global Note to be reduced accordingly pursuant to Section 2.06(g) hereof, and the Issuer shall execute and the Trustee shall authenticate and mail to the Person designated in the instructions a Definitive Note in the applicable principal amount. Any Definitive Note issued in exchange for a beneficial interest pursuant to this Section 2.06(c)(iv) shall be registered in such name or names and in such authorized denomination or denominations as the holder of such beneficial interest shall instruct the Registrar through instructions from or through the Depositary and the Participant or Indirect Participant. The Trustee shall mail such Definitive Notes to the Persons in whose names such Notes are so registered. Any Definitive Note issued in exchange for a beneficial interest pursuant to this Section 2.06(c)(iv) shall not bear the Private Placement Legend.
 - (d) Transfer and Exchange of Definitive Notes for Beneficial Interests.
- (i) <u>Restricted Definitive Notes to Beneficial Interests in Restricted Global Notes.</u> If any Holder of a Restricted Definitive Note proposes to exchange such Note for a beneficial interest in a Restricted Global Note or to transfer such Restricted Definitive Note to a Person who takes delivery thereof in the form of a beneficial interest in a Restricted Global Note, then, upon receipt by the Registrar of the following documentation:
 - (A) if the Holder of such Restricted Definitive Note proposes to exchange such Note for a beneficial interest in a Restricted Global Note, a certificate from such Holder substantially in the form of <u>Exhibit C</u> hereto, including the certifications in item (2)(b) thereof;
 - (B) if such Restricted Definitive Note is being transferred to a QIB in accordance with Rule 144A, a certificate substantially in the form of Exhibit B hereto, including the certifications in item (1) thereof;

- (C) if such Restricted Definitive Note is being transferred to a Non-U.S. Person in an offshore transaction in accordance with Rule 903 or Rule 904, a certificate substantially in the form of <u>Exhibit B</u> hereto, including the certifications in item (2) thereof;
- (D) if such Restricted Definitive Note is being transferred pursuant to an exemption from the registration requirements of the Securities Act in accordance with Rule 144, a certificate substantially in the form of Exhibit B hereto, including the certifications in item (3)(a) thereof;
- (E) if such Restricted Definitive Note is being transferred to the Issuer or any of its Restricted Subsidiaries, a certificate substantially in the form of Exhibit B hereto, including the certifications in item (3)(b) thereof; or
- (F) if such Restricted Definitive Note is being transferred pursuant to an effective registration statement under the Securities Act, a certificate substantially in the form of <u>Exhibit B</u> hereto, including the certifications in item (3)(c) thereof,

the Trustee shall cancel the Restricted Definitive Note, increase or cause to be increased the aggregate principal amount of, in the case of clause (A) above, the applicable Restricted Global Note, in the case of clause (B) above, the applicable 144A Global Note, and in the case of clause (C) above, the applicable Regulation S Global Note.

- (ii) <u>Restricted Definitive Notes to Beneficial Interests in Unrestricted Global Notes.</u> A Holder of a Restricted Definitive Note may exchange such Note for a beneficial interest in an Unrestricted Global Note or transfer such Restricted Definitive Note to a Person who takes delivery thereof in the form of a beneficial interest in an Unrestricted Global Note only if the Registrar receives the following:
 - (A) if the Holder of such Definitive Notes proposes to exchange such Notes for a beneficial interest in the Unrestricted Global Note, a certificate from such Holder substantially in the form of Exhibit C hereto, including the certifications in item (1)(c) thereof; or
 - (B) if the Holder of such Definitive Notes proposes to transfer such Notes to a Person who shall take delivery thereof in the form of a beneficial interest in the Unrestricted Global Note, a certificate from such Holder substantially in the form of Exhibit B hereto, including the certifications in item (4) thereof;

and, in each such case, if the Registrar so requests or if the Applicable Procedures so require, an Opinion of Counsel in form reasonably acceptable to the Registrar to the effect that such exchange or transfer is in compliance with the Securities Act and that the restrictions on transfer contained herein and in the Private Placement Legend are no longer required in order to maintain compliance with the Securities Act.

Upon satisfaction of the conditions of any of the subparagraphs in this Section 2.06(d)(ii), the Trustee shall cancel the Definitive Notes and increase or cause to be increased the aggregate principal amount of the Unrestricted Global Note.

(iii) <u>Unrestricted Definitive Notes to Beneficial Interests in Unrestricted Global Notes</u>. A Holder of an Unrestricted Definitive Note may exchange such Note for a beneficial interest in an Unrestricted Global Note or transfer such Definitive Notes to a Person who takes delivery thereof in the form of a beneficial interest in an Unrestricted Global Note at any time. Upon receipt of a request for such an exchange or transfer, the Trustee shall cancel the applicable Unrestricted Definitive Note and increase or cause to be increased the aggregate principal amount of one of the Unrestricted Global Notes.

If any such exchange or transfer from a Definitive Note to a beneficial interest is effected pursuant to subparagraph (ii) or (iii) above at a time when an Unrestricted Global Note has not yet been issued, the Issuer shall issue and, upon receipt of an Authentication Order in accordance with Section 2.02 hereof, the Trustee shall authenticate one or more Unrestricted Global Notes in an aggregate principal amount equal to the principal amount of Definitive Notes so transferred.

- (e) <u>Transfer and Exchange of Definitive Notes for Definitive Notes.</u> Upon request by a Holder of Definitive Notes and such Holder's compliance with the provisions of this Section 2.06(e), the Registrar shall register the transfer or exchange of Definitive Notes. Prior to such registration of transfer or exchange, the requesting Holder shall present or surrender to the Registrar the Definitive Notes duly endorsed or accompanied by a written instruction of transfer in form satisfactory to the Registrar duly executed by such Holder or by its attorney, duly authorized in writing. In addition, the requesting Holder shall provide any additional certifications, documents and information, as applicable, required pursuant to the following provisions of this Section 2.06(e):
 - (i) <u>Restricted Definitive Notes to Restricted Definitive Notes.</u> Any Restricted Definitive Note may be transferred to and registered in the name of Persons who take delivery thereof in the form of a Restricted Definitive Note if the Registrar receives the following:
 - (A) if the transfer will be made pursuant to a QIB in accordance with Rule 144A, then the transferor must deliver a certificate substantially in the form of Exhibit B hereto, including the certifications in item (1) thereof;

- (B) if the transfer will be made pursuant to Rule 903 or Rule 904 then the transferor must deliver a certificate in the form of Exhibit B hereto, including the certifications in item (2) thereof; or
- (C) if the transfer will be made pursuant to any other exemption from the registration requirements of the Securities Act, then the transferor must deliver a certificate in the form of <u>Exhibit B</u> hereto, including the certifications required by item (3) thereof, if applicable.
- (ii) <u>Restricted Definitive Notes to Unrestricted Definitive Notes.</u> Any Restricted Definitive Note may be exchanged by the Holder thereof for an Unrestricted Definitive Note or transferred to a Person or Persons who take delivery thereof in the form of an Unrestricted Definitive Note if the Registrar receives the following:
 - (A) if the Holder of such Restricted Definitive Notes proposes to exchange such Notes for an Unrestricted Definitive Note, a certificate from such Holder substantially in the form of Exhibit C hereto, including the certifications in item (1)(d) thereof; or
 - (B) if the Holder of such Restricted Definitive Notes proposes to transfer such Notes to a Person who shall take delivery thereof in the form of an Unrestricted Definitive Note, a certificate from such Holder substantially in the form of Exhibit B hereto, including the certifications in item (4) thereof;
 - and, in each such case, if the Registrar so requests, an Opinion of Counsel in form reasonably acceptable to the Registrar to the effect that such exchange or transfer is in compliance with the Securities Act and that the restrictions on transfer contained herein and in the Private Placement Legend are no longer required in order to maintain compliance with the Securities Act.
- (iii) <u>Unrestricted Definitive Notes to Unrestricted Definitive Notes.</u> A Holder of Unrestricted Definitive Notes may transfer such Notes to a Person who takes delivery thereof in the form of an Unrestricted Definitive Note. Upon receipt of a request to register such a transfer, the Registrar shall register the Unrestricted Definitive Notes pursuant to the instructions from the Holder thereof.

(f) <u>Legends</u>. The following legends shall appear on the face of all Global Notes and Definitive Notes issued under this Indenture unless specifically stated otherwise in the applicable provisions of this Indenture:

(i) Private Placement Legend.

(A) Except as permitted by subparagraph (B) below, each Global Note and each Definitive Note (and all Notes issued in exchange therefor or substitution thereof) shall bear the legend in substantially the following form:

"THE NOTE EVIDENCED HEREBY WAS ORIGINALLY ISSUED IN A TRANSACTION EXEMPT FROM REGISTRATION UNDER SECTION 5 OF THE UNITED STATES SECURITIES ACT OF 1933, AS AMENDED (THE "SECURITIES ACT"), AND THE NOTE EVIDENCED HEREBY MAY NOT BE OFFERED, SOLD, PLEDGED OR OTHERWISE TRANSFERRED IN THE ABSENCE OF SUCH REGISTRATION OR AN APPLICABLE EXEMPTION THEREFROM. EACH PURCHASER OF THE NOTE EVIDENCED HEREBY IS HEREBY NOTIFIED THAT THE SELLER MAY BE RELYING ON THE EXEMPTION FROM THE PROVISIONS OF SECTION 5 OF THE SECURITIES ACT PROVIDED BY RULE 144A THEREUNDER. THE HOLDER OF THE NOTE EVIDENCED HEREBY AGREES FOR THE BENEFIT OF THE COMPANY THAT (A) SUCH NOTE MAY BE OFFERED, SOLD, PLEDGED OR OTHERWISE TRANSFERRED ONLY (1) (a) IN THE UNITED STATES TO A PERSON WHO THE SELLER REASONABLY BELIEVES IS A QUALIFIED INSTITUTIONAL BUYER (AS DEFINED IN RULE 144A UNDER THE SECURITIES ACT) IN A TRANSACTION MEETING THE REQUIREMENTS OF RULE 144A, (b) OUTSIDE THE UNITED STATES IN AN OFFSHORE TRANSACTION IN ACCORDANCE WITH RULE 904 UNDER THE SECURITIES ACT, (c) IN A TRANSACTION MEETING THE REQUIREMENTS OF RULE 144 UNDER THE SECURITIES ACT, (d) TO AN INSTITUTIONAL "ACCREDITED INVESTOR" (AS DEFINED IN RULE 501 (a) (1), (2), (3) OR (7) UNDER THE SECURITIES ACT) THAT, PRIOR TO SUCH TRANSFER, FURNISHES THE TRUSTEE A SIGNED LETTER CONTAINING CERTAIN REPRESENTATIONS AND AGREEMENTS (THE FORM OF WHICH CAN BE OBTAINED FROM THE TRUSTEE) AND, IF SUCH TRANSFER IS IN RESPECT OF AN AGGREGATE PRINCIPAL AMOUNT OF NOTES LESS THAN \$250,000, AN OPINION OF COUNSEL ACCEPTABLE TO THE COMPANY THAT SUCH TRANSFER IS IN COMPLIANCE WITH THE SECURITIES ACT OR (e) IN ACCORDANCE WITH ANOTHER EXEMPTION FROM THE REGISTRATION REQUIREMENTS OF

THE SECURITIES ACT (AND BASED UPON AN OPINION OF COUNSEL IF THE COMPANY SO REQUESTS), (2) TO THE COMPANY OR (3) PURSUANT TO AN EFFECTIVE REGISTRATION STATEMENT AND, IN EACH CASE, IN ACCORDANCE WITH ANY APPLICABLE SECURITIES LAWS OF ANY STATE OF THE UNITED STATES OR ANY OTHER APPLICABLE JURISDICTION AND (B) THE HOLDER WILL, AND EACH SUBSEQUENT HOLDER IS REQUIRED TO, NOTIFY ANY PURCHASER FROM IT OF THE NOTE EVIDENCED HEREBY OF THE RESALE RESTRICTIONS SET FORTH IN (A) ABOVE."

- (B) Notwithstanding the foregoing, any Global Note or Definitive Note issued pursuant to subparagraph (b)(iv), (c)(iii), (d)(ii), (d)(iii), (e)(ii) or (e)(iii) of this Section 2.06 (and all Notes issued in exchange therefor or substitution thereof) shall not bear the Private Placement Legend.
- (ii) <u>Global Note Legend</u>. Each Global Note representing the Notes shall bear a legend in substantially the following form (with appropriate changes in the last sentence if DTC is not the Depositary):

"THIS GLOBAL NOTE IS HELD BY THE DEPOSITARY (AS DEFINED IN THE INDENTURE GOVERNING THIS NOTE) OR ITS NOMINEE IN CUSTODY FOR THE BENEFIT OF THE BENEFICIAL OWNERS HEREOF, AND IS NOT TRANSFERABLE TO ANY PERSON UNDER ANY CIRCUMSTANCES EXCEPT THAT (I) THE TRUSTEE MAY MAKE SUCH NOTATIONS HEREON AS MAY BE REQUIRED PURSUANT TO SECTION 2.06(g) OF THE INDENTURE, (II) THIS GLOBAL NOTE MAY BE EXCHANGED IN WHOLE BUT NOT IN PART PURSUANT TO SECTION 2.06(a) OF THE INDENTURE, (III) THIS GLOBAL NOTE MAY BE DELIVERED TO THE TRUSTEE FOR CANCELLATION PURSUANT TO SECTION 2.11 OF THE INDENTURE AND (IV) THIS GLOBAL NOTE MAY BE TRANSFERRED TO A SUCCESSOR DEPOSITARY WITH THE PRIOR WRITTEN CONSENT OF THE ISSUER. UNLESS AND UNTIL IT IS EXCHANGED IN WHOLE OR IN PART FOR NOTES IN DEFINITIVE FORM, THIS NOTE MAY NOT BE TRANSFERRED EXCEPT AS A WHOLE BY THE DEPOSITARY TO A NOMINEE OF THE DEPOSITARY OR BY A NOMINEE OF THE DEPOSITARY TO THE DEPOSITARY OR ANY SUCH NOMINEE TO A SUCCESSOR DEPOSITARY OR A NOMINEE OF SUCH SUCCESSOR DEPOSITARY. UNLESS THIS CERTIFICATE IS PRESENTED BY AN AUTHORIZED REPRESENTATIVE OF THE DEPOSITORY TRUST COMPANY (55 WATER STREET, NEW YORK, NEW YORK) ("DTC") TO THE ISSUER OR ITS AGENT FOR

REGISTRATION OF TRANSFER, EXCHANGE OR PAYMENT, AND ANY CERTIFICATE ISSUED IS REGISTERED IN THE NAME OF CEDE & CO. OR SUCH OTHER NAME AS MAY BE REQUESTED BY AN AUTHORIZED REPRESENTATIVE OF DTC (AND ANY PAYMENT IS MADE TO CEDE & CO. OR SUCH OTHER ENTITY AS MAY BE REQUESTED BY AN AUTHORIZED REPRESENTATIVE OF DTC), ANY TRANSFER, PLEDGE OR OTHER USE HEREOF FOR VALUE OR OTHERWISE BY OR TO ANY PERSON IS WRONGFUL INASMUCH AS THE REGISTERED OWNER HEREOF, CEDE & CO., HAS AN INTEREST HEREIN."

(iii) <u>Regulation S Temporary Global Note Legend.</u> The Regulation S Temporary Global Note shall bear a legend in substantially the following form:

"THIS NOTE (OR ITS PREDECESSOR) WAS ORIGINALLY ISSUED IN A TRANSACTION ORIGINALLY EXEMPT FROM REGISTRATION UNDER THE U.S. SECURITIES ACT OF 1933, AS AMENDED (THE "SECURITIES ACT"), AND MAY NOT BE TRANSFERRED IN THE UNITED STATES OR TO, OR FOR THE ACCOUNT OR BENEFIT OF, ANY U.S. PERSON EXCEPT PURSUANT TO AN AVAILABLE EXEMPTION FROM THE REGISTRATION REQUIREMENTS OF THE SECURITIES ACT AND ALL APPLICABLE STATE SECURITIES LAWS. TERMS USED ABOVE HAVE THE MEANINGS GIVEN TO THEM IN REGULATION S UNDER THE SECURITIES ACT."

(g) <u>Cancellation and/or Adjustment of Global Notes.</u> At such time as all beneficial interests in a particular Global Note have been exchanged for Definitive Notes or a particular Global Note has been redeemed, repurchased or canceled in whole and not in part, each such Global Note shall be returned to or retained and canceled by the Trustee in accordance with Section 2.11 hereof. At any time prior to such cancellation, if any beneficial interest in a Global Note is exchanged for or transferred to a Person who will take delivery thereof in the form of a beneficial interest in another Global Note or for Definitive Notes, the principal amount of Notes represented by such Global Note shall be reduced accordingly and an endorsement shall be made on such Global Note by the Trustee or by the Depositary at the direction of the Trustee to reflect such reduction; and if the beneficial interest is being exchanged for or transferred to a Person who will take delivery thereof in the form of a beneficial interest in another Global Note, such other Global Note shall be increased accordingly and an endorsement shall be made on such Global Note by the Trustee or by the Depositary at the direction of the Trustee to reflect such increase.

(h) General Provisions Relating to Transfers and Exchanges.

(i) To permit registrations of transfers and exchanges, the Issuer shall execute and the Trustee shall authenticate Global Notes and Definitive Notes upon receipt of an Authentication Order in accordance with Section 2.02 hereof or at the Registrar's request.

- (ii) No service charge shall be made to a holder of a beneficial interest in a Global Note or to a Holder of a Definitive Note for any registration of transfer or exchange, but the Issuer may require payment of a sum sufficient to cover any transfer tax or similar governmental charge payable in connection therewith (other than any such transfer taxes or similar governmental charge payable upon exchange or transfer pursuant to Sections 2.07, 2.10, 3.06, 3.09, 4.10, 4.14 and 9.04 hereof).
- (iii) Neither the Registrar nor the Issuer shall be required to register the transfer of or exchange any Note selected for redemption in whole or in part, except the unredeemed portion of any Note being redeemed in part.
- (iv) All Global Notes and Definitive Notes issued upon any registration of transfer or exchange of Global Notes or Definitive Notes shall be the valid obligations of the Issuer, evidencing the same debt, and entitled to the same benefits under this Indenture, as the Global Notes or Definitive Notes surrendered upon such registration of transfer or exchange.
- (v) The Issuer shall not be required (A) to issue, to register the transfer of or to exchange any Notes during a period beginning at the opening of business 15 days before the day of any selection of Notes for redemption under Section 3.02 hereof and ending at the close of business on the day of selection, (B) to register the transfer of or to exchange any Note so selected for redemption in whole or in part, except the unredeemed portion of any Note being redeemed in part or (C) to register the transfer of or to exchange a Note between a Record Date with respect to such Note and the next succeeding Interest Payment Date with respect to such Note.
- (vi) Prior to due presentment for the registration of a transfer of any Note, the Trustee, any Agent and the Issuer may deem and treat the Person in whose name any Note is registered as the absolute owner of such Note for the purpose of receiving payment of principal of (and premium, if any) and interest on such Notes and for all other purposes, and none of the Trustee, any Agent or the Issuer shall be affected by notice to the contrary.
- (vii) Upon surrender for registration of transfer of any Note at the office or agency of the Issuer designated pursuant to Section 4.02 hereof, the Issuer shall execute, and the Trustee shall authenticate and mail, in the name of the designated transferee or transferees, one or more replacement Notes of any authorized denomination or denominations of a like aggregate principal amount.

- (viii) At the option of the Holder, Notes may be exchanged for other Notes of any authorized denomination or denominations of a like aggregate principal amount upon surrender of the Notes to be exchanged at such office or agency. Whenever any Global Notes or Definitive Notes are so surrendered for exchange, the Issuer shall execute, and the Trustee shall authenticate and mail, the replacement Global Notes and Definitive Notes which the Holder making the exchange is entitled to in accordance with the provisions of Section 2.02 hereof.
- (ix) All certifications, certificates and Opinions of Counsel required to be submitted to the Registrar pursuant to this Section 2.06 to effect a registration of transfer or exchange may be submitted by facsimile.

SECTION 2.07. Replacement Notes. If any mutilated Note is surrendered to the Trustee, the Registrar or the Issuer and the Trustee receives evidence to its satisfaction of the ownership and destruction, loss or theft of any Note, the Issuer shall issue and the Trustee, upon receipt of an Authentication Order, shall authenticate a replacement Note if the Trustee's requirements are met. If required by the Trustee or the Issuer, an indemnity bond must be supplied by the Holder that is sufficient in the judgment of the Trustee and the Issuer to protect the Issuer, the Trustee, any Agent and any authenticating agent from any loss that any of them may suffer if a Note is replaced. The Issuer and the Trustee may charge the Holder for their expenses in replacing a Note.

Every replacement Note is a contractual obligation of the Issuer and shall be entitled to all of the benefits of this Indenture equally and proportionately with all other Notes duly issued hereunder.

SECTION 2.08. <u>Outstanding Notes.</u> The Notes outstanding at any time are all the Notes authenticated by the Trustee except for those canceled by it, those delivered to it for cancellation, those reductions in the interest in a Global Note effected by the Trustee in accordance with the provisions hereof and those described in this Section 2.08 as not outstanding. Except as set forth in Section 2.09 hereof, a Note does not cease to be outstanding because the Issuer, a Guarantor or an Affiliate of the Issuer or a Guarantor holds the Note.

If a Note is replaced pursuant to Section 2.07 hereof, it ceases to be outstanding unless the Trustee receives proof satisfactory to it that the replaced Note is held by a protected purchaser (as defined in Section 8-303 of the Uniform Commercial Code).

If the principal amount of any Note is considered paid under Section 4.01 hereof, it ceases to be outstanding and interest on it ceases to accrue.

If the Paying Agent (other than the Issuer, a Guarantor or an Affiliate of the Issuer or a Guarantor) holds, on a Redemption Date or maturity date, money sufficient to pay Notes (or portions thereof) payable on that date, then on and after that date such Notes (or portions thereof) shall be deemed to be no longer outstanding and shall cease to accrue interest.

SECTION 2.09. <u>Treasury Notes</u>. In determining whether the Holders of the required principal amount of Notes have concurred in any direction, waiver or consent, Notes owned by the Issuer, a Guarantor or by any Affiliate of the Issuer or a Guarantor, shall be considered as though not outstanding, except that for the purposes of determining whether the Trustee shall be protected in relying on any such direction, waiver or consent, only Notes that a Responsible Officer of the Trustee knows are so owned shall be so disregarded. Notes so owned which have been pledged in good faith shall not be disregarded if the pledgee establishes to the satisfaction of the Trustee the pledgee's right to deliver any such direction, waiver or consent with respect to the Notes and that the pledgee is not the Issuer, a Guarantor or any obligor upon the Notes or any Affiliate of the Issuer, a Guarantor or of such other obligor.

SECTION 2.10. <u>Temporary Notes</u>. Until certificates representing Notes are ready for delivery, the Issuer may prepare and the Trustee, upon receipt of an Authentication Order, shall authenticate temporary Notes. Temporary Notes shall be substantially in the form of certificated Notes but may have variations that the Issuer considers appropriate for temporary Notes and as shall be reasonably acceptable to the Trustee. Without unreasonable delay, the Issuer shall prepare and the Trustee shall authenticate definitive Notes in exchange for temporary Notes.

Holders and beneficial holders, as the case may be, of temporary Notes shall be entitled to all of the benefits accorded to Holders, or beneficial holders, respectively, of Notes under this Indenture.

SECTION 2.11. Cancellation. The Issuer at any time may deliver Notes to the Trustee for cancellation. The Registrar and Paying Agent shall forward to the Trustee any Notes surrendered to them for registration of transfer, exchange or payment. The Trustee or, at the direction of the Trustee, the Registrar or the Paying Agent and no one else shall cancel all Notes surrendered for registration of transfer, exchange, payment, replacement or cancellation and shall destroy cancelled Notes (subject to the record retention requirement of the Exchange Act). Certification of the destruction of all cancelled Notes shall be delivered to the Issuer upon written request. The Issuer may not issue new Notes to replace Notes that it has paid or that have been delivered to the Trustee for cancellation.

SECTION 2.12. <u>Defaulted Interest</u>. If the Issuer defaults in a payment of interest on the Notes, it shall pay the defaulted interest in any lawful manner plus, to the extent lawful, interest payable on the defaulted interest, in each case at the rate provided in the Notes and in Section 4.01 hereof. The Issuer may pay the defaulted interest to the Persons who are Holders on a subsequent special record date. The Issuer shall notify the Trustee in writing of the amount of defaulted interest proposed to be paid on each Note and the date of the proposed payment, and at the same time the Issuer shall deposit with the Trustee an amount of money equal to the aggregate amount proposed to be paid in respect of such defaulted interest or shall make arrangements satisfactory to the Trustee for such deposit prior to the date of the proposed payment, such money when deposited to

be held in trust for the benefit of the Persons entitled to such defaulted interest as provided in this Section 2.12. The Trustee shall fix or cause to be fixed any such special record date and payment date; <u>provided</u> that no such special record date shall be less than 10 days prior to the related payment date for such defaulted interest. The Trustee shall promptly notify the Issuer of any such special record date. At least 15 days before any such special record date, the Issuer (or, upon the written request of the Issuer, the Trustee in the name and at the expense of the Issuer) shall send to each Holder, with a copy to the Trustee, a notice at his or her address as it appears in the Note Register that states the special record date, the related payment date and the amount of such interest to be paid.

Subject to the foregoing provisions of this Section 2.12 and for greater certainty, each Note delivered under this Indenture upon registration of transfer of or in exchange for or in lieu of any other Note shall carry the rights to interest accrued and unpaid, and to accrue, which were carried by such other Note.

SECTION 2.13. <u>CUSIP/ISIN Numbers</u>. The Issuer in issuing the Notes may use CUSIP and ISIN numbers (in each case, if then generally in use) and, if so, the Trustee shall use CUSIP and ISIN numbers in notices of redemption as a convenience to Holders; <u>provided</u>, that any such notice may state that no representation is made as to the correctness of such numbers either as printed on the Notes or as contained in any notice of redemption and that reliance may be placed only on the other identification numbers printed on the Notes, and any such redemption shall not be affected by any defect in or omission of such numbers. The Issuer will as promptly as practicable notify the Trustee in writing of any change in the CUSIP and ISIN numbers.

ARTICLE III

REDEMPTION

SECTION 3.01. Notices to Trustee. If the Issuer elects to redeem Notes pursuant to Section 3.07 hereof, it shall furnish to the Trustee, at least 2 Business Days before notice of redemption is required to be mailed or caused to be sent to Holders pursuant to Section 3.03 hereof but not more than 60 days before a Redemption Date, an Officer's Certificate of the Issuer setting forth (i) the paragraph or subparagraph of the Note and/or Section of this Indenture pursuant to which the redemption shall occur, (ii) the Redemption Date, (iii) the principal amount of the Notes to be redeemed and (iv) the redemption price.

SECTION 3.02. <u>Selection of Notes to Be Redeemed.</u> If less than all of the Notes are to be redeemed at any time, the Trustee shall select the Notes to be redeemed (a) if the Notes are listed on any national securities exchange, in compliance with the requirements of the principal national securities exchange on which the Notes are listed or (b) on a <u>pro rata</u> basis to the extent practicable (and if the Notes are represented by one or more Global Notes, in accordance with the Applicable Procedures), or, if the <u>pro rata</u> basis is not practicable for any reason, by lot or by such other method the Trustee shall

deem fair and appropriate. In the event of partial redemption by lot, the particular Notes to be redeemed shall be selected, unless otherwise provided herein, not less than 30 nor more than 60 days prior to the Redemption Date by the Trustee from the outstanding Notes not previously called for redemption.

The Trustee shall promptly notify the Issuer in writing of the Notes selected for redemption and, in the case of any Note selected for partial redemption, the principal amount thereof to be redeemed. Notes and portions of Notes selected shall be in amounts of \$2,000 or whole multiples of \$1,000 in excess thereof; no Notes of less than \$2,000 can be redeemed in part, except that if all of the Notes of a Holder are to be redeemed, the entire outstanding amount of Notes held by such Holder, even if not a multiple of \$1,000 shall be redeemed. Except as provided in the preceding sentence, provisions of this Indenture that apply to Notes called for redemption also apply to portions of Notes called for redemption.

SECTION 3.03. Notice of Redemption. Subject to Section 3.09 hereof, the Issuer shall transmit or cause to be transmitted notices of redemption at least 30 days but not more than 60 days before the Redemption Date to each Holder of Notes to be redeemed at such Holder's registered address or otherwise in accordance with Applicable Procedures, except that redemption notices may be transmitted more than 60 days prior to a Redemption Date if the notice is issued in connection with Article 8 or Article 12 hereof. Except pursuant to a notice of redemption delivered in accordance with a redemption pursuant to Sections 3.07(b) hereof, notices of redemption may not be conditional.

The notice shall identify the Notes to be redeemed and shall state:

- (a) the Redemption Date;
- (b) the redemption price;
- (c) if any Note is to be redeemed in part only, the portion of the principal amount of that Note that is to be redeemed and that, after the Redemption Date upon surrender of such Note, a new Note or Notes in principal amount equal to the unredeemed portion of the original Note representing the same indebtedness to the extent not redeemed will be issued in the name of the Holder of the Notes upon cancellation of the original Note;
 - (d) the name and address of the Paying Agent;
 - (e) that Notes called for redemption must be surrendered to the Paying Agent to collect the redemption price;
- (f) that, unless the Issuer defaults in making such redemption payment, interest on Notes called for redemption ceases to accrue on and after the Redemption Date;

- (g) the paragraph or subparagraph of the Notes and/or Section of this Indenture pursuant to which the Notes called for redemption are being redeemed;
- (h) the CUSIP and ISIN number, if any, printed on the Notes being redeemed and that no representation is made as to the correctness or accuracy of any such CUSIP and ISIN number that is listed in such notice or printed on the Notes; and
 - (i) if in connection with a redemption pursuant to Section 3.07(b) hereof, any condition to such redemption.

At the Issuer's request, the Trustee shall give the notice of redemption in the Issuer's name and at its expense; <u>provided</u> that the Issuer shall have delivered to the Trustee, at least 2 Business Days before notice of redemption is required to be transmitted or caused to be transmitted to Holders pursuant to this Section 3.03 (unless a shorter notice shall be agreed to by the Trustee), an Officer's Certificate of the Issuer requesting that the Trustee give such notice and setting forth the information to be stated in such notice as provided in the preceding paragraph.

SECTION 3.04. Effect of Notice of Redemption. Once notice of redemption is transmitted in accordance with Section 3.03 hereof, Notes called for redemption become irrevocably due and payable on the Redemption Date at the redemption price (except as provided for in Sections 3.07(b) hereof). The notice, if transmitted in a manner herein provided, shall be conclusively presumed to have been given, whether or not the Holder receives such notice. In any case, failure to give such notice or any defect in the notice to the Holder of any Note designated for redemption in whole or in part shall not affect the validity of the proceedings for the redemption of any other Note. Subject to Section 3.05 hereof, on and after the Redemption Date, interest ceases to accrue on Notes or portions of Notes called for redemption.

SECTION 3.05. Deposit of Redemption Price.

- (a) Prior to 11:00 a.m. (New York City time) on the Redemption Date, the Issuer shall deposit with the Trustee or with the Paying Agent money sufficient to pay the redemption price of and accrued and unpaid interest on all Notes to be redeemed on that Redemption Date. The Trustee or the Paying Agent shall promptly return to the Issuer any money deposited with the Trustee or the Paying Agent by the Issuer in excess of the amounts necessary to pay the redemption price of, and accrued and unpaid interest on, all Notes to be redeemed.
- (b) If the Issuer complies with the provisions of the preceding paragraph (a), on and after the Redemption Date, interest shall cease to accrue on the applicable series of Notes or the portions of Notes called for redemption. If a Note is redeemed on or after a Record Date but on or prior to the related Interest Payment Date, then any accrued and unpaid interest to the Redemption Date shall be paid to the Person in whose name such Note was registered at the close of business on such Record Date. If any Note called for redemption shall not be so paid upon surrender for redemption

because of the failure of the Issuer to comply with the preceding paragraph, interest shall be paid on the unpaid principal, from the Redemption Date until such principal is paid, and to the extent lawful on any interest accrued to the Redemption Date not paid on such unpaid principal, in each case at the rate provided in the Notes and in Section 4.01 hereof.

SECTION 3.06. Notes Redeemed in Part. Upon surrender of a Note that is redeemed in part, the Issuer shall issue and the Trustee shall authenticate for the Holder at the expense of the Issuer a new Note equal in principal amount to the unredeemed portion of the Note surrendered representing the same indebtedness to the extent not redeemed; <u>provided</u> that each new Note will be in a principal amount of \$2,000 or an integral multiple of \$1,000 in excess thereof. It is understood that, notwithstanding anything in this Indenture to the contrary, only an Authentication Order and not an Opinion of Counsel or Officer's Certificate of the Issuer is required for the Trustee to authenticate such new Note.

SECTION 3.07. Optional Redemption.

- (a) At any time prior to November 15, 2016, the Issuer may redeem all or a part of the Notes, upon notice in accordance with Section 3.03, at a redemption price equal to 100% of the principal amount of the Notes redeemed plus the Applicable Premium as of, and accrued and unpaid interest, if any, to, the date of redemption (the "Redemption Date"), subject to the right of Holders of record on the relevant record date to receive interest due on the relevant interest payment date.
- (b) Until November 15, 2016, the Issuer may, at its option, redeem up to 35% of the aggregate principal amount of Notes issued by it at a redemption price equal to 106.000% of the aggregate principal amount thereof, plus accrued and unpaid interest, if any, to, the Redemption Date, subject to the right of Holders of Notes of record on the relevant record date to receive interest due on the relevant interest payment date, with the net cash proceeds received by it from one or more Equity Offerings; provided that (i) at least 50% of the sum of the aggregate principal amount of Notes originally issued under this Indenture and any Additional Notes that are Notes issued under this Indenture after the Issue Date remain outstanding immediately after the occurrence of each such redemption; and (ii) each such redemption occurs within 180 days of the date of closing of each such Equity Offering.
 - (c) Except pursuant to clause (a) or (b) of this Section 3.07, the Notes will not be redeemable at the Issuer's option prior to November 15, 2016.
- (d) On and after November 15, 2016, the Issuer may redeem the Notes, in whole or in part, upon notice in accordance with Section 3.03 at the redemption prices (expressed as percentages of principal amount of the Notes to be redeemed) set forth below, plus accrued and unpaid interest, if any, to the Redemption Date, subject to the right of Holders of record on the relevant record date to receive interest due on the relevant interest payment date, if redeemed during the twelve-month period beginning on November 15 of each of the years indicated below:

| <u>Year</u> | Percentage |
|---------------------|------------|
| <u>Year</u> 2016 | 104.500% |
| 2017 | 103.000% |
| 2018 | 101.500% |
| 2019 and thereafter | 100.000% |

(e) Any redemption pursuant to this Section 3.07 shall be made pursuant to the provisions of Sections 3.01 through 3.06 hereof.

SECTION 3.08. <u>Mandatory Redemption</u>. The Issuer shall not be required to make any mandatory redemption or sinking fund payments with respect to the Notes.

SECTION 3.09. Offers to Repurchase by Application of Excess Proceeds.

- (a) In the event that, pursuant to Section 4.10 hereof, the Issuer shall be required to commence an Asset Sale Offer, it shall follow the procedures specified below.
- (b) The Asset Sale Offer shall remain open for a period of 20 Business Days following its commencement and no longer, except to the extent that a longer period is required by applicable law (the "Offer Period"). No later than five Business Days after the termination of the Offer Period (the "Purchase Date"), the Issuer shall apply all Excess Proceeds (the "Offer Amount") to the purchase of Notes and, if required, any other Indebtedness constituting First Lien Obligations (on a pro rata basis, if applicable), or, if less than the Offer Amount has been tendered, all Notes and any other Indebtedness constituting First Lien Obligations tendered in response to the Asset Sale Offer. Payment for any Notes so purchased shall be made in the same manner as interest payments are made.
- (c) If the Purchase Date is on or after a Record Date and on or before the related Interest Payment Date, any accrued and unpaid interest, up to but excluding the Purchase Date, shall be paid to the Person in whose name a Note is registered at the close of business on such Record Date, and no additional interest shall be payable to Holders who tender Notes pursuant to the Asset Sale Offer.
- (d) Upon the commencement of an Asset Sale Offer, the Issuer shall send a notice to each of the Holders, with a copy to the Trustee. The notice shall contain all instructions and materials necessary to enable such Holders to tender Notes pursuant to the Asset Sale Offer. The Asset Sale Offer shall be made to all Holders and holders of any other Indebtedness constituting First Lien Obligations. The notice, which shall govern the terms of the Asset Sale Offer, shall state:
 - (i) that the Asset Sale Offer is being made pursuant to this Section 3.09 and Section 4.10 hereof and the length of time the Asset Sale Offer shall remain open;

- (ii) the Offer Amount, the purchase price and the Purchase Date;
- (iii) that any Note not tendered or accepted for payment shall continue to accrue interest;
- (iv) that, unless the Issuer defaults in making such payment, any Note accepted for payment pursuant to the Asset Sale Offer shall cease to accrue interest after the Purchase Date;
- (v) that any Holder electing to have less than all of the aggregate principal amount of its Notes purchased pursuant to an Asset Sale Offer may elect to have Notes purchased in denominations of \$2,000 or whole multiples of \$1,000 in excess thereof;
- (vi) that Holders electing to have a Note purchased pursuant to any Asset Sale Offer shall be required to surrender the Note, with the form entitled "Option of Holder to Elect Purchase" attached to the Note completed, or transfer by book-entry transfer, to the Issuer, the Depositary, if appointed by the Issuer, or a Paying Agent at the address specified in the notice at least two Business Days before the Purchase Date;
- (vii) that Holders shall be entitled to withdraw their election if the Issuer, the Depositary or the Paying Agent, as the case may be, receives, not later than the expiration of the Offer Period, a facsimile transmission or letter setting forth the name of the Holder, the principal amount of the Note the Holder delivered for purchase and a statement that such Holder is withdrawing his election to have such Note purchased;
- (viii) that, if the aggregate principal amount of Notes and any other Indebtedness constituting First Lien Obligations surrendered by the holders thereof exceeds the Offer Amount, the Trustee shall select the Notes and such other Indebtedness constituting First Lien Obligations to be purchased on a <u>pro rata</u> basis based on the accreted value or principal amount of the Notes or such other Indebtedness constituting First Lien Obligations tendered (with such adjustments as may be deemed appropriate by the Trustee so that only Notes in denominations of \$2,000 or whole multiples of \$1,000 in excess thereof are purchased); and
- (ix) that Holders whose Notes were purchased only in part shall be issued new Notes equal in principal amount to the unpurchased portion of the Notes surrendered (or transferred by book-entry transfer) representing the same indebtedness to the extent not repurchased.

- (e) On or before the Purchase Date, the Issuer shall, to the extent lawful, (1) accept for payment, on a <u>pro rata</u> basis as described in clause (d) (viii) of this Section 3.09, the Offer Amount of Notes or portions thereof validly tendered pursuant to the Asset Sale Offer, or if less than the Offer Amount has been tendered, all Notes tendered and (2) deliver or cause to be delivered to the Trustee the Notes properly accepted together with an Officer's Certificate stating the aggregate principal amount of Notes or portions thereof so tendered.
- (f) The Issuer, the Depositary or the Paying Agent, as the case may be, shall promptly mail or deliver to each tendering Holder an amount equal to the purchase price of the Notes properly tendered by such Holder and accepted by the Issuer for purchase, and the Issuer shall promptly issue a new Note, and the Trustee, upon receipt of an Authentication Order, shall authenticate and mail or deliver (or cause to be transferred by book-entry) such new Note to such Holder (it being understood that, notwithstanding anything in this Indenture to the contrary, no Opinion of Counsel or Officer's Certificate of the Issuer is required for the Trustee to authenticate and mail or deliver such new Note) in a principal amount equal to any unpurchased portion of the Note surrendered representing the same indebtedness to the extent not repurchased. Any Note not so accepted shall be promptly mailed or delivered by the Issuer to the Holder thereof. The Issuer shall publicly announce the results of the Asset Sale Offer on or as soon as practicable after the Purchase Date.
- (g) Prior to 11:00 a.m. (New York City time) on the Purchase Date, the Issuer shall deposit with the Trustee or with the Paying Agent money sufficient to pay the purchase price of and accrued and unpaid interest on all Notes to be purchased on that purchase date. The Trustee or the Paying Agent shall promptly return to the Issuer any money deposited with the Trustee or the Paying Agent by the Issuer in excess of the amounts necessary to pay the purchase price of, and accrued and unpaid interest on, all Notes to be redeemed.

Other than as specifically provided in this Section 3.09 or Section 4.10 hereof, any purchase pursuant to this Section 3.09 shall be made pursuant to the applicable provisions of Sections 3.01 through 3.06 hereof, and references therein to "redeem," "redemption" and similar words shall be deemed to refer to "purchase," "repurchase" and similar words, as applicable.

ARTICLE IV

COVENANTS

SECTION 4.01. <u>Payment of Notes.</u> The Issuer shall pay or cause to be paid the principal of, premium, if any, and interest on the Notes on the dates and in the manner provided in the Notes. Principal, premium, if any, and interest shall be considered paid on the date due if the Paying Agent, if other than the Issuer, a Guarantor or an Affiliate of the Issuer or a Guarantor, holds as of 11:00 a.m. Eastern Time on the due date money deposited by the Issuer in immediately available funds and designated for and sufficient to pay all principal, premium, if any, and interest then due.

The Issuer shall pay interest (including post-petition interest in any proceeding under any Bankruptcy Law) on overdue principal at the rate equal to the then applicable interest rate on the Notes to the extent lawful; it shall pay interest (including post-petition interest in any proceeding under any Bankruptcy Law) on overdue installments of interest (without regard to any applicable grace period) at the same rate to the extent lawful.

SECTION 4.02. <u>Maintenance of Office or Agency.</u> The Issuer shall maintain the offices or agencies (which may be an office of the Trustee or an affiliate of the Trustee, Registrar or co-registrar) required under Section 2.03 where Notes may be surrendered for registration of transfer or for exchange and where notices and demands to or upon the Issuer in respect of the Notes and this Indenture may be served. The Issuer shall give prompt written notice to the Trustee of the location, and any change in the location, of such office or agency. If at any time the Issuer shall fail to maintain any such required office or agency or shall fail to furnish the Trustee with the address thereof, such presentations, surrenders, notices and demands may be made or served at the Corporate Trust Office of the Trustee.

The Issuer may also from time to time designate one or more other offices or agencies where the Notes may be presented or surrendered for any or all such purposes and may from time to time rescind such designations; <u>provided</u> that no such designation or rescission shall in any manner relieve the Issuer of its obligation to maintain such offices or agencies as required by Section 2.03 for such purposes. The Issuer shall give prompt written notice to the Trustee of any such designation or rescission and of any change in the location of any such other office or agency.

The Issuer hereby designates the Corporate Trust Office of the Trustee as one such office or agency of the Issuer in accordance with Section 2.03 hereof.

SECTION 4.03. Reports and Other Information.

- (a) Notwithstanding that Holdings III may not be subject to the reporting requirements of Section 13 or 15(d) of the Exchange Act or that Holdings III does not otherwise report on an annual and quarterly basis on forms provided for such annual and quarterly reporting pursuant to rules and regulations promulgated by the SEC, Holdings III shall file with the SEC (and make available to the Trustee and Holders of the Notes (without exhibits), without cost to any Holder, within 15 days after it files them with the SEC) from and after the Issue Date,
 - (1) within 90 days (or any other time period then in effect under the rules and regulations of the Exchange Act with respect to the filing of a Form 10-K by a non-accelerated filer) after the end of each fiscal year, annual reports on Form 10-K, or any successor or comparable form, containing the information required to be contained therein, or required in such successor or comparable form;

- (2) within 45 days (or any other time period then in effect under the rules and regulations of the Exchange Act with respect to the filing of a Form 10-Q by a non-accelerated filer) after the end of each of the first three fiscal quarters of each fiscal year, reports on Form 10-Q containing all quarterly information that would be required to be contained in Form 10-Q, or any successor or comparable form;
- (3) promptly from time to time after the occurrence of an event required to be therein reported, such other reports on Form 8-K, or any successor or comparable form; and
- (4) any other information, documents and other reports which Holdings III would be required to file with the SEC if it were subject to Section 13 or 15(d) of the Exchange Act;

in each case, in a manner that complies in all material respects with the requirements specified in such form (assuming Holdings III were a U.S. person with only unsecured debt registered under the Securities Act); <u>provided</u>, that Holdings III shall not be so obligated to file such reports with the SEC if the SEC does not permit such filing, in which event Holdings III will make available such information to prospective purchasers of Notes, in addition to providing such information to the Trustee and the Holders of the Notes, in each case within 15 days after the time Holdings III would be required to file such information with the SEC, if it were subject to Sections 13 or 15(d) of the Exchange Act. Delivery of such reports, information and documents to the Trustee is for informational purposes only and the Trustee's receipt of such shall not constitute constructive notice of any information contained therein, including compliance with any of the covenants hereunder (as to which the Trustee is entitled to rely exclusively on Officer's Certificates).

In addition, to the extent not satisfied by the foregoing, for so long as any Notes are outstanding, Holdings III shall furnish to Holders and to securities analysts and prospective investors, upon their request, the information required to be delivered pursuant to Rule 144A(d)(4) under the Securities Act.

(b) For so long as Parent, Holdings II or any other direct or indirect parent company of Holdings III is a Guarantor, Holdings III shall be permitted to satisfy its obligations under this Section 4.03 with respect to financial information relating to Holdings III by furnishing financial information relating to Parent, Holdings II or such other parent; <u>provided</u> that the same is accompanied by consolidating information that explains in reasonable detail the differences between the information relating to Parent, Holdings II or such other parent, on the one hand, and the information relating to Holdings III and its Restricted Subsidiaries on a standalone basis, on the other hand or, at Holdings III's option, substantially in the form required by Rule 3-10(d) of Regulation S-X or any successor thereto.

- (c) Holdings III will be deemed to have furnished reports required to be delivered under this Section 4.03 to the Trustee and the Holders if it has filed such reports with the SEC using the Edgar filing system and such reports are publicly available without charge.
- (d) Notwithstanding anything herein to the contrary, Holdings III will not be deemed to have failed to comply with any of its obligations under this Section 4.03 for purposes of clause (3) under Section 6.01 until 120 days after the date any report is due under this Section 4.03.

SECTION 4.04. Compliance Certificate.

- (a) Holdings III shall deliver to the Trustee, within 90 days after the end of each fiscal year ending after the Issue Date, a certificate from the principal executive officer, principal financial officer or principal accounting officer stating that a review of the activities of Holdings III and its Restricted Subsidiaries during the preceding fiscal year has been made under the supervision of the signing Officer with a view to determining whether Holdings III and its Restricted Subsidiaries have kept, observed, performed and fulfilled their obligations under this Indenture, and further stating, as to such Officer signing such certificate, that to the best of his or her knowledge Holdings III and its Restricted Subsidiaries have kept, observed, performed and fulfilled each and every condition and covenant contained in this Indenture and is not in default in the performance or observance of any of the terms, provisions, covenants and conditions of this Indenture (or, if a Default shall have occurred, describing all such Defaults of which he or she may have knowledge and what action Holdings III is taking or proposes to take with respect thereto).
- (b) When any Default has occurred and is continuing under this Indenture, or if the Trustee or the holder of any other evidence of Indebtedness of Holdings III or any Subsidiary gives any notice or takes any other action with respect to a claimed Default, Holdings III shall promptly (which shall be no more than five (5) Business Days after becoming aware of such Default) deliver to the Trustee by registered or certified mail or by facsimile transmission an Officer's Certificate specifying such event and what action Holdings III proposes to take with respect thereto.

SECTION 4.05. Taxes.

(a) Holdings III shall pay, and shall cause each of its Restricted Subsidiaries to pay, prior to delinquency, all material taxes, assessments, and governmental levies except such as are contested in good faith and by appropriate negotiations or proceedings or where the failure to effect such payment is not adverse in any material respect to the Holders of the Notes.

- (b) All payments that any Guarantor that is not organized or existing under the laws of the United States, any state thereof, the District of Columbia, or any territory thereof (each a "Foreign Payor") makes under or with respect to the Notes or any Guarantee, will be made free and clear of, and without withholding or deduction for or on account of, any present or future tax, duty, levy, impost, assessment or other governmental charges (including penalties, interest and other similar liabilities related thereto) of whatever nature (collectively, "Taxes") imposed or levied by or on behalf of any jurisdiction in which any Foreign Payor is incorporated, organized or otherwise resident for tax purposes or from or through which any of the foregoing makes any payment on the Notes or by any taxing authority therein or political subdivision thereof (each, as applicable, a "Relevant Taxing Jurisdiction"), unless the applicable Foreign Payor is required to withhold or deduct Taxes by law or by the interpretation or administration of law. If a Foreign Payor is required to withhold or deduct any amount for, or on account of, Taxes of a Relevant Taxing Jurisdiction from any payment made under or with respect to the Notes or any Guarantee, such Foreign Payor will pay such additional amounts ("Additional Amounts") as may be necessary to ensure that the net amount received by each Holder of the Notes after such withholding or deduction will be not less than the amount such Holder would have received if such Taxes had not been required to be withheld or deducted.
- (c) Notwithstanding the foregoing, no Foreign Payor will be required to pay Additional Amounts to a Holder of Notes in respect of or on account
 - (1) any Taxes that are imposed or levied by a Relevant Taxing Jurisdiction by reason of such Holder's present or former connection with such Relevant Taxing Jurisdiction, including such Holder being or having been a citizen, national, or resident, being or having been engaged in a trade or business, being, or having been, physically present in or having or having had a permanent establishment in a Relevant Taxing Jurisdiction (but not including, in each case, any connection arising from the mere receipt or holding of Notes or the receipt of payments thereunder or under a Guarantee or the exercise or enforcement of rights under any Notes or this Indenture or a Guarantee);
 - (2) any Taxes that are imposed or levied by reason of the failure of such Holder, following the written request of any Foreign Payor (as the case may be) addressed to such Holder (and made at a time that would enable such Holder acting reasonably to comply with that request) made in accordance with the notice procedures set forth in this Indenture, to comply with any certification, identification, information or other reporting requirements, whether required by statute, treaty, regulation or administrative practice of a Relevant Taxing Jurisdiction, as a precondition to exemption from, or reduction in the rate of withholding or deduction of, Taxes imposed by the Relevant Taxing Jurisdiction (including a certification that such Holder is not resident in the Relevant Taxing Jurisdiction);
 - (3) any estate, inheritance, gift, sales, transfer, personal property or similar Taxes;

- (4) any Tax that is payable otherwise than by withholding or deduction from payments made under or with respect to the Notes;
- (5) any Tax that is imposed or levied by reason of the presentation (where presentation is required in order to receive payment) of the Notes for payment on a date more than 30 days after the date on which such payment became due and payable or the date on which payment thereof is duly provided for, whichever is later, except to the extent that the beneficial owner or holder thereof would have been entitled to Additional Amounts had the Notes been presented for payment on any date during such 30 day period;
- (6) any Tax except to the extent it exceeds any Tax that would have been required to be withheld from payments to the Holder if such payments were made by the Issuer; or
 - (7) any combination of items (1) through (6) above.
- (d) Additional Amounts will not be paid with respect to the Notes to a Holder who is a fiduciary, a partnership, a limited liability company or other than the sole beneficial owner of the payment under or with respect to the Notes, to the extent that payment would be required by the laws of a Relevant Taxing Jurisdiction to be included in the income, for tax purposes, of a beneficiary or settlor with respect to the fiduciary, a member of that partnership, an interest holder in that limited liability company or a beneficial owner who would not have been entitled to the Additional Amounts had it been the Holder of the Notes.
- (e) The relevant Foreign Payor shall (i) make such withholding or deduction as is required by applicable law and (ii) remit the full amount withheld or deducted to the relevant taxing authority in accordance with applicable law.

At least 30 calendar days prior to each date on which any payment under or with respect to the Notes is due and payable, if the relevant Foreign Payor will be obligated to pay Additional Amounts with respect to such payment (unless such obligation to pay Additional Amounts arises after the 30th day prior to the date on which payment under or with respect to the Notes is due and payable, in which case it will be promptly thereafter), the relevant Foreign Payor will deliver to the Trustee an Officer's Certificate of such Foreign Payor stating that such Additional Amounts will be payable and the amounts so payable and will set forth such other information necessary to enable the Trustee to pay such Additional Amounts to the applicable Holders on the payment date

The relevant Foreign Payor shall promptly publish a notice in accordance with the notice provisions set forth in this Indenture stating that such Additional Amounts will be payable and describing the obligation to pay such amounts.

- (f) Upon written request, the relevant Foreign Payor shall furnish to the Trustee or to a Holder of the Notes copies of tax receipts evidencing the payment of any Taxes by such Foreign Payor in such form as provided in the normal course by the taxing authority imposing such Taxes and as is reasonably available to such Foreign Payor. If, notwithstanding the efforts of such Foreign Payor to obtain such receipts, the same are not obtainable, such Foreign Payor shall provide the Trustee or the applicable Holder with other evidence reasonably satisfactory to the Trustee or such Holder.
- (g) The Issuer and any Guarantor, as the case may be, will pay any present or future stamp, issue, registration, court, documentation, excise or property taxes or other similar taxes, charges and duties, including interest and penalties with respect thereto, imposed by or in any Relevant Taxing Jurisdiction in respect of the execution, issue, enforcement or delivery of the Notes or any other document or instrument referred to thereunder (other than on or in connection with a transfer of the Notes other than the initial resale by the Initial Purchasers).
- (h) Whenever this Indenture or the Notes refers to, in any context, the payment of principal, premium, if any, interest or any other amount payable under or with respect to any Note or with respect to any Guarantee, such reference includes the payment of Additional Amounts, if applicable.

SECTION 4.06. Stay, Extension and Usury Laws. The Issuer and each of the Guarantors covenant (to the extent that they may lawfully do so) that they shall not at any time insist upon, plead, or in any manner whatsoever claim or take the benefit or advantage of, any stay, extension or usury law wherever enacted, now or at any time hereafter in force, that may affect the covenants or the performance of this Indenture; and the Issuer and each of the Guarantors (to the extent that they may lawfully do so) hereby expressly waive all benefit or advantage of any such law, and covenant that they shall not, by resort to any such law, hinder, delay or impede the execution of any power herein granted to the Trustee, but shall suffer and permit the execution of every such power as though no such law has been enacted.

SECTION 4.07. Limitation on Restricted Payments.

- (a) Holdings III shall not, and shall not permit any of its Restricted Subsidiaries to, directly or indirectly:
- (I) declare or pay any dividend or make any payment or distribution on account of Holdings III's, or any of its Restricted Subsidiaries' Equity Interests, including any dividend or distribution payable in connection with any merger, amalgamation or consolidation other than:
 - (A) dividends or distributions by Holdings III payable solely in Equity Interests (other than Disqualified Stock) of Holdings III; or

- (B) dividends or distributions by a Restricted Subsidiary so long as, in the case of any dividend or distribution payable on or in respect of any class or series of securities issued by a Restricted Subsidiary other than a Wholly-Owned Subsidiary, Holdings III or a Restricted Subsidiary receives at least its <u>pro rata</u> share of such dividend or distribution in accordance with its Equity Interests in such class or series of securities;
- (II) purchase, redeem, defease or otherwise acquire or retire for value any Equity Interests of Holdings III or any direct or indirect parent of Holdings III, including in connection with any merger, amalgamation or consolidation;
- (III) make any principal payment on, or redeem, repurchase, defease or otherwise acquire or retire for value in each case, prior to any scheduled repayment, sinking fund payment or maturity, any Subordinated Indebtedness, other than:
 - (A) Indebtedness permitted under clauses (7) and (8) of Section 4.09(b) hereof; or
 - (B) the purchase, repurchase or other acquisition of Subordinated Indebtedness purchased in anticipation of satisfying a sinking fund obligation, principal installment or final maturity, in each case due within one year of the date of purchase, repurchase or acquisition; or
 - (IV) make any Restricted Investment

(all such payments and other actions set forth in clauses (I) through (IV) above being collectively referred to as "Restricted Payments"), unless, at the time of such Restricted Payment:

- (1) no Default shall have occurred and be continuing or would occur as a consequence thereof;
- (2) immediately after giving effect to such transaction on a <u>pro forma</u> basis, Holdings III could incur \$1.00 of additional Indebtedness pursuant to the Fixed Charge Coverage Test set forth in Section 4.09(a) hereof; and
- (3) such Restricted Payment, together with the aggregate amount of all other Restricted Payments made by Holdings III and its Restricted Subsidiaries after the Measurement Date (including Restricted Payments permitted by clauses (1), (2) (with respect to the payment of dividends on Refunding Capital Stock pursuant to clause (b) thereof only), (6)(c) and (14) of Section 4.07(b) hereof, but excluding all other Restricted Payments permitted by Section 4.07(b) hereof), is less than the sum of (without duplication):

- (A) 50% of the Consolidated Net Income of Holdings III for the period (taken as one accounting period and including the predecessor) beginning on October 2, 2010, to the end of Holdings III's recently ended fiscal quarter for which internal financial statements are available at the time of such Restricted Payment, or, in the case such Consolidated Net Income for such period is a deficit, minus 100% of such deficit; plus
- (B) 100% of the aggregate net cash proceeds and the fair market value of marketable securities or other property received by Holdings III since immediately after the Measurement Date (other than net cash proceeds to the extent such net cash proceeds have been used to incur Indebtedness, Disqualified Stock or Preferred Stock pursuant to clause (12)(a) of Section 4.09(b) hereof) from the issue or sale of:
 - (i) (A) Equity Interests of Holdings III, including Treasury Capital Stock, but excluding cash proceeds and the fair market value of marketable securities or other property received from the sale of:
 - (x) Equity Interests to members of management, directors or consultants of Holdings III, any direct or indirect parent company of Holdings III and Holdings III's Subsidiaries after the Measurement Date to the extent such amounts have been applied to Restricted Payments made in accordance with clause (4) of Section 4.07(b) hereof; and
 - (y) Designated Preferred Stock;
 - and (B) to the extent such net cash proceeds are actually contributed to Holdings III, Equity Interests of Holdings III's direct or indirect parent companies (excluding contributions of the proceeds from the sale of Designated Preferred Stock of such companies or contributions to the extent such amounts have been applied to Restricted Payments made in accordance with clause (4) of Section 4.07(b) hereof; or
- (ii) debt securities of Holdings III that have been converted into or exchanged for such Equity Interests of Holdings III; provided, that this clause (B) shall not include the proceeds from (W) Refunding Capital Stock, (X) Equity Interests or convertible debt securities of Holdings III sold to a Restricted Subsidiary, (Y) Disqualified Stock or debt securities that have been converted into Disqualified Stock or (Z) Excluded Contributions; plus

- (C) 100% of the aggregate amount of cash and the fair market value of marketable securities or other property contributed to the capital of Holdings III following the Measurement Date (other than net cash proceeds to the extent such net cash proceeds have been used to incur Indebtedness, Disqualified Stock or Preferred Stock pursuant to clause (12)(a) of Section 4.09(b) hereof) (other than by a Restricted Subsidiary and other than by any Excluded Contributions); plus
- (D) 100% of the aggregate amount received in cash and the fair market value of marketable securities or other property received by means of:
 - (i) the sale or other disposition (other than to Holdings III or a Restricted Subsidiary) of Restricted Investments made by Holdings III or its Restricted Subsidiaries and repurchases and redemptions of such Restricted Investments from Holdings III or its Restricted Subsidiaries and repayments of loans or advances, and releases of guarantees, which constitute Restricted Investments by Holdings III or its Restricted Subsidiaries, in each case after the Measurement Date; or
 - (ii) the sale (other than to Holdings III or a Restricted Subsidiary) of the stock of an Unrestricted Subsidiary or a distribution from an Unrestricted Subsidiary (other than in each case to the extent the Investment in such Unrestricted Subsidiary was made by Holdings III or a Restricted Subsidiary pursuant to clause (7) of Section 4.07(b) hereof or to the extent such Investment constituted a Permitted Investment) or a dividend from an Unrestricted Subsidiary after the Measurement Date; <u>plus</u>
- (E) in the case of the redesignation of an Unrestricted Subsidiary as a Restricted Subsidiary after the Measurement Date, the fair market value of the Investment in such Unrestricted Subsidiary (which, if the fair market value of such Investment shall exceed \$100.0 million, shall be set forth in writing by an Independent Financial Advisor), at the time of the redesignation of such Unrestricted Subsidiary as a Restricted Subsidiary other than an Unrestricted Subsidiary to the extent the Investment in such Unrestricted Subsidiary was made by Holdings III or a Restricted Subsidiary pursuant to clause (7) of Section 4.07(b) hereof or to the extent such Investment constituted a Permitted Investment.
- (b) The foregoing provisions of Section 4.07(a) hereof will not prohibit:
- (1) the payment of any dividend within 60 days after the date of declaration thereof, if at the date of declaration such payment would have complied with the provisions of this Indenture;

- (2) (a) the redemption, repurchase, retirement or other acquisition of any Equity Interests ("<u>Treasury Capital Stock</u>") or Subordinated Indebtedness of Holdings III or any Equity Interests of any direct or indirect parent company of Holdings III, in exchange for, or out of the proceeds of the substantially concurrent sale (other than to a Restricted Subsidiary) of, Equity Interests of Holdings III or any direct or indirect parent company of Holdings III to the extent contributed to Holdings III (in each case, other than any Disqualified Stock) ("<u>Refunding Capital Stock</u>") and (b) if immediately prior to the retirement of Treasury Capital Stock, the declaration and payment of dividends thereon was permitted under clause (6) of this Section 4.07(b), the declaration and payment of dividends on the Refunding Capital Stock (other than Refunding Capital Stock the proceeds of which were used to redeem, repurchase, retire or otherwise acquire any Equity Interests of any direct or indirect parent company of Holdings III) in an aggregate amount per year no greater than the aggregate amount of dividends per annum that were declarable and payable on such Treasury Capital Stock immediately prior to such retirement;
- (3) the defeasance, redemption, repurchase or other acquisition or retirement of Subordinated Indebtedness of Holdings III, the Issuer or a Subsidiary Guarantor made (i) with Excluded Proceeds or (ii) by exchange for, or out of the proceeds of the substantially concurrent sale of, new Indebtedness of Holdings III, the Issuer or a Subsidiary Guarantor, as the case may be, which is incurred in compliance with Section 4.09 hereof so long as, in the case of clause (ii):
 - (A) the principal amount of such new Indebtedness does not exceed the principal amount of (or accreted value, if applicable), plus any accrued and unpaid interest on, the Subordinated Indebtedness being so redeemed, repurchased, acquired or retired for value, plus the amount of any reasonable premium required to be paid under the terms of the instrument governing the Subordinated Indebtedness being so redeemed, repurchased, acquired or retired and any reasonable fees and expenses incurred in connection with the issuance of such new Indebtedness;
 - (B) such new Indebtedness is subordinated to the Notes or the applicable Guarantee at least to the same extent as such Subordinated Indebtedness so purchased, exchanged, redeemed, repurchased, acquired or retired for value;
 - (C) such new Indebtedness has a final scheduled maturity date equal to or later than the final scheduled maturity date of the Subordinated Indebtedness being so redeemed, repurchased, acquired or retired; and
 - (D) such new Indebtedness has a Weighted Average Life to Maturity equal to or greater than the remaining Weighted Average Life to Maturity of the Subordinated Indebtedness being so redeemed, repurchased, acquired or retired;

- (4) a Restricted Payment to pay for the repurchase, retirement or other acquisition or retirement for value of Equity Interests (other than Disqualified Stock) of Holdings III or any of its direct or indirect parent companies held by any future, present or former employee, director or consultant of Holdings III, any of its Subsidiaries or any of its direct or indirect parent companies pursuant to any management equity plan or stock option plan or any other management or employee benefit plan or agreement; provided, that the aggregate Restricted Payments made under this clause (4) do not exceed in any calendar year \$75.0 million (with unused amounts in any calendar year being carried over to succeeding calendar years subject to a maximum (without giving effect to the following proviso) of \$100.0 million in any calendar year); provided further that such amount in any calendar year may be increased by an amount not to exceed:
 - (A) the cash proceeds from the sale of Equity Interests (other than Disqualified Stock) of Holdings III and, to the extent contributed to Holdings III, Equity Interests of any of Holdings III's direct or indirect parent companies, in each case to members of management, directors or consultants of Holdings III, any of its Subsidiaries or any of its direct or indirect parent companies that occurs after the Measurement Date, to the extent the cash proceeds from the sale of such Equity Interests have not otherwise been applied to the payment of Restricted Payments by virtue of clause (3) of Section 4.07(a) hereof; <u>plus</u>
 - (B) the cash proceeds of key man life insurance policies received by Holdings III or its Restricted Subsidiaries after the Measurement Date; less
 - (C) the amount of any Restricted Payments made after the Measurement Date with the cash proceeds described in clauses (A) and (B) of this clause (4);

and <u>provided further</u> that cancellation of Indebtedness owing to Holdings III from members of management of Holdings III, any of Holdings III's direct or indirect parent companies or any of Holdings III's Restricted Subsidiaries in connection with a repurchase of Equity Interests of Holdings III or any of its direct or indirect parent companies will not be deemed to constitute a Restricted Payment for purposes of this Section 4.07 or any other provision of this Indenture;

(5) the declaration and payment of dividends to holders of any class or series of Disqualified Stock of Holdings III or any of its Restricted Subsidiaries or any class or series of Preferred Stock of any Restricted Subsidiary issued in accordance with Section 4.09 hereof to the extent such dividends are included in the definition of "Fixed Charges";

- (6) (A) the declaration and payment of dividends to holders of any class or series of Designated Preferred Stock (other than Disqualified Stock) issued by Holdings III after the Measurement Date;
 - (B) the declaration and payment of dividends to a direct or indirect parent company of Holdings III, the proceeds of which will be used to fund the payment of dividends to holders of any class or series of Designated Preferred Stock (other than Disqualified Stock) of such parent corporation issued after the Measurement Date, <u>provided</u> that the amount of dividends paid pursuant to this clause (B) shall not exceed the aggregate amount of cash actually contributed to Holdings III from the sale of such Designated Preferred Stock; or
 - (C) the declaration and payment of dividends on Refunding Capital Stock that is Preferred Stock in excess of the dividends declarable and payable thereon pursuant to clause (2) of this Section 4.07(b);
- provided, in the case of each of (A), (B) and (C) of this clause (6), that for the most recently ended four full fiscal quarters for which internal financial statements are available immediately preceding the date of issuance of such Designated Preferred Stock or the declaration of such dividends on Refunding Capital Stock that is Preferred Stock, after giving effect to such issuance or declaration on a pro forma basis, Holdings III and its Restricted Subsidiaries on a consolidated basis would have had a Fixed Charge Coverage Ratio of at least 2.00 to 1.00;
- (7) Investments in Unrestricted Subsidiaries having an aggregate fair market value, taken together with all other Investments made after the Measurement Date pursuant to this clause (7) that are at the time outstanding, without giving effect to the sale of an Unrestricted Subsidiary to the extent the proceeds of such sale do not consist of cash or marketable securities, not to exceed 2.0% of Total Assets at the time of such Investment (with the fair market value of each Investment being measured at the time made and without giving effect to subsequent changes in value);
- (8) repurchases of Equity Interests deemed to occur upon exercise of stock options or warrants if such Equity Interests represent a portion of the exercise price of such options or warrants;
- (9) the declaration and payment of dividends on Holdings III's common stock (or the payment of dividends to any direct or indirect parent entity to fund a payment of dividends on such entity's common stock), following the first public offering of Holdings III's common stock or the common stock of any of its direct or indirect parent companies after the Measurement Date, of up to 6.0% per annum of the net cash proceeds received by or contributed to Holdings III in or from any such public offering, other than public offerings with respect to Holdings III's common stock registered on Form S-4 or Form S-8 and other than any public sale constituting an Excluded Contribution;

- (10) Restricted Payments that are made with Excluded Contributions;
- (11) other Restricted Payments in an aggregate amount taken together with all other Restricted Payments made pursuant to this clause (11) not to exceed \$450.0 million;
 - (12) distributions or payments of Securitization Fees;
- (13) any Restricted Payment made in connection with the Transaction and the fees and expenses related thereto or owed to Affiliates, in each case to the extent permitted by Section 4.11 hereof;
- (14) the repurchase, redemption or other acquisition or retirement for value of any Subordinated Indebtedness pursuant to the provisions similar to those described under Section 4.10 and Section 4.14 hereof; <u>provided</u> that all Notes validly tendered by Holders in connection with a Change of Control Offer or Asset Sale Offer, as applicable, have been repurchased, redeemed or acquired for value;
- (15) the declaration and payment of dividends by Holdings III to, or the making of loans to, any direct or indirect parent in amounts required for any direct or indirect parent companies to pay, in each case without duplication,
 - (A) franchise and excise taxes and other fees, taxes and expenses required to maintain their corporate existence;
 - (B) foreign, federal, state and local income taxes, to the extent such income taxes are attributable to the income of Holdings III and its Restricted Subsidiaries and, to the extent of the amount actually received from its Unrestricted Subsidiaries, in amounts required to pay such taxes to the extent attributable to the income of such Unrestricted Subsidiaries; <u>provided</u> that in each case the amount of such payments in any fiscal year does not exceed the amount that Holdings III and its Restricted Subsidiaries would be required to pay in respect of foreign, federal, state and local taxes for such fiscal year were Holdings III, its Restricted Subsidiaries and its Unrestricted Subsidiaries (to the extent described above) to pay such taxes separately from any such parent entity;
 - (C) customary salary, bonus and other benefits payable to officers and employees of any direct or indirect parent company of Holdings III to the extent such salaries, bonuses and other benefits are attributable to the ownership or operation of Holdings III and its Restricted Subsidiaries;

- (D) general corporate operating and overhead costs and expenses of any direct or indirect parent company of Holdings III to the extent such costs and expenses are attributable to the ownership or operation of Holdings III and its Restricted Subsidiaries; and
 - (E) fees and expenses other than to Affiliates of Holdings III related to any unsuccessful equity or debt offering of such parent entity; and
- (16) the distribution, by dividend or otherwise, of shares of Capital Stock of, or Indebtedness owed to Holdings III or a Restricted Subsidiary by, Unrestricted Subsidiaries (other than Unrestricted Subsidiaries, the primary assets of which are cash and/or Cash Equivalents);

provided, that at the time of, and after giving effect to, any Restricted Payment permitted under clauses (11) and (16) of this Section 4.07(b), no Default shall have occurred and be continuing or would occur as a consequence thereof.

(c) As of the Issue Date, all of Holdings III's Subsidiaries, including Holdings IV, Holdings V and the Issuer, will be Restricted Subsidiaries. Holdings III shall not permit any Unrestricted Subsidiary to become a Restricted Subsidiary except pursuant to the last sentence of the definition of "Unrestricted Subsidiary." For purposes of designating any Restricted Subsidiary as an Unrestricted Subsidiary, all outstanding Investments by Holdings III and its Restricted Subsidiaries (except to the extent repaid) in the Subsidiary so designated will be deemed to be Restricted Payments in an amount determined as set forth in the last sentence of the definition of "Investments." Such designation will be permitted only if a Restricted Payment in such amount would be permitted at such time, whether pursuant to Section 4.07(a) hereof or under clause (7), (10) or (11) of Section 4.07(b) hereof, or pursuant to the definition of "Permitted Investments," and if such Subsidiary otherwise meets the definition of an Unrestricted Subsidiary. Unrestricted Subsidiaries will not be subject to any of the restrictive covenants set forth in this Indenture.

SECTION 4.08. Dividend and Other Payment Restrictions Affecting Restricted Subsidiaries.

- (a) Holdings III shall not, and shall not permit any of its Restricted Subsidiaries that are not Guarantors to, directly or indirectly, create or otherwise cause or suffer to exist or become effective any consensual encumbrance or consensual restriction on the ability of any such Restricted Subsidiary to:
 - (1) (A) pay dividends or make any other distributions to Holdings III or any of its Restricted Subsidiaries on its Capital Stock or with respect to any other interest or participation in, or measured by, its profits, or

- (B) pay any Indebtedness owed to Holdings III or any of its Restricted Subsidiaries;
- (2) make loans or advances to Holdings III or any of its Restricted Subsidiaries; or
- (3) sell, lease or transfer any of its properties or assets to Holdings III or any of its Restricted Subsidiaries.
- (b) The restrictions in Section 4.08(a) hereof shall not apply to encumbrances or restrictions existing under or by reason of:
- (1) contractual encumbrances or restrictions in effect on the Issue Date, including pursuant to the Senior Credit Facilities and the related documentation, Hedging Obligations, the indentures governing the Existing Secured Notes and the related documentation, the indentures governing the Existing Senior Subordinated Notes and the related documentation and the indentures governing the Old Notes and the related documentation;
 - (2) this Indenture and the Notes;
- (3) purchase money obligations for property acquired in the ordinary course of business that impose restrictions of the nature discussed in clause (3) of Section 4.08(a) hereof on the property so acquired;
 - (4) applicable law or any applicable rule, regulation or order;
- (5) any agreement or other instrument of a Person acquired by Holdings III or any of its Restricted Subsidiaries in existence at the time of such acquisition or at the time it merges or amalgamates with or into Holdings III or any of its Restricted Subsidiaries or assumed in connection with the acquisition of assets from such Person (but, in any such case, not created in contemplation thereof), which encumbrance or restriction is not applicable to any Person, or the properties or assets of any Person, other than the Person and its Subsidiaries, or the property or assets of the Person and its Subsidiaries, so acquired or the property or assets so assumed;
- (6) contracts for the sale of assets, including customary restrictions with respect to a Subsidiary of Holdings III pursuant to an agreement that has been entered into for the sale or disposition of all or substantially all of the Capital Stock or assets of such Subsidiary;
- (7) Secured Indebtedness otherwise permitted to be incurred pursuant to Section 4.09 hereof and Section 4.12 hereof that limit the right of the debtor to dispose of the assets securing such Indebtedness;

- (8) restrictions on cash or other deposits or net worth imposed by customers under contracts entered into in the ordinary course of business;
- (9) other Indebtedness, Disqualified Stock or Preferred Stock of Foreign Subsidiaries permitted to be incurred subsequent to the Issue Date pursuant to the provisions of Section 4.09 hereof;
 - (10) customary provisions in joint venture agreements and other similar agreements relating solely to such joint venture;
- (11) customary provisions contained in leases, licenses or similar agreements, including with respect to intellectual property and other agreements, in each case, entered into in the ordinary course of business;
- (12) any encumbrances or restrictions of the type referred to in clauses (1), (2) and (3) of Section 4.08(a) hereof imposed by any amendments, modifications, restatements, renewals, increases, supplements, refundings, replacements or refinancings of the contracts, instruments or obligations referred to in clauses (1) through (11) of this Section 4.08(b); provided that such amendments, modifications, restatements, renewals, increases, supplements, refundings, replacements or refinancings are, in the good faith judgment of Holdings III, no more restrictive with respect to such encumbrance and other restrictions taken as a whole than those prior to such amendment, modification, restatement, renewal, increase, supplement, refunding, replacement or refinancing; and
- (13) restrictions created in connection with any Qualified Securitization Facility that, in the good faith determination of Holdings III, are necessary or advisable to effect such Qualified Securitization Facility.

SECTION 4.09. <u>Limitation on Incurrence of Indebtedness and Issuance of Disqualified Stock and Preferred Stock.</u>

(a) Holdings III shall not, and shall not permit any of its Restricted Subsidiaries to, directly or indirectly, create, incur, issue, assume, guarantee or otherwise become directly or indirectly liable, contingently or otherwise (collectively, "incur" and collectively, an "incurrence") with respect to any Indebtedness (including Acquired Indebtedness) and Holdings III will not issue any shares of Disqualified Stock and will not permit any Restricted Subsidiary to issue any shares of Disqualified Stock or Preferred Stock; provided, that Holdings III may incur Indebtedness (including Acquired Indebtedness) or issue shares of Disqualified Stock, and, subject to Section 4.09(c) hereof, any Restricted Subsidiary may incur Indebtedness (including Acquired Indebtedness), issue shares of Disqualified Stock and issue shares of Preferred Stock, if the Fixed Charge Coverage Ratio on a consolidated basis for Holdings III and its Restricted Subsidiaries' most recently ended four fiscal quarters for which internal financial statements are available immediately preceding the date on which such additional Indebtedness is incurred or such Disqualified Stock or Preferred Stock is

issued would have been at least 2.00 to 1.00 (the "<u>Fixed Charge Coverage Test</u>"), determined on a <u>pro forma</u> basis (including a <u>pro forma</u> application of the net proceeds therefrom), as if the additional Indebtedness had been incurred, or the Disqualified Stock or Preferred Stock had been issued, as the case may be, and the application of proceeds therefrom had occurred at the beginning of such four-quarter period.

- (b) The provisions of Section 4.09(a) hereof shall not apply to:
- (1) the incurrence of Indebtedness under Credit Facilities by Holdings III, the Issuer or any other Restricted Subsidiary and the issuance and creation of letters of credit and bankers' acceptances thereunder (with letters of credit and bankers' acceptances being deemed to have a principal amount equal to the face amount thereof), up to an aggregate principal amount, when taken together with the aggregate principal amount (or, if issued with original issue discount, the accreted value) of Existing Secured Notes and Notes then outstanding, of \$5,250.0 million outstanding at any one time;
- (2) the incurrence by the Issuer and any Guarantor of Indebtedness represented by the Notes (not including any Additional Notes), including any Guarantee of the Notes;
- (3) Indebtedness of Holdings III and its Subsidiaries in existence on the Issue Date (other than Indebtedness described in clauses (1) and (2) of this Section 4.09(b));
- (4) Indebtedness (including Capitalized Lease Obligations), Disqualified Stock and Preferred Stock incurred by Holdings III or any of its Restricted Subsidiaries, to finance the purchase, lease or improvement of property (real or personal) or equipment that is used or useful in a Similar Business, whether through the direct purchase of assets or the Capital Stock of any Person owning such assets in an aggregate principal amount, together with any Refinancing Indebtedness in respect thereof and all other Indebtedness, Disqualified Stock and/or Preferred Stock issued and outstanding under this clause (4), not to exceed 4.0% of Total Assets at any time outstanding; so long as such Indebtedness exists at the date of such purchase, lease or improvement or is created within 270 days thereafter;
- (5) Indebtedness incurred by Holdings III or any of its Restricted Subsidiaries constituting reimbursement obligations with respect to letters of credit issued in the ordinary course of business, including letters of credit in respect of workers' compensation claims, or other Indebtedness with respect to reimbursement type obligations regarding workers' compensation claims; <u>provided</u>, that upon the drawing of such letters of credit or the incurrence of such Indebtedness, such obligations are reimbursed within 30 days following such drawing or incurrence;

- (6) Indebtedness arising from agreements of Holdings III or its Restricted Subsidiaries providing for indemnification, adjustment of purchase price, earnouts or similar obligations, in each case, incurred or assumed in connection with the disposition of any business, assets or a Subsidiary, other than guarantees of Indebtedness incurred by any Person acquiring all or any portion of such business, assets or a Subsidiary for the purpose of financing such acquisition; provided, that
 - (A) such Indebtedness is not reflected on the balance sheet of Holdings III or any of its Restricted Subsidiaries (contingent obligations referred to in a footnote to financial statements and not otherwise reflected on the balance sheet will not be deemed to be reflected on such balance sheet for purposes of this clause (6)(a)); and
 - (B) the maximum assumable liability in respect of all such Indebtedness shall at no time exceed the gross proceeds including non-cash proceeds (the fair market value of such non-cash proceeds being measured at the time received and without giving effect to any subsequent changes in value) actually received by Holdings III and its Restricted Subsidiaries in connection with such disposition;
- (7) Indebtedness of Holdings III to a Restricted Subsidiary; <u>provided</u> that any such Indebtedness owing to a Restricted Subsidiary that is not a Guarantor (other than the Issuer) is expressly subordinated in right of payment to the Notes; <u>provided further</u> that any subsequent issuance or transfer of any Capital Stock or any other event which results in any Restricted Subsidiary ceasing to be a Restricted Subsidiary or any other subsequent transfer of any such Indebtedness (except to Holdings III or another Restricted Subsidiary) shall be deemed, in each case, to be an incurrence of such Indebtedness;
- (8) Indebtedness of a Restricted Subsidiary to Holdings III or another Restricted Subsidiary; <u>provided</u> that if a Guarantor incurs such Indebtedness to a Restricted Subsidiary that is not a Guarantor (other than the Issuer), such Indebtedness is expressly subordinated in right of payment to the Guarantee of the Notes of such Guarantor; <u>provided further</u> that any subsequent transfer of any such Indebtedness (except to Holdings III or another Restricted Subsidiary) shall be deemed, in each case, to be an incurrence of such Indebtedness;
- (9) shares of Preferred Stock of a Restricted Subsidiary issued to Holdings III or another Restricted Subsidiary; <u>provided</u> that any subsequent issuance or transfer of any Capital Stock or any other event which results in any such Restricted Subsidiary ceasing to be a Restricted Subsidiary or any other subsequent transfer of any such shares of Preferred Stock (except to Holdings III or another of its Restricted Subsidiaries) shall be deemed in each case to be an issuance of such shares of Preferred Stock;

- (10) Hedging Obligations (excluding Hedging Obligations entered into for speculative purposes) for the purpose of limiting interest rate risk with respect to any Indebtedness permitted to be incurred pursuant to this Section 4.09, exchange rate risk or commodity pricing risk;
- (11) obligations in respect of performance, bid, appeal and surety bonds and completion guarantees provided by Holdings III or any of its Restricted Subsidiaries in the ordinary course of business;
- (12) (a) Indebtedness or Disqualified Stock of Holdings III and Indebtedness, Disqualified Stock or Preferred Stock of Holdings III or any Restricted Subsidiary equal to 200.0% of the net cash proceeds received by Holdings III since immediately after the Transaction Date from the issue or sale of Equity Interests of Holdings III or cash contributed to the capital of Holdings III (in each case, other than proceeds of Disqualified Stock or sales of Equity Interests to Holdings III or any of its Subsidiaries) as determined in accordance with clauses (3)(B) and (3)(C) of Section 4.07(a) hereof to the extent such net cash proceeds or cash have not been applied pursuant to such clauses to make Restricted Payments or to make other Investments, payments or exchanges pursuant to Section 4.07(b) hereof or to make Permitted Investments (other than Permitted Investments specified in clauses (1) and (3) of the definition thereof) and (b) Indebtedness or Disqualified Stock of Holdings III and Indebtedness, Disqualified Stock or Preferred Stock of Holdings III or, subject to Section 4.09(c) hereof, any Restricted Subsidiary not otherwise permitted hereunder in an aggregate principal amount or liquidation preference, which when aggregated with the principal amount and liquidation preference of all other Indebtedness, Disqualified Stock and Preferred Stock then outstanding and incurred pursuant to this clause (12)(b), does not at any one time outstanding exceed \$900.0 million (it being understood that any Indebtedness, Disqualified Stock or Preferred Stock incurred pursuant to this clause (12)(b) shall cease to be deemed incurred or outstanding for purposes of this clause (12)(b) but shall be deemed incurred for the purposes of Section 4.09(a) hereof from and after the first date on which Holdings III or such Restricted Subsidiary could have incurred such Indebtedness, Disqualified Stock or Preferred Stock under Section 4.09(a) hereof without reliance on this clause (12)(b));
- (13) the incurrence by Holdings III or any Restricted Subsidiary, of Indebtedness, Disqualified Stock or Preferred Stock which serves to refund or refinance any Indebtedness, Disqualified Stock or Preferred Stock incurred as permitted under Section 4.09(a) hereof and clauses (2), (3), (4) and (12) (a) of this Section 4.09(b), this clause (13) and clause (14) of this Section 4.09(b) or any Indebtedness, Disqualified Stock or Preferred Stock including additional Indebtedness, Disqualified Stock or Preferred Stock incurred to pay premiums (including reasonable tender premiums), defeasance costs and fees in connection therewith (the "Refinancing Indebtedness") prior to its respective maturity; provided, that such Refinancing Indebtedness:

- (A) has a Weighted Average Life to Maturity at the time such Refinancing Indebtedness is incurred which is not less than the remaining Weighted Average Life to Maturity of, the Indebtedness, Disqualified Stock or Preferred Stock being refunded or refinanced,
- (B) to the extent such Refinancing Indebtedness refinances (i) Indebtedness subordinated or <u>pari passu</u> to the Notes or any Guarantee thereof, such Refinancing Indebtedness is subordinated or <u>pari passu</u> to the Notes or the Guarantee at least to the same extent as the Indebtedness being refinanced or refunded or (ii) Disqualified Stock or Preferred Stock, such Refinancing Indebtedness must be Disqualified Stock or Preferred Stock, respectively,
- (C) in the case of any Refinancing Indebtedness in respect of Indebtedness under the Notes, the Existing Senior Notes, the Existing Senior Subordinated Notes or the Existing Secured Notes, or Refinancing Indebtedness of any of the foregoing, such Refinancing Indebtedness shall not be required to be incurred substantially contemporaneously with the related refinancing of such Notes, Existing Senior Notes, Existing Senior Subordinated Notes or Existing Secured Note, or Refinancing Indebtedness of any of the foregoing, as applicable; provided that any portion of the net proceeds of such Refinancing Indebtedness that is not applied to the repayment or prepayment of such Notes, Existing Senior Notes, Existing Senior Subordinated Notes or Existing Secured Note, or Refinancing Indebtedness of any of the foregoing, as applicable, within 45 days following the incurrence of such Refinancing Indebtedness shall not constitute Refinancing Indebtedness in respect of such Notes, Existing Senior Notes, Existing Senior Subordinated Notes or Existing Secured Note, or Refinancing Indebtedness of any of the foregoing, as applicable, and

(D) shall not include:

- (i) Indebtedness, Disqualified Stock or Preferred Stock of a Subsidiary of Holdings III that is not a Guarantor (other than the Issuer) that refinances Indebtedness, Disqualified Stock or Preferred Stock of Holdings III or the Issuer;
- (ii) Indebtedness, Disqualified Stock or Preferred Stock of a Subsidiary of Holdings III that is not a Guarantor (other than the Issuer) that refinances Indebtedness, Disqualified Stock or Preferred Stock of a Guarantor or the Issuer; or

- (iii) Indebtedness, Disqualified Stock or Preferred Stock of Holdings III or a Restricted Subsidiary that refinances Indebtedness, Disqualified Stock or Preferred Stock of an Unrestricted Subsidiary;
- (14) Indebtedness, Disqualified Stock or Preferred Stock of (x) Holdings III or, subject to Section 4.09(c) hereof, a Restricted Subsidiary incurred to finance an acquisition or (y) Persons that are acquired by Holdings III or any Restricted Subsidiary or merged or amalgamated into Holdings III or a Restricted Subsidiary in accordance with the terms of this Indenture; <u>provided</u> that after giving effect to such acquisition, merger or amalgamation either
 - (A) Holdings III would be permitted to incur at least \$1.00 of additional Indebtedness pursuant to the Fixed Charge Coverage Test set forth in Section 4.09(a) hereof, or
 - (B) the Fixed Charge Coverage Ratio of Holdings III and the Restricted Subsidiaries is equal to or greater than immediately prior to such acquisition, merger or amalgamation;
- (15) Indebtedness arising from the honoring by a bank or other financial institution of a check, draft or similar instrument drawn against insufficient funds in the ordinary course of business, provided that such Indebtedness is extinguished within five Business Days of its incurrence;
- (16) Indebtedness of Holdings III or any of its Restricted Subsidiaries supported by a letter of credit issued pursuant to the Credit Facilities, in a principal amount not in excess of the stated amount of such letter of credit;
- (17) (A) any guarantee by Holdings III or a Restricted Subsidiary of Indebtedness or other obligations of any Restricted Subsidiary so long as the incurrence of such Indebtedness incurred by such Restricted Subsidiary is permitted under the terms of this Indenture, or
- (B) any guarantee by a Restricted Subsidiary of Indebtedness of the Issuer; <u>provided</u> that such guarantee is incurred in accordance with Section 4.15 hereof;
- (18) Indebtedness consisting of Indebtedness issued by Holdings III or any of its Restricted Subsidiaries to current or former officers, directors and employees thereof, their respective estates, spouses or former spouses, in each case to finance the purchase or redemption of Equity Interests of Holdings III or any direct or indirect parent company of Holdings III to the extent described in clause (4) of Section 4.07(b) hereof.

- (19) customer deposits and advance payments received in the ordinary course of business from customers for goods purchased in the ordinary course of business;
- (20) Indebtedness owed on a short-term basis of no longer than 30 days to banks and other financial institutions incurred in the ordinary course of business of Holdings III and its Restricted Subsidiaries with such banks or financial institutions that arises in connection with ordinary banking arrangements to manage cash balances of Holdings III and its Restricted Subsidiaries;
- (21) Indebtedness incurred by a Restricted Subsidiary in connection with bankers' acceptances, discounted bills of exchange or the discounting or factoring of receivables for credit management purposes, in each case incurred or undertaken in the ordinary course of business on arm's length commercial terms on a recourse basis; and
- (22) Indebtedness of Holdings III or any of its Restricted Subsidiaries consisting of (i) the financing of insurance premiums or (ii) take-or-pay obligations contained in supply arrangements in each case, incurred in the ordinary course of business.
- (c) Restricted Subsidiaries of Holdings III that are not Guarantors (other than the Issuer) may not incur Indebtedness or Disqualified Stock or Preferred Stock under Section 4.09(a) hereof or clause 12(b) or 14(x) of Section 4.09(b) hereof if, after giving <u>pro forma</u> effect to such incurrence or issuance (including a <u>pro forma</u> application of the net proceeds therefrom), the aggregate amount of Indebtedness and Disqualified Stock and Preferred Stock of Restricted Subsidiaries that are not Guarantors (other than the Issuer) incurred or issued pursuant to Section 4.09(a) hereof and clauses 12(b) and 14(x) of Section 4.09(b) hereof, collectively, would exceed \$1,250.0 million.
 - (d) For purposes of determining compliance with this Section 4.09:
- (1) in the event that an item of Indebtedness, Disqualified Stock or Preferred Stock (or any portion thereof) meets the criteria of more than one of the categories of Permitted Indebtedness, Disqualified Stock or Preferred Stock described in clauses (1) through (22) of Section 4.09(b) hereof or is entitled to be incurred pursuant to Section 4.09(a) hereof, Holdings III, in its sole discretion, will classify or reclassify such item of Indebtedness, Disqualified Stock or Preferred Stock (or any portion thereof) and will only be required to include the amount and type of such Indebtedness, Disqualified Stock or Preferred Stock in one of the above clauses or under Section 4.09(a) hereof; provided that all Indebtedness outstanding under the Senior Credit Facilities on the Issue Date will be treated as incurred on the Issue Date under clause (1) of Section 4.09(b) hereof; and

(2) at the time of incurrence, Holdings III will be entitled to divide and classify an item of Indebtedness in more than one of the types of Indebtedness described in Section 4.09(a) and Section 4.09(b) hereof.

Accrual of interest or dividends, the accretion of accreted value, the accretion or amortization of original issue discount and the payment of interest or dividends in the form of additional Indebtedness, Disqualified Stock or Preferred Stock, as the case may be, of the same class will not be deemed to be an incurrence of Indebtedness, Disqualified Stock or Preferred Stock for purposes of this Section 4.09.

For purposes of determining compliance with any U.S. dollar-denominated restriction on the incurrence of Indebtedness, the U.S. dollar-equivalent principal amount of Indebtedness denominated in a foreign currency shall be calculated based on the relevant currency exchange rate in effect on the date such Indebtedness was incurred, in the case of term debt, or first committed, in the case of revolving credit debt; <u>provided</u> that if such Indebtedness is incurred to refinance other Indebtedness denominated in a foreign currency, and such refinancing would cause the applicable U.S. dollar denominated restriction to be exceeded if calculated at the relevant currency exchange rate in effect on the date of such refinancing, such U.S. dollar-denominated restriction shall be deemed not to have been exceeded so long as the principal amount of such refinancing Indebtedness does not exceed the principal amount of such Indebtedness being refinanced.

The principal amount of any Indebtedness incurred to refinance other Indebtedness, if incurred in a different currency from the Indebtedness being refinanced, shall be calculated based on the currency exchange rate applicable to the currencies in which such respective Indebtedness is denominated that is in effect on the date of such refinancing.

Notwithstanding anything to the contrary, Holdings III shall not, and shall not permit any Guarantor or the Issuer to, directly or indirectly, incur any Indebtedness (including Acquired Indebtedness) that is subordinated or junior in right of payment to any Indebtedness of Holdings III, such Guarantor or the Issuer, as the case may be, unless such Indebtedness is expressly subordinated in right of payment to the Notes or Holdings III's or such Guarantor's Guarantee to the extent and in the same manner as such Indebtedness is subordinated to other Indebtedness of Holdings III, such Guarantor or the Issuer, as the case may be. For the purposes of this Indenture, Indebtedness that is unsecured is not deemed to be subordinated or junior to Secured Indebtedness merely because it is unsecured, and Senior Indebtedness is not deemed to be subordinated or junior to any other Senior Indebtedness merely because it has a junior priority with respect to the same collateral.

SECTION 4.10. Asset Sales.

(a) Holdings III shall not, and shall not permit any of its Restricted Subsidiaries to, cause, make or suffer to exist an Asset Sale, unless:

- (1) Holdings III or such Restricted Subsidiary, as the case may be, receives consideration at the time of such Asset Sale at least equal to the fair market value of the assets sold or otherwise disposed of; and
- (2) except in the case of a Permitted Asset Swap, at least 75% of the consideration therefor received by Holdings III or such Restricted Subsidiary, as the case may be, is in the form of cash or Cash Equivalents; <u>provided</u> that the amount of:
 - (A) any liabilities (as shown on Holdings III's or such Restricted Subsidiary's most recent balance sheet or in the footnotes thereto) of Holdings III or such Restricted Subsidiary, other than liabilities that are by their terms subordinated to the Notes, that are assumed by the transferee of any such assets and for which Holdings III and all of its Restricted Subsidiaries have been validly released by all creditors in writing,
 - (B) any securities received by Holdings III or such Restricted Subsidiary from such transferee that are converted by Holdings III or such Restricted Subsidiary into cash (to the extent of the cash received) within 180 days following the closing of such Asset Sale, and
 - (C) any Designated Non-cash Consideration received by Holdings III or such Restricted Subsidiary in such Asset Sale having an aggregate fair market value, taken together with all other Designated Non-cash Consideration received pursuant to this clause (c) that is at that time outstanding, not to exceed 2.5% of Total Assets at the time of the receipt of such Designated Non-cash Consideration, with the fair market value of each item of Designated Non-cash Consideration being measured at the time received and without giving effect to subsequent changes in value,

shall be deemed to be cash for purposes of this provision and for no other purpose.

- (b) Within 450 days after the receipt of any Net Proceeds of any Asset Sale, Holdings III or such Restricted Subsidiary, at its option, may apply the Net Proceeds from such Asset Sale,
 - (1) to permanently reduce:
 - (A) First Lien Obligations (including Obligations under the Senior Credit Facilities and the Existing Secured Notes), and to correspondingly reduce commitments with respect thereto;
 - (B) Obligations under Senior Indebtedness that is secured by a Lien, which Lien is permitted by this Indenture, and to correspondingly reduce commitments with respect thereto; or

- (C) Indebtedness of a Restricted Subsidiary that is not a Guarantor, other than Indebtedness owed to Holdings III or another Restricted Subsidiary;
- (2) to make (a) an Investment in any one or more businesses, <u>provided</u> that such Investment in any business is in the form of the acquisition of Capital Stock and results in Holdings III or another of its Restricted Subsidiaries, as the case may be, owning an amount of the Capital Stock of such business such that it constitutes a Restricted Subsidiary, (b) capital expenditures or (c) acquisitions of other assets, in each of (a), (b) and (c), used or useful in a Similar Business, or
- (3) to make an investment in (a) any one or more businesses, <u>provided</u> that such investment in any business is in the form of the acquisition of Capital Stock and results in Holdings III or another of its Restricted Subsidiaries, as the case may be, owning an amount of the Capital Stock of such business such that it constitutes a Restricted Subsidiary, (b) properties or (c) acquisitions of other assets that, in each of (a), (b) and (c), replace the businesses, properties and/or assets that are the subject of such Asset Sale;

provided that, in the case of clauses (2) and (3) above, a binding commitment shall be treated as a permitted application of the Net Proceeds from the date of such commitment so long as Holdings III or such other Restricted Subsidiary enters into such commitment with the good faith expectation that such Net Proceeds will be applied to satisfy such commitment within 180 days of such commitment (an "Acceptable Commitment") and, in the event any Acceptable Commitment is later cancelled or terminated for any reason before the Net Proceeds are applied in connection therewith, Holdings III or such Restricted Subsidiary enters into another Acceptable Commitment (a "Second Commitment") within 180 days of such cancellation or termination; provided further that if any Second Commitment is later cancelled or terminated for any reason before such Net Proceeds are applied, then such Net Proceeds shall constitute Excess Proceeds.

(c) Any Net Proceeds from the Asset Sale that are not invested or applied as provided and within the time period set forth in Section 4.10(b) hereof will be deemed to constitute "Excess Proceeds." When the aggregate amount of Excess Proceeds exceeds \$100.0 million, the Issuer shall make an offer to all Holders of the Notes and, if required by the terms of any other Indebtedness constituting First Lien Obligations, to the holders of such other First Lien Obligations (an "Asset Sale Offer"), to purchase the maximum aggregate principal amount of the Notes and such other First Lien Obligations that is at least \$2,000 or an integral multiple of \$1,000 thereafter that may be purchased out of the Excess Proceeds at an offer price in cash in an amount equal to 100% of the principal amount thereof (or accreted value, if less), plus accrued and unpaid interest, if any, to the date fixed for the closing of such offer, in accordance with the procedures set forth in this Indenture. The Issuer will commence an Asset Sale Offer with respect to Excess Proceeds within ten Business Days after the date that Excess Proceeds exceed \$100.0 million by sending the notice required pursuant to the terms of this Indenture,

with a copy to the Trustee. The Issuer may satisfy the foregoing obligations with respect to any Net Proceeds from an Asset Sale by making an Asset Sale Offer with respect to such Net Proceeds prior to the expiration of the relevant 450 days or with respect to Excess Proceeds of \$100.0 million or less.

To the extent that the aggregate amount of Notes and such other First Lien Obligations tendered pursuant to an Asset Sale Offer is less than the Excess Proceeds, the Issuer may use any remaining Excess Proceeds for general corporate purposes, subject to other covenants contained in this Indenture. If the aggregate principal amount of Notes or the other First Lien Obligations surrendered by such holders thereof exceeds the amount of Excess Proceeds, the Trustee shall select the Notes and such other First Lien Obligations to be purchased on a <u>pro rata</u> basis based on the accreted value or principal amount of the Notes or such other First Lien Obligations tendered. Upon completion of any such Asset Sale Offer, the amount of Excess Proceeds that resulted in the Asset Sale Offer shall be reset to zero.

- (d) Pending the final application of any Net Proceeds pursuant to this Section 4.10, the holder of such Net Proceeds may apply such Net Proceeds temporarily to reduce Indebtedness outstanding under a revolving credit facility or otherwise invest such Net Proceeds in any manner not prohibited by this Indenture.
- (e) The Issuer will comply with the requirements of Rule 14e-1 under the Exchange Act and any other securities laws and regulations thereunder to the extent such laws or regulations are applicable in connection with the repurchase of the Notes pursuant to an Asset Sale Offer. To the extent that the provisions of any securities laws or regulations conflict with the provisions of this Indenture, the Issuer will comply with the applicable securities laws and regulations and shall not be deemed to have breached its obligations described in this Indenture by virtue thereof.
- SECTION 4.11. <u>Transactions with Affiliates.</u> (a) Holdings III will not, and will not permit any of its Restricted Subsidiaries to, make any payment to, or sell, lease, transfer or otherwise dispose of any of its properties or assets to, or purchase any property or assets from, or enter into or make or amend any transaction, contract, agreement, understanding, loan, advance or guarantee with, or for the benefit of, any Affiliate of Holdings III (each of the foregoing, an "<u>Affiliate Transaction</u>") involving aggregate payments or consideration in excess of \$25.0 million, unless:
 - (1) such Affiliate Transaction is on terms that are not materially less favorable to Holdings III or its relevant Restricted Subsidiary than those that would have been obtained in a comparable transaction by Holdings III or such Restricted Subsidiary with an unrelated Person on an arm's-length basis; and
 - (2) the Issuer delivers to the Trustee with respect to any Affiliate Transaction or series of related Affiliate Transactions involving aggregate payments or consideration in excess of \$60.0 million, a resolution adopted by the majority of the board of directors of the Issuer approving such Affiliate Transaction and set forth in an Officer's Certificate certifying that such Affiliate Transaction complies with clause (1) of this Section 4.11(a).

- (b) The provisions of Section 4.11(a) will not apply to the following:
- (1) transactions between or among Holdings III or any of its Restricted Subsidiaries;
- (2) Restricted Payments permitted by Section 4.07 hereof and the definition of "Permitted Investments";
- (3) [intentionally omitted];
- (4) the payment of reasonable and customary fees paid to, and indemnities provided for the benefit of, current or former officers, directors, employees or consultants of Holdings III, any of its direct or indirect parent companies or any of its Restricted Subsidiaries;
- (5) transactions in which Holdings III or any of its Restricted Subsidiaries, as the case may be, delivers to the Trustee a letter from an Independent Financial Advisor stating that such transaction is fair to Holdings III or such Restricted Subsidiary from a financial point of view or stating that the terms are not materially less favorable to Holdings III or its relevant Restricted Subsidiary than those that would have been obtained in a comparable transaction by Holdings III or such Restricted Subsidiary with an unrelated Person on an arm's-length basis;
- (6) any agreement as in effect as of the Issue Date, or any amendment thereto (so long as any such amendment is not disadvantageous to the Holders when taken as a whole as compared to the applicable agreement as in effect on the Issue Date);
- (7) the existence of, or the performance by Holdings III or any of its Restricted Subsidiaries of its obligations under the terms of, any stockholders agreement (including any registration rights agreement or purchase agreement related thereto) to which it is a party as of the Issue Date and any similar agreements which it may enter into thereafter; <u>provided</u>, that the existence of, or the performance by Holdings III or any of its Restricted Subsidiaries of obligations under any future amendment to any such existing agreement or under any similar agreement entered into after the Issue Date shall only be permitted by this clause (7) to the extent that the terms of any such amendment or new agreement are not otherwise disadvantageous to the Holders when taken as a whole;
 - (8) the Transaction and the payment of all fees and expenses related to the Transaction;

- (9) transactions with customers, clients, suppliers, or purchasers or sellers of goods or services that are Affiliates, in each case in the ordinary course of business and otherwise in compliance with the terms of this Indenture which are fair to Holdings III and its Restricted Subsidiaries, in the reasonable determination of the board of directors of Holdings III or the senior management thereof, or are on terms at least as favorable as might reasonably have been obtained at such time from an unaffiliated party;
- (10) the issuance of Equity Interests (other than Disqualified Stock) of Holdings III to any Permitted Holder or to any director, officer, employee or consultant of Holdings III, any of its direct or indirect parent companies or any of its Restricted Subsidiaries;
- (11) sales of accounts receivable, or participations therein, or Securitization Assets or related assets in connection with any Qualified Securitization Facility;
- (12) payments by Holdings III or any of its Restricted Subsidiaries to any of the Investors made for any financial advisory, financing, underwriting or placement services or in respect of other investment banking activities, including, without limitation, in connection with acquisitions or divestitures which payments are approved by a majority of the board of directors of Holdings III in good faith;
- (13) payments or loans (or cancellation of loans) to employees or consultants of Holdings III, any of its direct or indirect parent companies or any of its Restricted Subsidiaries and employment agreements, stock option plans and other similar arrangements with such employees or consultants which, in each case, are approved by a majority of the board of directors of Holdings III in good faith;
- (14) investments by any of the Investors in securities of Holdings III or any of its Restricted Subsidiaries (and payment of reasonable out-of-pocket expenses incurred by such investors in connection therewith) so long as (i) the investment is being offered generally to other investors on the same or more favorable terms and (ii) the investment constitutes less than 5% of the proposed or outstanding issue amount of such class of securities; and
- (15) any transactions with respect to the Issuer's jointly funded alliance with respect to the 300 millimeter wafer fabrication in Crolles, France, as in effect on the Transaction Date, and any amendment, modification or restructuring thereof, or any successor or replacement alliance or arrangement with respect thereto, or any additional alliance or arrangement with respect to 300 millimeter or larger wafer fabrication (in each case whether or not located in Crolles, France) which successor or replacement alliance or arrangement is otherwise permitted under this Indenture.

SECTION 4.12. <u>Liens.</u> Holdings III shall not, and shall not permit the Issuer, Holdings IV, Holdings V or any Subsidiary Guarantor to, directly or indirectly, create, incur, assume or suffer to exist any Lien that secures obligations under any Indebtedness or any related guarantee (the "<u>Initial Lien</u>"), on any asset or property of Holdings III, the Issuer, Holdings IV, Holdings V or any Subsidiary Guarantor, or any income or profits therefrom, or assign or convey any right to receive income therefrom, except:

- (1) in the case of any Initial Lien on any Collateral, such Initial Lien if such Initial Lien is a Permitted Lien; and
- (2) in the case of any Initial Lien on any asset or property not constituting or required to become Collateral, such Initial Lien if (a) the Notes and Guarantees are equally and ratably secured with (or on a senior basis to, in the case such Initial Lien secures any Subordinated Indebtedness) the Obligations secured by such Initial Lien, or (b) such Initial Lien is a Permitted Lien.

Any Lien created for the benefit of the Holders pursuant to clause (2) of this Section 4.12 shall provide by its terms that such Lien shall be automatically and unconditionally released and discharged upon the release and discharge of the Initial Lien which release and discharge in the case of any sale of any such asset or property shall not affect any Lien that the Trustee, the Collateral Agent or any other Authorized Representative may have on the proceeds from such sale.

If the Issuer or any Guarantor creates any additional Lien upon any property or assets to secure any First Lien Obligations, it must concurrently grant a First Lien upon such property or assets as security for the Notes or the applicable Guarantee of the Notes such that the property or assets subject to such Lien becomes Collateral subject to the First Lien, except to the extent such property constitutes cash or cash equivalents required to secure only letter of credit obligations under the Senior Credit Facilities.

SECTION 4.13. <u>Company Existence</u>. Subject to Article 5 hereof, Holdings III shall do or cause to be done all things necessary to preserve and keep in full force and effect (i) its company existence, and the corporate, partnership or other existence of each of its Restricted Subsidiaries, in accordance with the respective organizational documents (as the same may be amended from time to time) of Holdings III or any such Restricted Subsidiary and (ii) the rights (charter and statutory), licenses and franchises of Holdings III and its Restricted Subsidiaries; <u>provided</u> that Holdings III shall not be required to preserve any such right, license or franchise, or the corporate, partnership or other existence of any of its Restricted Subsidiaries (other than the Issuer), if Holdings III in good faith shall determine that the preservation thereof is no longer desirable in the conduct of the business of Holdings III and its Restricted Subsidiaries, taken as a whole.

SECTION 4.14. Offer to Repurchase Upon Change of Control. If a Change of Control occurs, unless the Issuer has previously or concurrently transmitted a redemption notice with respect to all the outstanding Notes as described under Section 3.07 hereof, the Issuer shall make an offer to purchase all of the Notes pursuant to the offer described below (the "Change of Control Offer") at a price in cash (the "Change of Control Payment") equal to 101% of the aggregate principal amount thereof plus accrued and unpaid interest, if any, to the date of purchase, subject to the right of Holders of the Notes of record on the relevant Record Date to receive interest due on the relevant Interest Payment Date. Within 30 days following any Change of Control, the Issuer shall send notice of such Change of Control Offer by first-class mail, with a copy to the Trustee, or otherwise transmit to each Holder of Notes to the address of such Holder appearing in the Note Register or otherwise in accordance with Applicable Procedures, with a copy to the Trustee, with the following information:

- (1) that a Change of Control Offer is being made pursuant to this Section 4.14 and that all Notes properly tendered pursuant to such Change of Control Offer will be accepted for payment by the Issuer;
- (2) the purchase price and the purchase date, which will be no earlier than 30 days nor later than 60 days from the date such notice is sent (the "<u>Change of Control Payment Date</u>");
 - (3) that any Note not properly tendered will remain outstanding and continue to accrue interest;
- (4) that unless the Issuer defaults in the payment of the Change of Control Payment, all Notes accepted for payment pursuant to the Change of Control Offer will cease to accrue interest on the Change of Control Payment Date;
- (5) that Holders electing to have any Notes purchased pursuant to a Change of Control Offer will be required to surrender such Notes, with the form entitled "Option of Holder to Elect Purchase" on the reverse of such Notes completed, to the paying agent specified in the notice at the address specified in the notice prior to the close of business on the third Business Day preceding the Change of Control Payment Date;
- (6) that Holders will be entitled to withdraw their tendered Notes and their election to require the Issuer to purchase such Notes, <u>provided</u> that the paying agent receives, not later than the close of business on the expiration date of the Change of Control Offer, a telegram, facsimile transmission or letter setting forth the name of the Holder of the Notes, the principal amount of Notes tendered for purchase, and a statement that such Holder is withdrawing its tendered Notes and its election to have such Notes purchased;
- (7) that if the Issuer is redeeming less than all of the Notes, the Holders of the remaining Notes will be issued new Notes and such new Notes will be equal in principal amount to the unpurchased portion of the Notes surrendered. The unpurchased portion of the Notes must be equal to at least \$2,000 or an integral multiple of \$1,000 thereafter;

- (8) if such notice is sent prior to the occurrence of a Change of Control, stating that the Change of Control Offer is conditional on the occurrence of such Change of Control; and
 - (9) the other instructions, as determined by the Issuer, consistent with this Section 4.14 described hereunder, that a Holder must follow.

The notice, if transmitted in a manner herein provided, shall be conclusively presumed to have been given, whether or not the Holder receives such notice. If (a) the notice is transmitted in a manner herein provided and (b) any Holder fails to receive such notice or a Holder receives such notice but it is defective, such Holder's failure to receive such notice or such defect shall not affect the validity of the proceedings for the purchase of the Notes as to all other Holders that properly received such notice without defect. The Issuer shall comply with the requirements of Rule 14e-1 under the Exchange Act and any other securities laws and regulations thereunder to the extent such laws or regulations are applicable in connection with the repurchase of Notes pursuant to a Change of Control Offer. To the extent that the provisions of any securities laws or regulations conflict with the provisions of this Indenture, the Issuer shall comply with the applicable securities laws and regulations and shall not be deemed to have breached its obligations under this Indenture by virtue thereof.

- (b) On the Change of Control Payment Date, the Issuer shall, to the extent permitted by law,
- (1) accept for payment all Notes issued by it or portions thereof properly tendered pursuant to the Change of Control Offer,
- (2) deposit with the Paying Agent an amount equal to the aggregate Change of Control Payment in respect of all Notes or portions thereof so tendered, and
- (3) deliver, or cause to be delivered, to the Trustee for cancellation the Notes so accepted together with an Officer's Certificate to the Trustee stating that such Notes or portions thereof have been tendered to and purchased by the Issuer.
- (c) The Issuer shall not be required to make a Change of Control Offer following a Change of Control if a third party makes the Change of Control Offer in the manner, at the times and otherwise in compliance with the requirements set forth in this Indenture applicable to a Change of Control Offer made by the Issuer and purchases all Notes validly tendered and not withdrawn under such Change of Control Offer. Notwithstanding anything to the contrary herein, a Change of Control Offer may be made in advance of a Change of Control, conditional upon such Change of Control, if a definitive agreement is in place for the Change of Control at the time of making of the Change of Control Offer.

- (d) Other than as specifically provided in this Section 4.14, any purchase pursuant to this Section 4.14 shall be made pursuant to the provisions of Sections 3.02, 3.05 and 3.06 hereof, and references therein to "redeem," "redemption" and similar words shall be deemed to refer to "purchase," "repurchase" and similar words, as applicable.
- SECTION 4.15. <u>Limitation on Guarantees of Indebtedness by Restricted Subsidiaries</u>. Holdings III shall not permit any of its Restricted Subsidiaries, other than a Guarantor or the Issuer, to guarantee the payment of any First Lien Obligations, including any Indebtedness (or any interest on such Indebtedness) under the Senior Credit Facilities and the Existing Secured Notes unless:
 - (1) such Restricted Subsidiary within 30 days executes and delivers a supplemental indenture to this Indenture, the form of which is attached as Exhibit D hereto, providing for a Guarantee by such Restricted Subsidiary, except that with respect to a guarantee of Indebtedness of the Issuer or any Guarantor, if such Indebtedness is by its express terms subordinated in right of payment to the Notes or such Guarantor's Guarantee, any such guarantee by such Restricted Subsidiary with respect to such Indebtedness shall be subordinated in right of payment to such Guarantee substantially to the same extent as such Indebtedness is subordinated to the Notes;
 - (2) such Restricted Subsidiary waives and shall not in any manner whatsoever claim or take the benefit or advantage of, any rights of reimbursement, indemnity or subrogation or any other rights against any Guarantor or any other Restricted Subsidiary as a result of any payment by such Person under its Guarantee or otherwise; and
 - (3) such Restricted Subsidiary shall deliver to the Trustee an Opinion of Counsel to the effect that:
 - (A) such Guarantee has been duly executed and authorized; and
 - (B) such Guarantee constitutes a valid, binding and enforceable obligation of such Restricted Subsidiary, except insofar as enforcement thereof may be limited by bankruptcy, insolvency or similar laws (including, without limitation, all laws relating to fraudulent transfers) and except insofar as enforcement thereof is subject to general principles of equity.

SECTION 4.16. Suspension of Covenants.

- (a) During any period of time that (i) the Notes have Investment Grade Ratings from both Rating Agencies and (ii) no Default has occurred and is continuing under this Indenture (the occurrence of the events described in the foregoing clauses (i) and (ii) being collectively referred to as a "Covenant Suspension Event" and the date thereof being referred to as the "Suspension Date") then, Section 4.07 hereof, Section 4.08 hereof, Section 4.09 hereof, Section 4.11 hereof, clause (4) of Section 5.01(a) hereof and clause (4) of Section 5.01(c) hereof shall not be applicable to the Notes (collectively, the "Suspended Covenants").
- (b) During any period that the foregoing covenants have been suspended, Holdings III may not designate any of its Subsidiaries as Unrestricted Subsidiaries pursuant to the second sentence of the definition of "Unrestricted Subsidiary."
- (c) In the event that Holdings III and its Restricted Subsidiaries are not subject to the Suspended Covenants under this Indenture for any period of time as a result of the foregoing, and on any subsequent date (the "Reversion Date") one or both of the Rating Agencies withdraw their Investment Grade Rating or downgrade the rating assigned to the Notes below an Investment Grade Rating, then Holdings III and its Restricted Subsidiaries will thereafter again be subject to the Suspended Covenants under this Indenture with respect to future events. The period of time between the Suspension Date and the Reversion Date is referred to in this Section 4.16 as the "Suspension Period." Additionally, upon the occurrence of a Covenant Suspension Event, the amount of Excess Proceeds from Net Proceeds shall be reset to zero.
- (d) During any Suspension Period, Holdings III will not, and will not permit any Restricted Subsidiary to, enter into any Sale and Lease-Back Transaction; <u>provided</u>, that Holdings III or any Restricted Subsidiary may enter into a Sale and Lease-Back Transaction if (i) Holdings III or such Restricted Subsidiary could have incurred a Lien to secure the Indebtedness attributable to such Sale and Lease-Back Transaction pursuant to Section 4.12 hereof without equally and ratably securing the Notes pursuant to the covenant described under such section; and (ii) the consideration received by Holdings III or such Restricted Subsidiary in that Sale and Lease-Back Transaction is at least equal to the fair market value of the property sold and otherwise complies with Section 4.10 hereof; <u>provided</u>, <u>further</u>, that the foregoing provisions shall cease to apply on and subsequent to the Reversion Date following such Suspension Period.
- (e) Notwithstanding the foregoing, in the event of any such reinstatement, no action taken or omitted to be taken by Holdings III or any of its Restricted Subsidiaries prior to such reinstatement will give rise to a Default or Event of Default under this Indenture; <u>provided</u> that (1) with respect to Restricted Payments made after such reinstatement, the amount of Restricted Payments made will be calculated as though Section 4.07 had been in effect prior to, but not during, the Suspension Period; and (2) all Indebtedness incurred, or Disqualified Stock issued, during the Suspension Period will be

classified to have been incurred or issued pursuant to Section 4.09(b)(3). In addition, for purposes of clause (3) of Section 4.07(a) hereof, all events set forth in such clause (3) occurring during a Suspension Period shall be disregarded for purposes of determining the amount of Restricted Payments Holdings III or any Restricted Subsidiary is permitted to make pursuant to such clause (3).

(f) The Issuer shall deliver promptly to the Trustee an Officer's Certificate of the Issuer notifying it of any event set forth under this Section 4.16.

ARTICLE V

SUCCESSORS

SECTION 5.01. Merger, Consolidation or Sale of All or Substantially All Assets.

- (a) The Issuer may not consolidate or merge with or into or wind up into (whether or not the Issuer is the surviving corporation), or sell, assign, transfer, lease, convey or otherwise dispose of all or substantially all of its properties or assets, in one or more related transactions, to any Person unless:
 - (1) the Issuer is the surviving corporation or the Person formed by or surviving any such consolidation or merger (if other than the Issuer) or to which such sale, assignment, transfer, lease, conveyance or other disposition will have been made, is a Person organized or existing under the laws of the jurisdiction of organization of the Issuer or the laws of the United States, any state thereof, the District of Columbia, or any territory thereof (such Person, as the case may be, being herein called the "Successor Company"); provided that in the case where the surviving Person is not a corporation, a co-obligor of the Notes is a corporation;
 - (2) the Successor Company, if other than the Issuer, expressly assumes all the obligations of the Issuer under this Indenture and the Notes pursuant to supplemental indentures or other documents or instruments and the performance of the covenants and obligations of the Issuer under the Collateral Documents relating to the Notes and shall cause such amendments, supplements, or other instruments to be executed, filed and recorded in such jurisdictions as may be required by applicable law to preserve and protect the Lien on the Collateral owned by or transferred to the Successor Company, together with such financing statements or comparable documents as may be required to perfect any security interests in such Collateral which may be perfected by the filing of a financing statement or a similar document under the UCC or other similar statute or regulation of the relevant states or jurisdictions;
 - (3) immediately after such transaction, no Default exists;

- (4) immediately after giving <u>pro forma</u> effect to such transaction and any related financing transactions, as if such transactions had occurred at the beginning of the applicable four-quarter period,
 - (A) the Successor Company or the Issuer would be permitted to incur at least \$1.00 of additional Indebtedness pursuant to the Fixed Charge Coverage Test set forth in Section 4.09(a) hereof, or
 - (B) the Fixed Charge Coverage Ratio for Holdings III and the Restricted Subsidiaries would be equal to or greater than the Fixed Charge Coverage Ratio for Holdings III and its Restricted Subsidiaries immediately prior to such transaction;
- (5) each Guarantor, unless it is the other party to the transactions described above, in which case Section 5.01(e)(1)(B) hereof shall apply, shall have by supplemental indenture confirmed that its Guarantee shall apply to such Person's obligations under this Indenture and the Notes; and
- (6) the Issuer shall have delivered to the Trustee an Officer's Certificate and an Opinion of Counsel, each stating that such consolidation, merger or transfer and such supplemental indentures, if any, comply with this Indenture.
- (b) The Successor Company will succeed to, and be substituted for the Issuer under this Indenture, the Guarantees and the Notes, as applicable. Notwithstanding clauses (3) and (4) of Section 5.01(a) hereof,
 - (1) any Restricted Subsidiary may consolidate with or merge into or transfer all or part of its properties and assets to the Issuer, and
 - (2) the Issuer may merge with an Affiliate of the Issuer solely for the purpose of reincorporating the Issuer in a State of the United States so long as the amount of Indebtedness of Holdings III and its Restricted Subsidiaries is not increased thereby.
- (c) Holdings III may not consolidate, amalgamate or merge with or into or wind up into (whether or not Holdings III is the surviving corporation), or sell, assign, transfer, lease, convey or otherwise dispose of all or substantially all of its properties or assets, in one or more related transactions, to any Person unless:
 - (1) Holdings III is the surviving corporation or the Person formed by or surviving any such consolidation, amalgamation or merger (if other than Holdings III) or to which such sale, assignment, transfer, lease, conveyance or other disposition will have been made, is a Person organized or existing under the laws of the jurisdiction of organization of Holdings III or the laws of the United States, any state thereof, the District of Columbia, or any territory thereof (such Person, as the case may be, being herein called the "Successor Guarantor");

- (2) the Successor Guarantor, if other than Holdings III, expressly assumes all the obligations of Holdings III under this Indenture and the Notes pursuant to supplemental indentures or other documents or instruments and the performance of the covenants and obligations of Holdings III under the Collateral Documents relating to the Notes and shall cause such amendments, supplements, or other instruments to be executed, filed and recorded in such jurisdictions as may be required by applicable law to preserve and protect the Lien on the Collateral owned by or transferred to the Successor Guarantor, together with such financing statements or comparable documents as may be required to perfect any security interests in such Collateral which may be perfected by the filing of a financing statement or a similar document under the UCC or other similar statute or regulation of the relevant states or jurisdictions;
 - (3) immediately after such transaction, no Default exists;
- (4) immediately after giving <u>pro forma</u> effect to such transaction and any related financing transactions, as if such transactions had occurred at the beginning of the applicable four-quarter period,
 - (A) the Successor Guarantor or Holdings III would be permitted to incur at least \$1.00 of additional Indebtedness pursuant to the Fixed Charge Coverage Test set forth in Section 4.09(a) hereof, or
 - (B) the Fixed Charge Coverage Ratio for the Successor Guarantor or Holdings III, as applicable, and the Restricted Subsidiaries would be equal to or greater than the Fixed Charge Coverage Ratio for Holdings III and its Restricted Subsidiaries immediately prior to such transaction; and
- (5) Holdings III shall have delivered to the Trustee an Officer's Certificate and an Opinion of Counsel, each stating that such consolidation, amalgamation, merger or transfer and such supplemental indentures, if any, comply with this Indenture.
- (d) The Successor Guarantor, if other than Holdings III, will succeed to, and be substituted for Holdings III under this Indenture, the Guarantees and the Notes, as applicable. Notwithstanding the clauses (3) and (4) of Section 5.01(c) hereof,
 - (1) any Restricted Subsidiary may consolidate or amalgamate with or merge into or transfer all or part of its properties and assets to Holdings III, and
 - (2) Holdings III may amalgamate or merge with its Affiliate solely for the purpose of reincorporating Holdings III in another jurisdiction (regardless of clause (1) of paragraph (c) above) so long as the amount of Indebtedness of Holdings III and its Restricted Subsidiaries is not increased thereby and so long as the surviving entity (if not Holdings III) assumes all of Holdings III's obligations under this Indenture, the Notes and its Guarantee in connection with such reincorporation.

- (e) Subject to Section 10.06 hereof, no Guarantor (other than Parent, Holdings II and Holdings III, subject to Section 5.01(c) above) will, and Holdings III will not permit any such Guarantor (other than Parent and Holdings II) to, consolidate, amalgamate or merge with or into or wind up into (whether or not Holdings III, the Issuer or such Guarantor is the surviving corporation), or sell, assign, transfer, lease, convey or otherwise dispose of all or substantially all of its properties or assets, in one or more related transactions, to any Person unless:
 - (1) (A) such Guarantor is the surviving corporation or the Person formed by or surviving any such consolidation, amalgamation or merger (if other than such Guarantor) or to which such sale, assignment, transfer, lease, conveyance or other disposition will have been made is a Person organized or existing under the laws of the jurisdiction of organization of such Guarantor, as the case may be, or the laws of the United States, any state thereof, the District of Columbia, or any territory thereof (such Person being herein called the "Successor Person");
 - (B) the Successor Person, if other than such Guarantor, expressly assumes all the obligations of such Guarantor under this Indenture and such Guarantor's related Guarantee pursuant to supplemental indentures or other documents or instruments and the performance of the covenants and obligations of such Guarantor under the Collateral Documents relating to the Notes and shall cause such amendments, supplements, or other instruments to be executed, filed and recorded in such jurisdictions as may be required by applicable law to preserve and protect the Lien on the Collateral owned by or transferred to the Successor Person, together with such financing statements or comparable documents as may be required to perfect any security interests in such Collateral which may be perfected by the filing of a financing statement or a similar document under the UCC or other similar statute or regulation of the relevant states or jurisdictions;
 - (C) immediately after such transaction, no Default exists; and
 - (D) the Issuer shall have delivered to the Trustee an Officer's Certificate and an Opinion of Counsel, each stating that such consolidation, amalgamation, merger or transfer and such supplemental indentures, if any, comply with this Indenture; or
 - (2) the transaction is made in compliance with Section 4.10 hereof.
- (f) Subject to Section 10.06 hereof, the Successor Person will succeed to, and be substituted for, such Guarantor under this Indenture and such Guarantor's Guarantee. Notwithstanding the foregoing, any Guarantor (other than Holdings III, subject to Section 5.01(d) above) may merge or amalgamate into or transfer all or part of

its properties and assets to Holdings III, the Issuer or any Guarantor and any such Guarantor may merge or amalgamate with a Subsidiary of Holdings III solely for the purpose of reincorporating such Guarantor in another jurisdiction (regardless of clause (1) of paragraph (e) above) so long as the amount of Indebtedness of Holdings III and its Restricted Subsidiaries is not increased thereby and so long as the surviving entity (if not the Guarantor) assumes all of the Guarantor's obligations under its Guarantee in connection with such reincorporation.

(g) Holdings III shall, directly or indirectly, at all times own 100% of the Equity Interests of the Issuer (other than Equity Interests held by employees of the Issuer or any Restricted Subsidiary as of the Issue Date and Equity Interests issued in exchange therefor).

SECTION 5.02. Successor Corporation Substituted. Upon any consolidation, amalgamation or merger, or any sale, assignment, transfer, lease, conveyance or other disposition of all or substantially all of the assets of the Issuer or a Guarantor in accordance with Section 5.01 hereof, the successor corporation formed by such consolidation or into or with which the Issuer or such Guarantor, as applicable, is merged, amalgamated or to which such sale, assignment, transfer, lease, conveyance or other disposition is made shall succeed to, and be substituted for (so that from and after the date of such consolidation, amalgamation, merger, sale, lease, conveyance or other disposition, the provisions of this Indenture referring to the Issuer or such Guarantor, as applicable, shall refer instead to the successor corporation and not to the Issuer or such Guarantor, as applicable), and may exercise every right and power of the Issuer or such Guarantor, as applicable, under this Indenture with the same effect as if such successor Person had been named as the Issuer or a Guarantor, as applicable, herein; provided that the predecessor Issuer shall not be relieved from the obligation to pay the principal of and interest on the Notes except in the case of a sale, assignment, transfer, conveyance or other disposition of all of the Issuer's assets that meets the requirements of Section 5.01 hereof.

ARTICLE VI

DEFAULTS AND REMEDIES

SECTION 6.01. Events of Default.

An "Event of Default" wherever used herein, means any one of the following events (whatever the reason for such Event of Default and whether it shall be voluntary or involuntary or be effected by operation of law or pursuant to any judgment, decree or order of any court or any order, rule or regulation of any administrative or governmental body):

(1) default in payment when due and payable, upon redemption, acceleration or otherwise, of principal of, or premium, if any, on the Notes;

- (2) default for 30 days or more in the payment when due of interest on or with respect to the Notes;
- (3) failure by Holdings III, the Issuer or any other Guarantor for 60 days after receipt of written notice given by the Trustee or the Holders of not less than 30% in principal amount of the Notes to comply with any of its obligations, covenants or agreements (other than a default referred to in clauses (1) and (2) above) contained in this Indenture or the Notes;
- (4) default under any mortgage, indenture or instrument under which there is issued or by which there is secured or evidenced any Indebtedness for money borrowed by Holdings III or any of its Restricted Subsidiaries or the payment of which is guaranteed by Holdings III or any of its Restricted Subsidiaries, other than Indebtedness owed to Holdings III or a Restricted Subsidiary, whether such Indebtedness or guarantee now exists or is created after the issuance of the Notes, if both:
 - (A) such default either results from the failure to pay any principal of such Indebtedness at its stated final maturity (after giving effect to any applicable grace periods) or relates to an obligation other than the obligation to pay principal of any such Indebtedness at its stated final maturity and results in the holder or holders of such Indebtedness causing such Indebtedness to become due prior to its stated maturity; and
 - (B) the principal amount of such Indebtedness, together with the principal amount of any other such Indebtedness in default for failure to pay principal at stated final maturity (after giving effect to any applicable grace periods), or the maturity of which has been so accelerated, aggregate \$50.0 million or more at any one time outstanding;
- (5) failure by Holdings III or any Significant Subsidiary (or any group of Subsidiaries that together would constitute a Significant Subsidiary) to pay final judgments aggregating in excess of \$50.0 million, which final judgments remain unpaid, undischarged and unstayed for a period of more than 60 days after such judgment becomes final, and in the event such judgment is covered by insurance, an enforcement proceeding has been commenced by any creditor upon such judgment or decree which is not promptly stayed;

- (6) Holdings III, the Issuer or any of its Restricted Subsidiaries that is a Significant Subsidiary (or any group of Restricted Subsidiaries that, taken together, would constitute a Significant Subsidiary), pursuant to or within the meaning of any Bankruptcy Law:
 - (i) commences proceedings to be adjudicated bankrupt or insolvent;
 - (ii) consents to the institution of bankruptcy or insolvency proceedings against it, or the filing by it of a petition or answer or consent seeking reorganization or relief under applicable Bankruptcy law;
 - (iii) consents to the appointment of a receiver, liquidator, assignee, trustee, sequestrator or other similar official of it or for all or substantially all of its property;
 - (iv) makes a general assignment for the benefit of its creditors; or
 - (v) generally is not paying its debts as they become due;
 - (7) a court of competent jurisdiction enters an order or decree under any Bankruptcy Law that:
 - (i) is for relief against Holdings III, the Issuer or any of its Restricted Subsidiaries that is a Significant Subsidiary (or any group of Restricted Subsidiaries that, taken together, would constitute a Significant Subsidiary), in a proceeding in which Holdings III, the Issuer or any such Restricted Subsidiaries, that is a Significant Subsidiary (or any group of Restricted Subsidiaries that, taken together, would constitute a Significant Subsidiary), is to be adjudicated bankrupt or insolvent;
 - (ii) appoints a receiver, liquidator, assignee, trustee, sequestrator or other similar official of Holdings III, the Issuer or any of its Restricted Subsidiaries that is a Significant Subsidiary (or any group of Restricted Subsidiaries that, taken together, would constitute a Significant Subsidiary), or for all or substantially all of the property of Holdings III, the Issuer or any of its Restricted Subsidiaries that is a Significant Subsidiary (or any group of Restricted Subsidiaries that, taken together, would constitute a Significant Subsidiary); or
 - (iii) orders the liquidation of Holdings III, the Issuer or any of its Restricted Subsidiaries that is a Significant Subsidiary (or any group of Restricted Subsidiaries that, taken together, would constitute a Significant Subsidiary);

and the order or decree remains unstayed and in effect for 60 consecutive days;

- (8) the Guarantee of any Restricted Parent Guarantor or Significant Subsidiary (or any group of Subsidiaries that together would constitute a Significant Subsidiary) shall for any reason cease to be in full force and effect or be declared null and void or any responsible officer of any Restricted Parent Guarantor or any Guarantor that is a Significant Subsidiary (or the responsible officers of any group of Subsidiaries that together would constitute a Significant Subsidiary), as the case may be, denies that it has any further liability under its Guarantee or gives notice to such effect, other than by reason of the termination of this Indenture or the release of any such Guarantee in accordance with this Indenture; or
- (9) the Liens created by the Collateral Documents relating to the Notes shall not constitute a valid and perfected Lien on any portion of the Collateral with a fair market value or book value equal to or more than \$25.0 million intended to be covered thereby (to the extent perfection is required by the First Lien Debt Documents) except as otherwise permitted by the terms of this Indenture or the relevant First Lien Debt Documents and other than the satisfaction in full of all obligations of the Issuer and the Guarantors under this Indenture or the release or amendment of any such Lien in accordance with the terms of the First Lien Debt Documents, or, except for expiration in accordance with its terms or amendment, modification, waiver, termination or release in accordance with the terms of the First Lien Debt Documents, any of the Collateral Documents relating to the Notes shall for whatever reason be terminated or cease to be in full force and effect, if, in either case, such default continues for 60 days after notice, or the enforceability thereof shall be contested by the Issuer or any Guarantor, except to the extent that any such loss of perfection or priority results from the failure of the Collateral Agent to make filings, renewals and continuations (or other equivalent filings) or take other appropriate action or the failure of the Collateral Agent to maintain possession of certificates, instruments or other documents actually delivered to it representing securities pledged or other possessory collateral pledged under the applicable Collateral Documents relating to the Notes.

SECTION 6.02. <u>Acceleration</u>. If any Event of Default (other than an Event of Default specified in clause (6) or (7) of Section 6.01 hereof) occurs and is continuing under this Indenture, the Trustee, upon receipt of actual written notice of a default, or the Holders of at least 30% in principal amount of the then total outstanding Notes may declare the principal, premium, if any, interest and any other monetary obligations on all the then outstanding Notes to be due and payable immediately. Upon the effectiveness of such declaration, such principal and interest shall be due and payable immediately. The Trustee shall have no obligation to accelerate the Notes if it believes in good faith that acceleration is not in the best interests of the Holders of the Notes.

Notwithstanding the foregoing, in the case of an Event of Default arising under clause (6) or (7) of Section 6.01 hereof, all outstanding Notes shall be due and payable immediately without further action or notice.

The Holders of a majority in aggregate principal amount of the then outstanding Notes by written notice to the Trustee may on behalf of all of the Holders of all of the Notes rescind any acceleration with respect to the Notes and its consequences if such rescission would not conflict with any judgment or decree of a court of competent jurisdiction and if all existing Events of Default (except nonpayment of principal, interest or premium that has become due solely because of the acceleration) have been cured or waived.

In the event of any Event of Default specified in clause (4) of Section 6.01 hereof, such Event of Default and all consequences thereof (excluding any resulting payment default, other than as a result of acceleration of the Notes) shall be annulled, waived and rescinded, automatically and without any action by the Trustee or the Holders, if within 20 days after such Event of Default arose:

- (1) the Indebtedness or guarantee that is the basis for such Event of Default has been discharged; or
- (2) holders thereof have rescinded or waived the acceleration, notice or action (as the case may be) giving rise to such Event of Default; or
- (3) the default that is the basis for such Event of Default has been cured.

SECTION 6.03. Other Remedies. If an Event of Default occurs and is continuing, the Trustee may pursue any available remedy to collect the payment of principal, premium, if any, and interest on the Notes or to enforce the performance of any provision of the Notes or this Indenture.

The Trustee may maintain a proceeding even if it does not possess any of the Notes or does not produce any of them in the proceeding. A delay or omission by the Trustee or any Holder of a Note in exercising any right or remedy accruing upon an Event of Default shall not impair the right or remedy or constitute a waiver of or acquiescence in the Event of Default. All remedies are cumulative to the extent permitted by law.

SECTION 6.04. Waiver of Past Defaults. Subject to Section 6.02 hereof, Holders of not less than a majority in aggregate principal amount of the then outstanding Notes by notice to the Trustee may on behalf of the Holders of all of the Notes waive any existing Default and its consequences hereunder (except a continuing Default in the payment of the principal of, premium, if any, or interest on, any Note held by a non-consenting Holder) (including in connection with an Asset Sale Offer or a Change of Control Offer). Upon any such waiver, such Default shall cease to exist, and any Event of Default arising therefrom shall be deemed to have been cured for every purpose of this Indenture; but no such waiver shall extend to any subsequent or other Default or impair any right consequent thereon.

SECTION 6.05. Control by Majority. Holders of a majority in principal amount of the then total outstanding Notes may direct the time, method and place of conducting any proceeding for any remedy available to the Trustee or of exercising any trust or power conferred on the Trustee without any liability to the Trustee. The Trustee, however, may refuse to follow any direction that conflicts with law or this Indenture or that the Trustee determines is unduly prejudicial to the rights of any other Holder of a Note or that would involve the Trustee in personal liability.

SECTION 6.06. <u>Limitation on Suits.</u> Subject to Section 6.07 hereof, no Holder of a Note may pursue any remedy with respect to this Indenture or the Notes unless:

- (1) such Holder has previously given the Trustee notice that an Event of Default is continuing;
- (2) Holders of at least 30% in principal amount of the total outstanding Notes have requested the Trustee to pursue the remedy;
- (3) Holders of the Notes have offered the Trustee security or indemnity satisfactory to it against any loss, liability or expense;
- (4) the Trustee has not complied with such request within 60 days after the receipt thereof and the offer of security or indemnity; and
- (5) Holders of a majority in principal amount of the total outstanding Notes have not given the Trustee a direction inconsistent with such request within such 60-day period.

A Holder of a Note may not use this Indenture to prejudice the rights of another Holder of a Note or to obtain a preference or priority over another Holder of a Note.

SECTION 6.07. <u>Rights of Holders of Notes to Receive Payment.</u> Notwithstanding any other provision of this Indenture, the right of any Holder of a Note to receive payment of principal of, premium, if any, and interest on the Note, on or after the respective due dates expressed in the Note (including in connection with an Asset Sale Offer or a Change of Control Offer), or to bring suit for the enforcement of any such payment on or after such respective dates, shall not be impaired or affected without the consent of such Holder.

SECTION 6.08. <u>Collection Suit by Trustee</u>. If an Event of Default specified in Section 6.01(1) or (2) hereof occurs and is continuing, the Trustee is authorized to recover judgment in its own name and as trustee of an express trust against the Issuer for the whole amount of principal of, premium, if any, and interest remaining unpaid on the Notes and interest on overdue principal and, to the extent lawful, interest and such further amount as shall be sufficient to cover the costs and expenses of collection, including the reasonable compensation, expenses, disbursements and advances of the Trustee, its agents and counsel.

SECTION 6.09. Restoration of Rights and Remedies. If the Trustee or any Holder has instituted any proceeding to enforce any right or remedy under this Indenture and such proceeding has been discontinued or abandoned for any reason, or has been determined adversely to the Trustee or to such Holder, then and in every such case, subject to any determination in such proceedings, the Issuer, the Trustee and the Holders shall be restored severally and respectively to their former positions hereunder and thereafter all rights and remedies of the Trustee and the Holders shall continue as though no such proceeding has been instituted.

SECTION 6.10. <u>Rights and Remedies Cumulative</u>. Except as otherwise provided with respect to the replacement or payment of mutilated, destroyed, lost or stolen Notes in Section 2.07 hereof, no right or remedy herein conferred upon or reserved to the Trustee or to the Holders is intended to be exclusive of any other right or remedy, and every right and remedy shall, to the extent permitted by law, be cumulative and in addition to every other right and remedy given hereunder or now or hereafter existing at law or in equity or otherwise. The assertion or employment of any right or remedy hereunder, or otherwise, shall not prevent the concurrent assertion or employment of any other appropriate right or remedy.

SECTION 6.11. <u>Delay or Omission Not Waiver.</u> No delay or omission of the Trustee or of any Holder of any Note to exercise any right or remedy accruing upon any Event of Default shall impair any such right or remedy or constitute a waiver of any such Event of Default or an acquiescence therein. Every right and remedy given by this Article or by law to the Trustee or to the Holders may be exercised from time to time, and as often as may be deemed expedient, by the Trustee or by the Holders, as the case may be.

SECTION 6.12. <u>Trustee May File Proofs of Claim.</u> The Trustee is authorized to file such proofs of claim and other papers or documents as may be necessary or advisable in order to have the claims of the Trustee (including any claim for the reasonable compensation, expenses, disbursements and advances of the Trustee, its agents and counsel) and the Holders of the Notes allowed in any judicial proceedings relative to the Issuer (or any other obligor upon the Notes including the Guarantors), its creditors or its property and shall be entitled and empowered to participate as a member in any official committee of creditors appointed in such matter and to collect, receive and distribute any money or other property payable or deliverable on any such claims and any custodian in any such judicial proceeding is hereby authorized by each Holder to make such payments to the Trustee, and in the event that the Trustee shall consent to the making of such payments directly to the Holders, to pay to the Trustee any amount due to

it for the reasonable compensation, expenses, disbursements and advances of the Trustee, its agents and counsel, and any other amounts due the Trustee under Section 7.06 hereof. To the extent that the payment of any such compensation, expenses, disbursements and advances of the Trustee, its agents and counsel, and any other amounts due the Trustee under Section 7.06 hereof out of the estate in any such proceeding, shall be denied for any reason, payment of the same shall be secured by a Lien on, and shall be paid out of, any and all distributions, dividends, money, securities and other properties that the Holders may be entitled to receive in such proceeding whether in liquidation or under any plan of reorganization or arrangement or otherwise. Nothing herein contained shall be deemed to authorize the Trustee to authorize or consent to or accept or adopt on behalf of any Holder any plan of reorganization, arrangement, adjustment or composition affecting the Notes or the rights of any Holder, or to authorize the Trustee to vote in respect of the claim of any Holder in any such proceeding.

SECTION 6.13. <u>Priorities.</u> If the Trustee or any Agent collects any money pursuant to this Article 6, it shall pay out the money in the following order:

- (i) to the Trustee, such Agent, their agents and attorneys for amounts due under Section 7.06 hereof, including payment of all compensation, expenses and liabilities incurred, and all advances made, by the Trustee or such Agent and the costs and expenses of collection;
- (ii) to Holders of Notes for amounts due and unpaid on the Notes for principal, premium, if any, and interest, ratably, without preference or priority of any kind, according to the amounts due and payable on the Notes for principal, premium, if any, and interest, respectively; and
 - (iii) to the Issuer or to such party as a court of competent jurisdiction shall direct including a Guarantor, if applicable.

The Trustee may fix a record date and payment date for any payment to Holders of Notes pursuant to this Section 6.13.

SECTION 6.14. <u>Undertaking for Costs.</u> In any suit for the enforcement of any right or remedy under this Indenture or in any suit against the Trustee for any action taken or omitted by it as a Trustee, a court in its discretion may require the filing by any party litigant in the suit of an undertaking to pay the costs of the suit, and the court in its discretion may assess reasonable costs, including reasonable attorneys' fees, against any party litigant in the suit, having due regard to the merits and good faith of the claims or defenses made by the party litigant. This Section 6.14 does not apply to a suit by the Trustee, a suit by a Holder of a Note pursuant to Section 6.07 hereof, or a suit by Holders of more than 10% in principal amount of the then outstanding Notes.

ARTICLE VII

TRUSTEE

SECTION 7.01. Duties of Trustee.

- (a) If an Event of Default has occurred and is continuing, the Trustee shall exercise such of the rights and powers vested in it by this Indenture, and use the same degree of care and skill in its exercise, as a prudent person would exercise or use under the circumstances in the conduct of such person's own affairs.
 - (b) Except during the continuance of an Event of Default:
 - (i) the duties of the Trustee shall be determined solely by the express provisions of this Indenture and the Trustee need perform only those duties that are specifically set forth in this Indenture and no others, and no implied covenants or obligations shall be read into this Indenture against the Trustee; and
 - (ii) in the absence of bad faith on its part, the Trustee may conclusively rely, as to the truth of the statements and the correctness of the opinions expressed therein, upon certificates or opinions furnished to the Trustee and conforming to the requirements of this Indenture. However, in the case of any such certificates or opinions which by any provision hereof are specifically required to be furnished to the Trustee, the Trustee shall examine the certificates and opinions to determine whether or not they conform to the requirements of this Indenture.
- (c) The Trustee may not be relieved from liabilities for its own negligent action, its own negligent failure to act, or its own willful misconduct, except that:
 - (i) this paragraph does not limit the effect of paragraph (b) of this Section 7.01;
 - (ii) the Trustee shall not be liable for any error of judgment made in good faith, unless it is proved in a court of competent jurisdiction that the Trustee was negligent in ascertaining the pertinent facts; and
 - (iii) the Trustee shall not be liable with respect to any action it takes or omits to take in good faith in accordance with a direction received by it pursuant to Section 6.02, 6.04 or 6.05 hereof.
- (d) Whether or not therein expressly so provided, every provision of this Indenture that in any way relates to the Trustee is subject to paragraphs (a), (b) and (c) of this Section 7.01.

- (e) The Trustee shall be under no obligation to exercise any of its rights or powers under this Indenture at the request or direction of any of the Holders of the Notes unless the Holders have offered to the Trustee indemnity or security reasonably satisfactory to it against any loss, liability or expense.
- (f) The Trustee shall not be liable for interest on any money received by it except as the Trustee may agree in writing with the Issuer. Money held in trust by the Trustee need not be segregated from other funds except to the extent required by law.

SECTION 7.02. Rights of Trustee.

- (a) The Trustee may conclusively rely upon any document believed by it to be genuine and to have been signed or presented by the proper Person. The Trustee need not investigate any fact or matter stated in the document, but the Trustee, in its discretion, may make such further inquiry or investigation into such facts or matters as it may see fit, and, if the Trustee shall determine to make such further inquiry or investigation, it shall be entitled to examine the books, records and premises of Holdings III and its Restricted Subsidiaries, personally or by agent or attorney at the sole cost of the Issuer and shall incur no liability or additional liability of any kind by reason of such inquiry or investigation.
- (b) Before the Trustee acts or refrains from acting, it may require an Officer's Certificate of the Issuer or Holdings III or an Opinion of Counsel or both. The Trustee shall not be liable for any action it takes or omits to take in good faith in reliance on such Officer's Certificate or Opinion of Counsel. The Trustee may consult with counsel of its selection and the written advice of such counsel or any Opinion of Counsel shall be full and complete authorization and protection from liability in respect of any action taken, suffered or omitted by it hereunder in good faith and in reliance thereon.
- (c) The Trustee may act through its attorneys and agents and shall not be responsible for the misconduct or negligence of any agent or attorney appointed with due care.
- (d) The Trustee shall not be liable for any action it takes or omits to take in good faith that it believes to be authorized or within the rights or powers conferred upon it by this Indenture.
- (e) Unless otherwise specifically provided in this Indenture, any demand, request, direction or notice from the Issuer shall be sufficient if signed by an Officer of the Issuer.
- (f) None of the provisions of this Indenture shall require the Trustee to expend or risk its own funds or otherwise to incur any liability, financial or otherwise, in the performance of any of its duties hereunder, or in the exercise of any of its rights or powers if it shall have reasonable grounds for believing that repayment of such funds or indemnity satisfactory to it against such risk or liability is not assured to it.

- (g) The Trustee shall not be deemed to have notice of any Default or Event of Default unless written notice of any event which is in fact such a Default is received by a Responsible Officer of the Trustee at the Corporate Trust Office of the Trustee, and such notice references the Notes and this Indenture.
- (h) In no event shall the Trustee be responsible or liable for any punitive, special, indirect, or consequential loss or damage of any kind whatsoever (including, but not limited to, loss of profit) irrespective of whether the Trustee has been advised of the likelihood of such loss or damage and regardless of the form of action.
- (i) The rights, privileges, protections, immunities and benefits given to the Trustee, including, without limitation, its right to be indemnified, are extended to, and shall be enforceable by, the Trustee in each of its capacities hereunder, and each agent, custodian and other Person employed to act hereunder.

SECTION 7.03. <u>Individual Rights of Trustee</u>. The Trustee in its individual or any other capacity may become the owner or pledgee of Notes and may otherwise deal with the Issuer or any Affiliate of the Issuer with the same rights it would have if it were not Trustee. However, in the event that the Trustee acquires any conflicting interest it must eliminate such conflict within 90 days, apply to the SEC for permission to continue as trustee or resign. Any Agent may do the same with like rights and duties. The Trustee is also subject to Section 7.09 hereof.

SECTION 7.04. <u>Trustee's Disclaimer.</u> The Trustee shall not be responsible for and makes no representation as to the validity or adequacy of this Indenture or the Notes, it shall not be accountable for the Issuer's use of the proceeds from the Notes or any money paid to the Issuer or upon the Issuer's direction under any provision of this Indenture, it shall not be responsible for the use or application of any money received by any Paying Agent other than the Trustee, and it shall not be responsible for any statement or recital herein or any statement in the Notes or any other document in connection with the sale of the Notes or pursuant to this Indenture other than its certificate of authentication.

The Trustee shall not be responsible or liable for noncompliance by the Issuer or the Depositary. The Trustee also shall not be responsible or liable for any failure of the Issuer or any other party to comply with any securities laws, including, without limitation, the Securities Act, that may be caused by or result from the failure of the Issuer to comply with the requirements of the Indenture or the failure of the Depositary to comply with any request related to this Indenture.

The Trustee shall not have any obligation or duty to monitor, determine or inquire as to compliance with any restrictions on transfer imposed under this Indenture or under applicable law with respect to any transfer of any interest in any Note (including any transfers between or among the depositary participants, members or beneficial owners in any Global Note) other than to require delivery of such certificates and other documentation or evidence as are expressly required by, and to do so if and when expressly required by, the terms of this Indenture, and to examine the same to determine substantial compliance as to form with the express requirements hereof.

SECTION 7.05. <u>Notice of Defaults</u>. If a Default occurs and is continuing and if it is known to the Trustee, the Trustee shall send to Holders of Notes a notice of the Default within 90 days after it occurs. Except in the case of a Default relating to the payment of principal, premium, if any, or interest on any Note, the Trustee may withhold from the Holders notice of any continuing Default if and so long as a committee of its Responsible Officers in good faith determines that withholding the notice is in the interests of the Holders of the Notes.

SECTION 7.06. Compensation and Indemnity. The Issuer shall pay to the Trustee from time to time such compensation for its acceptance of this Indenture and services hereunder as the parties shall agree in writing from time to time. The Trustee's compensation shall not be limited by any law on compensation of a trustee of an express trust. The Issuer shall reimburse the Trustee promptly upon request for all reasonable disbursements, advances and expenses incurred or made by it in addition to the compensation for its services. Such expenses shall include the reasonable compensation, disbursements and expenses of the Trustee's agents and counsel.

The Issuer and the Guarantors, jointly and severally, shall indemnify the Trustee and its officers, directors, employees, agents and any predecessor trustee and its officers, directors, employees and agents for, and hold the Trustee harmless against, any and all loss, damage, claims, liability or expense (including attorneys' fees) incurred by it in connection with the acceptance or administration of this trust and the performance of its duties hereunder (including the costs and expenses of enforcing this Indenture against the Issuer or any of the Guarantors (including this Section 7.06) or defending itself against any claim whether asserted by any Holder, the Issuer or any Guarantor, or liability in connective with the acceptance, exercise or performance of any of its powers or duties hereunder). The Trustee shall notify the Issuer promptly of any claim for which it may seek indemnity. Failure by the Trustee to so notify the Issuer shall not relieve the Issuer of its obligations hereunder. The Issuer shall defend the claim and the Trustee may have separate counsel and the Issuer shall pay the fees and expenses of such counsel. The Issuer need not reimburse any expense or indemnify against any loss, liability or expense incurred by the Trustee through the Trustee's own willful misconduct, negligence or bad faith.

The obligations of the Issuer under this Section 7.06 shall survive the satisfaction and discharge of this Indenture or the earlier resignation or removal of the Trustee.

Notwithstanding anything contrary in Section 4.12 hereof, to secure the payment obligations of the Issuer and the Guarantors in this Section 7.06, the Trustee shall have a Lien prior to the Notes on all money or property held or collected by the Trustee, except that held in trust to pay principal and interest on particular Notes. Such Lien shall survive the satisfaction and discharge of this Indenture.

When the Trustee incurs expenses or renders services after an Event of Default specified in Section 6.01(6) or (7) hereof occurs, the expenses and the compensation for the services (including the fees and expenses of its agents and counsel) are intended to constitute expenses of administration under any Bankruptcy Law.

SECTION 7.07. <u>Replacement of Trustee</u>. A resignation or removal of the Trustee and appointment of a successor Trustee shall become effective only upon the successor Trustee's acceptance of appointment as provided in this Section 7.07. The Trustee may resign in writing at any time and be discharged from the trust hereby created by so notifying the Issuer. The Holders of a majority in principal amount of the then outstanding Notes may remove the Trustee by so notifying the Trustee and the Issuer in writing. The Issuer may remove the Trustee if:

- (A) the Trustee is adjudged a bankrupt or an insolvent or an order for relief is entered with respect to the Trustee under any Bankruptcy Law;
 - (B) a custodian or public officer takes charge of the Trustee or its property; or
 - (C) the Trustee becomes incapable of acting.

If the Trustee resigns or is removed or if a vacancy exists in the office of Trustee for any reason, the Issuer shall promptly appoint a successor Trustee. Within one year after the successor Trustee takes office, the Holders of a majority in principal amount of the then outstanding Notes may appoint a successor Trustee to replace the successor Trustee appointed by the Issuer.

If a successor Trustee does not take office within 60 days after the retiring Trustee resigns or is removed, the retiring Trustee (at the Issuer's expense), the Issuer or the Holders of at least 10% in principal amount of the then outstanding Notes may petition any court of competent jurisdiction for the appointment of a successor Trustee.

If the Trustee, after written request by any Holder who has been a Holder for at least six months, fails to comply with Section 7.09 hereof, such Holder may petition any court of competent jurisdiction for the removal of the Trustee and the appointment of a successor Trustee.

A successor Trustee shall deliver a written acceptance of its appointment to the retiring Trustee and to the Issuer. Thereupon, the resignation or removal of the retiring Trustee shall become effective, and the successor Trustee shall have all the rights, powers and duties of the Trustee under this Indenture. The successor Trustee shall send a notice of its succession to Holders. The retiring Trustee shall promptly transfer all property held by it as Trustee to the successor Trustee; provided all sums owing to the

Trustee hereunder have been paid and subject to the Lien provided for in Section 7.06 hereof. Notwithstanding replacement of the Trustee pursuant to this Section 7.07, the Issuer's obligations under Section 7.06 hereof shall continue for the benefit of the retiring Trustee.

SECTION 7.08. <u>Successor Trustee by Merger, etc.</u> If the Trustee consolidates, merges or converts into, or transfers all or substantially all of its corporate trust business to, another corporation, the successor corporation without any further act shall be the successor Trustee.

SECTION 7.09. <u>Eligibility</u>; <u>Disqualification</u>. There shall at all times be a Trustee hereunder that is a corporation organized and doing business under the laws of the United States of America or of any state thereof that is authorized under such laws to exercise corporate trustee power, that is subject to supervision or examination by federal or state authorities and that has, together with its parent, a combined capital and surplus of at least \$50,000,000 as set forth in its most recent published annual report of condition.

SECTION 7.10. <u>Incumbency Certificate</u>; <u>Specimen Signatures</u>. The Issuer shall furnish, within five (5) Business Days following the Issue Date, to the Trustee, and from time to time thereafter may furnish, an Officer's Certificate identifying and certifying the incumbency and specimen signatures of the Authorized Persons of the Issuer. Until the Trustee receives a subsequent Officer's Certificate, the Trustee shall be entitled to conclusively rely on the last such Officer's Certificate delivered to it for purposes of determining the Authorized Persons of the Issuer.

ARTICLE VIII

LEGAL DEFEASANCE AND COVENANT DEFEASANCE

SECTION 8.01. Option to Effect Legal Defeasance or Covenant Defeasance. The Issuer may, at its option and at any time, elect to have either Section 8.02 or 8.03 hereof applied to all outstanding Notes upon compliance with the conditions set forth below in this Article 8.

SECTION 8.02. <u>Legal Defeasance and Discharge</u>. Upon the Issuer's exercise under Section 8.01 hereof of the option applicable to this Section 8.02, the Issuer and the Guarantors shall, subject to the satisfaction of the conditions set forth in Section 8.04 hereof, be deemed to have been discharged from their obligations with respect to all outstanding Notes and Guarantees on the date the conditions set forth below are satisfied ("<u>Legal Defeasance</u>"). For this purpose, Legal Defeasance means that the Issuer shall be deemed to have paid and discharged the entire Indebtedness represented by the outstanding Notes, which shall thereafter be deemed to be "outstanding" only for the purposes of Section 8.05 hereof and the other Sections of this Indenture referred to in (a) and (b) below, and to have satisfied all its other obligations under such Notes and this Indenture including that of the Guarantors (and the Trustee, on demand of and at the expense of the Issuer, shall execute proper instruments acknowledging the same), except for the following provisions which shall survive until otherwise terminated or discharged hereunder:

- (A) the rights of Holders of Notes to receive payments in respect of the principal of, premium, if any, and interest on the Notes when such payments are due solely out of the trust created pursuant to this Indenture referred to in Section 8.04 hereof;
- (B) the Issuer's obligations with respect to Notes concerning issuing temporary Notes, registration of such Notes, mutilated, destroyed, lost or stolen Notes and the maintenance of an office or agency for payment and money for security payments held in trust;
 - (C) the rights, powers, trusts, duties and immunities of the Trustee, and the Issuer's obligations in connection therewith; and
 - (D) this Section 8.02.

Subject to compliance with this Article 8, the Issuer may exercise its option under this Section 8.02 notwithstanding the prior exercise of its option under Section 8.03 hereof.

If the Issuer exercises its legal defeasance option, the First Liens, as they pertain to the Notes and the Guarantees, will be released and each Guaranter will be released from all its obligations under its Guarantee of the Notes.

SECTION 8.03. Covenant Defeasance. Upon the Issuer's exercise under Section 8.01 hereof of the option applicable to this Section 8.03, the Issuer and the Guarantors shall, subject to the satisfaction of the conditions set forth in Section 8.04 hereof, be released from their obligations under the covenants contained in Sections 4.03, 4.04, 4.05, 4.07, 4.08, 4.09, 4.10, 4.11, 4.12, 4.13, 4.14 and 4.15 hereof and clauses (4) and (5) of Section 5.01(a), clause (4) of Section 5.01(c), Sections 5.01(e) and 5.01(f) hereof with respect to the outstanding Notes on and after the date the conditions set forth in Section 8.04 hereof are satisfied ("Covenant Defeasance"), and the Notes shall thereafter be deemed not "outstanding" for the purposes of any direction, waiver, consent or declaration or act of Holders (and the consequences of any thereof) in connection with such covenants, but shall continue to be deemed "outstanding" for all other purposes hereunder (it being understood that such Notes shall not be deemed outstanding for accounting purposes). For this purpose, Covenant Defeasance means that, with respect to the outstanding Notes, the Issuer may omit to comply with and shall have no liability in respect of any term, condition or limitation set forth in any such covenant, whether directly or indirectly, by reason of any reference elsewhere herein to any such covenant or by reason of any reference in any such covenant to any other provision herein or in any other document and such omission to comply shall not constitute a Default or an Event of Default under Section 6.01 hereof, but, except as specified above, the remainder of this Indenture and such Notes shall be unaffected thereby. In addition, upon the Issuer's exercise under Section 8.01 hereof of the option applicable to this Section 8.03 hereof,

subject to the satisfaction of the conditions set forth in Section 8.04 hereof, Sections 6.01(3) (solely with respect to the covenants that are released upon a Covenant Defeasance), 6.01(4), 6.01(5), 6.01(6) (solely with respect to Holdings III and its Restricted Subsidiaries other than the Issuer), 6.01(7) (solely with respect to Holdings III and its Restricted Subsidiaries other than the Issuer) and 6.01(8) hereof shall not constitute Events of Default.

If the Issuer exercises its covenant defeasance option, the First Liens, as they pertain to the Notes and the Guarantees, will be released and each Guarantor will be released from all its obligations under its Guarantee of the Notes.

SECTION 8.04. <u>Conditions to Legal or Covenant Defeasance.</u> The following shall be the conditions to the application of either Section 8.02 or 8.03 hereof to the outstanding Notes:

In order to exercise either Legal Defeasance or Covenant Defeasance with respect to the Notes:

- (1) the Issuer must irrevocably deposit with the Trustee, in trust, for the benefit of the Holders of the Notes, cash in U.S. dollars, U.S. dollar-denominated Government Securities, or a combination thereof, in such amounts as will be sufficient, in the opinion of a nationally recognized firm of independent public accountants, to pay the principal of, premium, if any, and interest due on the Notes on the stated maturity date or on the Redemption Date, as the case may be, of such principal, premium, if any, or interest on such Notes and the Issuer must specify whether such Notes are being defeased to maturity or to a particular Redemption Date.
- (2) in the case of Legal Defeasance, the Issuer shall have delivered to the Trustee an Opinion of Counsel reasonably acceptable to the Trustee confirming that, subject to customary assumptions and exclusions,
 - (A) the Issuer has received from, or there has been published by, the United States Internal Revenue Service a ruling, or
 - (B) since the issuance of the Notes, there has been a change in the applicable U.S. federal income tax law,

in either case to the effect that, and based thereon such Opinion of Counsel shall confirm that, subject to customary assumptions and exclusions, the Holders of the Notes will not recognize income, gain or loss for U.S. federal income tax purposes, as applicable, as a result of such Legal Defeasance and will be subject to U.S. federal income tax on the same amounts, in the same manner and at the same times as would have been the case if such Legal Defeasance had not occurred;

- (3) in the case of Covenant Defeasance, the Issuer shall have delivered to the Trustee an Opinion of Counsel reasonably acceptable to the Trustee confirming that, subject to customary assumptions and exclusions, the Holders of the Notes will not recognize income, gain or loss for U.S. federal income tax purposes as a result of such Covenant Defeasance and will be subject to such tax on the same amounts, in the same manner and at the same times as would have been the case if such Covenant Defeasance had not occurred;
- (4) no Default (other than that resulting from borrowing funds to be applied to make such deposit and any similar and simultaneous deposit relating to other Indebtedness and, in each case, the granting of Liens in connection therewith) shall have occurred and be continuing on the date of such deposit;
- (5) such Legal Defeasance or Covenant Defeasance shall not result in a breach or violation of, or constitute a default under the Senior Credit Facilities, the Existing Secured Notes, the Existing Senior Notes, the Existing Senior Subordinated Notes, the indentures pursuant to which the Existing Senior Notes were issued, the indenture pursuant to which the Existing Senior Subordinated Notes were issued or any other material agreement or instrument (other than this Indenture) to which, the Issuer or any Guarantor is a party or by which the Issuer or any Guarantor is bound (other than that resulting from any borrowing of funds to be applied to make the deposit required to effect such Legal Defeasance or Covenant Defeasance and any similar and simultaneous deposit relating to other Indebtedness, and the granting of Liens in connection therewith);
- (6) the Issuer shall have delivered to the Trustee an Opinion of Counsel to the effect that, as of the date of such opinion and subject to customary assumptions and exclusions following the deposit, the trust funds will not be subject to the effect of any applicable bankruptcy, insolvency, reorganization, or similar laws affecting creditors' rights generally (including Section 547 of Title 11 of the United States Code) under any applicable U.S. Federal or state law, and that the Trustee has a perfected security interest in such trust funds for the ratable benefit of the Holders;
- (7) the Issuer shall have delivered to the Trustee an Officer's Certificate stating that the deposit was not made by the Issuer with the intent of defeating, hindering, delaying or defrauding any creditors of the Issuer or any Guarantor or others; and
- (8) the Issuer shall have delivered to the Trustee an Officer's Certificate and an Opinion of Counsel (which Opinion of Counsel may be subject to customary assumptions and exclusions) each stating that all conditions precedent provided for or relating to the Legal Defeasance or the Covenant Defeasance, as the case may be, have been complied with.

SECTION 8.05. <u>Deposited Money and Government Securities to Be Held in Trust; Other Miscellaneous Provisions.</u> Subject to Section 8.06 hereof, all money and Government Securities (including the proceeds thereof) deposited with the Trustee (or other qualifying trustee, collectively for purposes of this Section 8.05, the "<u>Trustee</u>") pursuant to Section 8.04 hereof in respect of the outstanding Notes shall be held in trust and applied by the Trustee, in accordance with the provisions of such Notes and this Indenture, to the payment, either directly or through any Paying Agent (including the Issuer or a Guarantor acting as Paying Agent) as the Trustee may determine, to the Holders of such Notes of all sums due and to become due thereon in respect of principal, premium and interest, but such money need not be segregated from other funds except to the extent required by law.

The Issuer shall pay and indemnify the Trustee against any tax, fee or other charge imposed on or assessed against the cash or Government Securities deposited pursuant to Section 8.04 hereof or the principal and interest received in respect thereof other than any such tax, fee or other charge which by law is for the account of the Holders of the outstanding Notes.

Anything in this Article 8 to the contrary notwithstanding, the Trustee shall deliver or pay to the Issuer from time to time upon the request of the Issuer any money or Government Securities held by it as provided in Section 8.04 hereof which, in the opinion of a nationally recognized firm of independent public accountants expressed in a written certification thereof delivered to the Trustee (which may be the opinion delivered under Section 8.04(a) hereof), are in excess of the amount thereof that would then be required to be deposited to effect an equivalent Legal Defeasance or Covenant Defeasance.

SECTION 8.06. Repayment to Issuer. Subject to any applicable abandoned property law, any money deposited with the Trustee or any Paying Agent, or then held by the Issuer, in trust for the payment of the principal of, premium, if any, or interest on any Note and remaining unclaimed for two years after such principal, and premium, if any, or interest has become due and payable shall be paid to the Issuer on its request or (if then held by the Issuer) shall be discharged from such trust; and the Holder of such Note shall thereafter look only to the Issuer for payment thereof, and all liability of the Trustee or such Paying Agent with respect to such trust money, and all liability of the Issuer as trustee thereof, shall thereupon cease.

SECTION 8.07. Reinstatement. If the Trustee or Paying Agent is unable to apply any United States dollars or Government Securities in accordance with Section 8.02 or 8.03 hereof, as the case may be, by reason of any order or judgment of any court or governmental authority enjoining, restraining or otherwise prohibiting such application, then the Issuer's obligations under this Indenture and the Notes shall be revived and reinstated as though no deposit had occurred pursuant to Section 8.02 or 8.03 hereof until such time as the Trustee or Paying Agent is permitted to apply all such money in accordance with Section 8.02 or 8.03 hereof, as the case may be; provided that,

if the Issuer makes any payment of principal of, premium, if any, or interest on any Note following the reinstatement of its obligations, the Issuer shall be subrogated to the rights of the Holders of such Notes to receive such payment from the money held by the Trustee or Paying Agent.

ARTICLE IX

AMENDMENT, SUPPLEMENT AND WAIVER

SECTION 9.01. Without Consent of Holders of Notes. Notwithstanding Section 9.02 hereof, the Issuer, the Guarantors and the Trustee may amend or supplement this Indenture and any Guarantee or Notes without the consent of any Holder:

- (1) to cure any ambiguity, omission, mistake, defect or inconsistency;
- (2) to provide for uncertificated Notes of such series in addition to or in place of certificated Notes;
- (3) to comply with Section 5.01 hereof;
- (4) to provide the assumption of the Issuer's or any Guarantor's obligations to the Holders;
- (5) to make any change that would provide any additional rights or benefits to the Holders or that does not adversely affect the legal rights under this Indenture of any such Holder;
 - (6) to add covenants for the benefit of the Holders or to surrender any right or power conferred upon the Issuer or any Guarantor;
- (7) to evidence and provide for the acceptance and appointment under this Indenture of a successor Trustee hereunder pursuant to the requirements hereof;
 - (8) to add a Guarantor under this Indenture or to remove any Parent Guarantor that is not a Restricted Parent Guarantor;
- (9) to conform the text of this Indenture, Guarantees or the Notes to any provision of the "Description of the Notes" section of the Offering Memorandum to the extent that such provision in such "Description of the notes" section was intended to be a verbatim recitation of a provision of this Indenture, Guarantee or Notes; or
- (10) to make any amendment to the provisions of this Indenture relating to the transfer and legending of Notes as permitted by this Indenture, including, without limitation to facilitate the issuance and administration of the Notes; <u>provided</u>, that (i) compliance with this Indenture as so amended would not result in Notes being transferred in violation of the Securities Act or any applicable securities law and (ii) such amendment does not materially and adversely affect the rights of Holders to transfer Notes.

(11) to add additional assets as Collateral or to release any Collateral from the liens securing the Notes, in each case pursuant to the terms of this Indenture, the Collateral Documents relating to the Notes and the Intercreditor Agreement, as and when permitted or required by this Indenture, the Collateral Documents relating to the Notes or the Intercreditor Agreement.

In addition, the Collateral Agent and the Trustee are authorized to amend the Collateral Documents relating to the Notes to comply with the provisions hereof and thereof.

Upon the request of the Issuer accompanied by a resolution of its board of directors authorizing the execution of any such amended or supplemental indenture, and upon receipt by the Trustee of the documents described in Section 7.02 hereof, the Trustee shall join with the Issuer and the Guarantors in the execution of any amended or supplemental indenture authorized or permitted by the terms of this Indenture and to make any further appropriate agreements and stipulations that may be therein contained, but the Trustee shall have the right, but not be obligated to, enter into such amended or supplemental indenture that affects its own rights, duties or immunities under this Indenture or otherwise. Notwithstanding the foregoing, neither an Opinion of Counsel nor an Officer's Certificate shall be required in connection with the addition of a Guarantor under this Indenture (other than as required by Section 4.15 hereof) upon execution and delivery by such Guarantor and the Trustee of a supplemental indenture to this Indenture, the form of which is attached as Exhibit D hereto.

SECTION 9.02. With Consent of Holders of Notes. Except as provided below in this Section 9.02, the Issuer, the Guarantors and the Trustee may amend or supplement this Indenture, the Notes, any Guarantee, the Collateral Documents relating to the Notes with the consent of the Holders of at least a majority in principal amount of the Notes (including Additional Notes, if any) then outstanding voting as a single class (including consents obtained in connection with a tender offer or exchange offer for, or purchase of, the Notes), and, subject to Sections 6.04 and 6.07 hereof, any existing Default or Event of Default (other than a Default or Event of Default in the payment of the principal of, premium, if any, or interest on the Notes, except a payment default resulting from an acceleration that has been rescinded) or compliance with any provision of this Indenture, any Guarantee, the Collateral Documents relating to the Notes or the Notes may be waived with the consent of the Holders of a majority in principal amount of the then outstanding Notes (including Additional Notes, if any) voting as a single class (including consents obtained in connection with a tender offer or exchange offer for, or purchase of, the Notes).

Upon the request of the Issuer accompanied by a resolution of its board of directors authorizing the execution of any such amended or supplemental indenture, and upon the filing with the Trustee of evidence satisfactory to the Trustee of the consent of the Holders of Notes as aforesaid, and upon receipt by the Trustee of the documents described in Section 7.02 hereof, the Trustee shall join with the Issuer in the execution of such amended or supplemental indenture unless such amended or supplemental indenture directly affects the Trustee's own rights, duties or immunities under this Indenture or otherwise, in which case the Trustee may in its discretion, but shall not be obligated to, enter into such amended or supplemental indenture.

It shall not be necessary for the consent of the Holders of Notes under this Section 9.02 to approve the particular form of any proposed amendment or waiver, but it shall be sufficient if such consent approves the substance thereof.

After an amendment, supplement or waiver under this Section 9.02 becomes effective, the Issuer shall send to the Holders of Notes affected thereby a notice briefly describing the amendment, supplement or waiver. Any failure of the Issuer to send such notice, or any defect therein, shall not, however, in any way impair or affect the validity of any such amended or supplemental indenture or waiver.

Without the consent of each affected Holder of Notes, an amendment or waiver under this Section 9.02 may not (with respect to any Notes held by a non-consenting Holder):

- (1) reduce the principal amount of such Notes whose Holders must consent to an amendment, supplement or waiver;
- (2) reduce the principal of or change the fixed final maturity of any such Note or alter or waive the provisions with respect to the redemption of such Note (other than provisions relating to Section 3.09, Section 4.10 and Section 4.14 hereof to the extent that any such amendment or waiver does not have the effect of reducing the principal of or changing the fixed final maturity of any such Note or altering or waiving the provisions with respect to the redemption of such Notes);
 - (3) reduce the rate of or change the time for payment of interest on any Note;
- (4) waive a Default in the payment of principal of or premium, if any, or interest on the Notes, except a rescission of acceleration of the Notes by the Holders of at least a majority in aggregate principal amount of the Notes and a waiver of the payment default that resulted from such acceleration, or in respect of a covenant or provision contained in this Indenture or any Guarantee which cannot be amended or modified without the consent of all Holders;
 - (5) make any Note payable in money other than that stated therein;

- (6) make any change in the provisions of this Indenture relating to waivers of past Defaults or the rights of Holders to receive payments of principal of or premium, if any, or interest on the Notes;
 - (7) make any change in these amendment and waiver provisions;
- (8) impair the right of any Holder to receive payment of principal of, or interest on such Holder's Notes on or after the due dates therefor or to institute suit for the enforcement of any payment on or with respect to such Holder's Notes;
 - (9) make any change to or modify the ranking of the Notes that would adversely affect the Holders;
- (10) except as expressly permitted by this Indenture, modify the Guarantees of any Restricted Parent Guarantor or Significant Subsidiary (or any group of Subsidiaries that together would constitute a Significant Subsidiary) in any manner adverse to the Holders of the Notes; or
- (11) make any change in the provisions described under Section 4.05(b)—(h) hereof that adversely affects the rights of any Holder of Notes or amend the terms of any Notes or this Indenture in a way that would result in the loss of an exemption from any of the Taxes described in such Section.

Without the consent of at least two-thirds in aggregate principal amount of Notes then outstanding, an amendment or waiver may not:

- (1) modify any Collateral Document relating to the Notes or the provisions of this Indenture dealing with the Collateral Documents or the application of trust moneys, or otherwise release all or substantially all of the Collateral, except as otherwise permitted by this Indenture or the Collateral Documents; or
- (2) modify the Intercreditor Agreement in any manner materially adverse to the Holders except as otherwise permitted by this Indenture or the Collateral Documents.

SECTION 9.03. Revocation and Effect of Consents. Until an amendment, supplement or waiver becomes effective, a consent to it by a Holder of a Note is a continuing consent by the Holder of a Note and every subsequent Holder of a Note or portion of a Note that evidences the same debt as the consenting Holder's Note, even if notation of the consent is not made on any Note. However, any such Holder of a Note or subsequent Holder of a Note may revoke the consent as to its Note if the Trustee receives written notice of revocation before the date the waiver, supplement or amendment becomes effective. An amendment, supplement or waiver becomes effective in accordance with its terms and thereafter binds every Holder.

The Issuer may, but shall not be obligated to, fix a record date for the purpose of determining the Holders entitled to consent to any amendment, supplement, or waiver. If a record date is fixed, then, notwithstanding the preceding paragraph, those Persons who were Holders at such record date (or their duly designated proxies), and only such Persons, shall be entitled to consent to such amendment, supplement, or waiver or to revoke any consent previously given, whether or not such Persons continue to be Holders after such record date. No such consent shall be valid or effective for more than 120 days after such record date unless the consent of the requisite number of Holders has been obtained.

SECTION 9.04. <u>Notation on or Exchange of Notes.</u> The Trustee may place an appropriate notation about an amendment, supplement or waiver on any Note thereafter authenticated. The Issuer in exchange for all Notes may issue and the Trustee shall, upon receipt of an Authentication Order, authenticate new Notes that reflect the amendment, supplement or waiver.

Failure to make the appropriate notation or issue a new Note shall not affect the validity and effect of such amendment, supplement or waiver.

SECTION 9.05. <u>Trustee to Sign Amendments, etc.</u> The Trustee shall sign, and shall direct the Collateral Agent to sign (as applicable), any amendment, supplement or waiver authorized pursuant to this Article 9 if the amendment or supplement does not adversely affect the rights, duties, liabilities or immunities of the Trustee and the Collateral Agent, as applicable. The Issuer may not sign an amendment, supplement or waiver until the board of directors of the Issuer approves it. In executing any amendment, supplement or waiver, the Trustee and the Collateral Agent shall be entitled to receive, upon request, and (subject to Section 7.01 hereof) shall be fully protected in relying upon, in addition to the documents required by Section 13.03 hereof, an Officer's Certificate and an Opinion of Counsel stating that the execution of such amended or supplemental indenture is authorized or permitted by this Indenture and that such amendment, supplement or waiver is the legal, valid and binding obligation of the Issuer and any Guarantors party thereto, enforceable against them in accordance with its terms, subject to customary exceptions, and complies with the provisions hereof. Notwithstanding the foregoing, except as required by Section 4.15 hereof, neither an Opinion of Counsel nor an Officer's Certificate will be required for the Trustee to execute any amendment or supplement adding a new Guarantor under this Indenture.

SECTION 9.06. <u>Payment for Consent.</u> Neither the Issuer, Holdings III nor any Affiliate of the Issuer shall, directly or indirectly, pay or cause to be paid any consideration, whether by way of interest, fee or otherwise, to any Holder for or as an inducement to any consent, waiver or amendment of any of the terms or provisions of this Indenture or the Notes unless such consideration is offered to all Holders and is paid to all Holders that so consent, waive or agree to amend in the time frame set forth in solicitation documents relating to such consent, waiver or agreement.

SECTION 9.07. <u>Additional Voting Terms; Calculation of Principal Amount.</u> Except as provided in the proviso to the first sentence of Section 9.02, all Notes issued under this Indenture shall vote and consent together on all matters (as to which any of such Notes may vote) as one class and no series of Notes will have the right to vote or consent as a separate series on any matter. Determinations as to whether Holders of the requisite aggregate principal amount of Notes have concurred in any direction, waiver or consent shall be made in accordance with this Article Nine.

ARTICLE X

GUARANTEES

SECTION 10.01. <u>Guarantee</u>. Subject to this Article 10, each of the Guarantors hereby, jointly and severally, unconditionally guarantees to each Holder of a Note authenticated and delivered by the Trustee and to the Trustee and its successors and assigns, irrespective of the validity and enforceability of this Indenture, the Notes or the obligations of the Issuer hereunder or thereunder, that: (a) the principal of and interest and premium, if any, on the Notes shall be promptly paid in full when due, whether at maturity, by acceleration, redemption or otherwise, and interest on the overdue principal of and interest on the Notes, if any, if lawful, and all other obligations of the Issuer to the Holders or the Trustee hereunder or thereunder shall be promptly paid in full or performed, all in accordance with the terms hereof and thereof; and (b) in case of any extension of time of payment or renewal of any Notes or any of such other obligations, that same shall be promptly paid in full when due or performed in accordance with the terms of the extension or renewal, whether at stated maturity, by acceleration or otherwise. Failing payment when due of any amount so guaranteed or any performance so guaranteed for whatever reason, the Guarantors shall be jointly and severally obligated to pay the same immediately. Each Guarantor agrees that this is a guarantee of payment and not a guarantee of collection.

The Guarantors hereby agree that their obligations hereunder shall be unconditional, irrespective of the validity, regularity or enforceability of the Notes or this Indenture, the absence of any action to enforce the same, any waiver or consent by any Holder of the Notes with respect to any provisions hereof or thereof, the recovery of any judgment against the Issuer, any action to enforce the same or any other circumstance which might otherwise constitute a legal or equitable discharge or defense of a guarantor. Each Guarantor hereby waives diligence, presentment, demand of payment, filing of claims with a court in the event of insolvency or bankruptcy of the Issuer, any right to require a proceeding first against the Issuer, protest, notice and all demands whatsoever and covenants that this Guarantee shall not be discharged except by complete performance of the obligations contained in the Notes and this Indenture.

Each Guarantor also agrees to pay any and all costs and expenses (including reasonable attorneys' fees) incurred by the Trustee or any Holder in enforcing any rights under this Section 10.01.

If any Holder or the Trustee is required by any court or otherwise to return to the Issuer, the Guarantors or any custodian, trustee, liquidator or other similar official acting in relation to either the Issuer or the Guarantors, any amount paid either to the Trustee or such Holder, this Guarantee, to the extent theretofore discharged, shall be reinstated in full force and effect.

Each Guarantor agrees that it shall not be entitled to any right of subrogation in relation to the Holders in respect of any obligations guaranteed hereby until payment in full of all obligations guaranteed hereby. Each Guarantor further agrees that, as between the Guarantors, on the one hand, and the Holders and the Trustee, on the other hand, (x) the maturity of the obligations guaranteed hereby may be accelerated as provided in Article 6 hereof for the purposes of this Guarantee, notwithstanding any stay, injunction or other prohibition preventing such acceleration in respect of the obligations guaranteed hereby, and (y) in the event of any declaration of acceleration of such obligations as provided in Article 6 hereof, such obligations (whether or not due and payable) shall forthwith become due and payable by the Guarantors for the purpose of this Guarantee. The Guarantors shall have the right to seek contribution from any non-paying Guarantor so long as the exercise of such right does not impair the rights of the Holders under the Guarantees.

Each Guarantee shall remain in full force and effect and continue to be effective should any petition be filed by or against the Issuer for liquidation, reorganization, should the Issuer become insolvent or make an assignment for the benefit of creditors or should a receiver or trustee be appointed for all or any significant part of the Issuer's assets, and shall, to the fullest extent permitted by law, continue to be effective or be reinstated, as the case may be, if at any time payment and performance of the Notes are, pursuant to applicable law, rescinded or reduced in amount, or must otherwise be restored or returned by any obligee on the Notes or Guarantees, whether as a "voidable preference," "fraudulent transfer" or otherwise, all as though such payment or performance had not been made. In the event that any payment or any part thereof, is rescinded, reduced, restored or returned, the Notes shall, to the fullest extent permitted by law, be reinstated and deemed reduced only by such amount paid and not so rescinded, reduced, restored or returned.

In case any provision of any Guarantee shall be invalid, illegal or unenforceable, the validity, legality, and enforceability of the remaining provisions shall not in any way be affected or impaired thereby.

The Guarantees issued by each Unrestricted Parent Guarantor shall be a general unsecured senior obligation of such Guarantor and shall be <u>pari passu</u> in right of payment with all existing and future Senior Indebtedness of such Guarantor. The Guarantees issued by each Secured Guarantor will be senior secured obligations of such Guarantor and shall be <u>pari passu</u> in right of payment with all existing and future First Lien Obligations and Senior Indebtedness of such Guarantor.

Each payment to be made by a Guarantor in respect of its Guarantee shall be made without set-off, counterclaim, reduction or diminution of any kind or nature.

SECTION 10.02. <u>Limitation on Guarantor Liability.</u> Each Guarantor, and by its acceptance of Notes, each Holder, hereby confirms that it is the intention of all such parties that the Guarantee of such Guarantor not constitute a fraudulent transfer or conveyance for purposes of Bankruptcy Law, the Uniform Fraudulent Conveyance Act, the Uniform Fraudulent Transfer Act or any similar federal or state law to the extent applicable to any Guarantee. To effectuate the foregoing intention, the Trustee, the Holders and the Guarantors hereby irrevocably agree that the obligations of each Guarantor shall be limited to the maximum amount as will, after giving effect to such maximum amount and all other contingent and fixed liabilities of such Guarantor that are relevant under such laws and after giving effect to any collections from, rights to receive contribution from or payments made by or on behalf of any other Guarantor in respect of the obligations of such other Guarantor under this Article 10, result in the obligations of such Guarantor under its Guarantee not constituting a fraudulent conveyance or fraudulent transfer under applicable law. Each Subsidiary Guarantor that makes a payment under its Guarantee shall be entitled upon payment in full of all guaranteed obligations under this Indenture to a contribution from each other Subsidiary Guarantor in an amount equal to such other Subsidiary Guarantor's <u>pro rata</u> portion of such payment based on the respective net assets of all the Subsidiary Guarantors at the time of such payment determined in accordance with GAAP.

SECTION 10.03. Execution and Delivery. To evidence its Guarantee set forth in Section 10.01 hereof, each Guarantor hereby agrees that this Indenture shall be executed on behalf of such Guarantor by its President, one of its Vice Presidents or one of its Assistant Vice Presidents.

Each Guarantor hereby agrees that its Guarantee set forth in Section 10.01 hereof shall remain in full force and effect notwithstanding the absence of the endorsement of any notation of such Guarantee on the Notes.

If an Officer whose signature is on this Indenture no longer holds that office at the time the Trustee authenticates the Note, the Guarantee shall be valid nevertheless.

The delivery of any Note by the Trustee, after the authentication thereof hereunder, shall constitute due delivery of the Guarantee set forth in this Indenture on behalf of the Guarantors.

If required by Section 4.15 hereof, the Issuer shall cause any newly created or acquired Restricted Subsidiary to comply with the provisions of Section 4.15 hereof and this Article 10, to the extent applicable.

SECTION 10.04. <u>Subrogation.</u> Each Guarantor shall be subrogated to all rights of Holders of Notes against the Issuer in respect of any amounts paid by any Guarantor pursuant to the provisions of Section 10.01 hereof; <u>provided</u> that, if an Event of Default has occurred and is continuing, no Guarantor shall be entitled to enforce or receive any payments arising out of, or based upon, such right of subrogation until all amounts then due and payable by the Issuer under this Indenture or the Notes shall have been paid in full.

SECTION 10.05. <u>Benefits Acknowledged</u>. Each Guarantor acknowledges that it will receive direct and indirect benefits from the financing arrangements contemplated by this Indenture and that the guarantee and waivers made by it pursuant to its Guarantee are knowingly made in contemplation of such benefits.

SECTION 10.06. <u>Release of Guarantees</u>. A Guarantee by a Guarantor shall be automatically and unconditionally released and discharged, and no further action by such Guarantor, the Issuer or the Trustee is required for the release of such Guarantor's Guarantee, upon:

- (1) (A) any sale, exchange or transfer (by merger or otherwise) of (i) the Capital Stock of such Guarantor (including any sale, exchange or transfer), after which the applicable Guarantor is no longer a Restricted Subsidiary or (ii) all or substantially all the assets of such Guarantor, in each case made in compliance with the applicable provisions of this Indenture;
- (B) the release or discharge of the guarantee by such Guarantor of Indebtedness under all other First Lien Obligations (including the Senior Credit Facilities and the Existing Secured Notes) or such other guarantee that resulted in the creation of such Guarantee, except a discharge or release by or as a result of payment under such guarantee;
- (C) the designation of any Restricted Subsidiary that is a Guarantor as an Unrestricted Subsidiary in compliance with the applicable provisions of this Indenture;
 - (D) the release of an Unrestricted Parent Guarantor of all Senior Credit Agreement Obligations; or
- (E) the exercise by the Issuer of its Legal Defeasance option or Covenant Defeasance option in accordance with Article 8 hereof or the discharge of the Issuer's obligations under this Indenture in accordance with the terms of this Indenture; and
- (2) such Guarantor delivering to the Trustee an Officer's Certificate of such Guarantor and an Opinion of Counsel, each stating that all conditions precedent provided for in this Indenture relating to such transaction have been complied with.

ARTICLE XI

COLLATERAL AND SECURITY

SECTION 11.01. The Collateral Agent.

- (a) Each of the Trustee and, by accepting the Notes, the Holders hereby appoints and authorizes Citibank, N.A. to act as Collateral Agent and in such capacity to act as the agent of (and to hold any security interest created by the Collateral Documents relating to the Notes for and on behalf of or on trust for) the Trustee and each Holders for purposes of acquiring, holding and enforcing any and all Liens on Collateral granted by the Issuer or any Secured Guarantor to secure any of the Obligations, together with such powers and discretion as are reasonably incidental thereto. The use of the term "agent" herein with reference to the Collateral Agent is not intended to connote any fiduciary or other implied (or express) obligations arising under agency doctrine of any applicable law other than as a "representative" as such term is used in Section 9-102(a)(72)(E) of the Uniform Commercial Code. Instead, such term is used merely as a matter of market custom, and is intended to create or reflect only an administrative relationship between independent contracting parties.
- (b) The Collateral Agent shall be subject to such directions as may be given it by the Trustee from time to time as required or permitted by this Indenture and the Intercreditor Agreement. Except as directed by the Trustee and as required or permitted by this Indenture, the Intercreditor Agreement or the other Collateral Documents relating to the Notes, the Collateral Agent shall not be obligated:
 - (i) to act upon directions purported to be delivered to it by any other Person;
 - (ii) to foreclose upon or otherwise enforce any Lien securing the Notes and the Guarantees of the Notes; or
 - (iii) to take any other action whatsoever with regard to any or all of the Liens securing the Notes and the Guarantees of the Notes, the Collateral Documents relating to the Notes or the Collateral.
- (c) The Collateral Agent is authorized and empowered to appoint one or more co-agents or sub-agents or attorneys-in-fact as it deems necessary or appropriate in connection herewith and shall not be liable for the negligence or misconduct of any such agents or attorneys-in-fact selected by it in good faith.
- (d) The Collateral Agent shall be accountable only for amounts that it actually receives as a result of the enforcement of this Indenture, the Collateral Documents relating to the Notes or the Liens created by the Collateral Documents relating to the Notes.

- (e) The Trustee may, from time to time, appoint another financial institution to act as Collateral Agent so long as such institution meets the requirements applicable to the Trustee as set forth in Section 7.09. Subject to the appointment and acceptance of a successor Collateral Agent as provided in this subsection, the Collateral Agent (if other than the Trustee) may resign at any time by notifying the Trustee and the Issuer. Upon any such resignation, the Trustee shall have the right to appoint a successor Collateral Agent. If no successor shall have been so appointed by the Trustee and shall have accepted such appointment within 30 days after the retiring Collateral Agent gives notice of its resignation, then the retiring Collateral Agent may, on behalf of the Holders and the Trustee, appoint a successor Collateral Agent which shall meet the eligibility requirements applicable to the Trustee as set forth in Section 7.09 and shall accept and comply in all material respects with the Collateral Documents. Upon a successor's acceptance of its appointment as Collateral Agent hereunder, such successor shall succeed to and become vested with all the rights, powers, privileges and duties of the retiring Collateral Agent hereunder and under the Collateral Documents, and the retiring Collateral Agent shall be discharged from its duties and obligations hereunder and under the Collateral Documents. If the Trustee shall be acting at any time as the Collateral Agent, then it will be deemed to have resigned as Collateral Agent upon its replacement as Trustee pursuant to Section 7.07, and the successor Trustee shall select (or may act as) the replacement Collateral Agent.
- (f) The Collateral Agent shall have all of the rights of the Trustee under Article VII of this Indenture, including, without limitation, the rights to compensation, indemnification and resignation.
- (g) At all times when the Trustee is not itself the Collateral Agent, the Issuer will deliver to the Trustee copies of all Collateral Documents relating to the Notes delivered to the Collateral Agent and copies of all documents delivered to the Collateral Agent pursuant to the Collateral Documents relating to the Notes.

SECTION 11.02. The Collateral.

(a) The payment of the principal of and interest, and premium, if any, on the Notes when and as the same shall be due and payable, whether on an interest payment date, at maturity, by acceleration, repurchase, redemption or otherwise and whether by the Issuer pursuant to the Notes or by any Secured Guarantor pursuant to its Guarantee and the payment of all other First Lien Obligations of the Issuer and the Guarantors under this Indenture, the Notes, the Guarantees and the Collateral Documents relating to the Notes are secured by First Liens on the Collateral, subject to Permitted Liens, as provided in the Collateral Documents relating to the Notes which the Issuer and the Guarantors have entered into simultaneously with the execution of this Indenture, or in certain circumstances, subsequent to the Issue Date, and will be secured as provided in the Collateral Document relating to the Notes hereafter delivered as required or permitted by this Indenture.

- (b) Each Holder of Notes, by its acceptance of the Notes and the Guarantees of the Notes, will be deemed to have consented and agreed to the terms of each Collateral Document relating to the Notes, as originally in effect and as amended, supplemented or replaced from time to time in accordance with its terms or the terms of this Indenture, to have authorized and directed the Trustee and the Collateral Agent, as applicable, to enter into the Collateral Documents relating to the Notes to which it is a party, and to have authorized and empowered the Trustee and the Collateral Agent, as applicable, and (through the Intercreditor Agreement) the Directing Agent to bind the Holders of Notes and other holders of First Lien Obligations as set forth in the Collateral Documents to which they are a party and to perform its respective obligations and exercise its respective rights and powers thereunder. Notwithstanding the foregoing, no such consent or deemed consent shall be deemed or construed to represent an amendment or waiver, in whole or in part, of any provision of this Indenture or the Notes. The foregoing will not limit the right of the Issuer to amend, waive or otherwise modify the Collateral Documents relating to the Notes in accordance with their terms.
- (c) The Trustee and each Holder, by accepting the Notes and the Guarantees of the Notes, acknowledges that, as more fully set forth in the Collateral Documents relating to the Notes, the Collateral as now or hereafter constituted shall be held by the Collateral Agent for the benefit of all the Holders, the Collateral Agent and the Trustee, and that the Lien granted by the Collateral Documents relating to the Notes in respect of the Trustee and the Holders is subject to and qualified and limited in all respects by the Collateral Documents relating to the Notes and actions that may be taken thereunder. In the event of conflict between the Intercreditor Agreement, any of the other Collateral Documents and this Indenture, the Intercreditor Agreement shall control.

SECTION 11.03. Impairment of Security Interest.

Neither the Issuer nor any Secured Guarantor will take or omit to take any action which would materially adversely affect or impair the Liens in favor of the Collateral Agent and the Holders with respect to the Collateral; <u>provided</u>, <u>however</u>, that the foregoing shall not be deemed to prohibit any action or inaction that is otherwise permitted by this Indenture or required by law.

SECTION 11.04. After-Acquired Collateral. If:

- (a) property (other than Excluded Assets) is acquired by the Issuer or a Secured Guarantor that is intended to be subject to the Lien created by the Collateral Documents relating to the Notes but is not so subject;
 - (b) an Excluded Asset ceases to be an Excluded Asset;
 - (c) a Subsidiary of the Issuer becomes a Secured Guarantor; or

(d) any property of the Issuer or any Secured Guarantor becomes subject to a Lien with respect to any First Lien Obligations (or the Guarantees thereof) and is not already subject to the Lien created by the Collateral Documents relating to the Notes, then the Issuer or such Secured Guarantor will, as soon as practical after such property's acquisition or such property no longer being an Excluded Asset or such Subsidiary becoming a Secured Guarantor or such property becoming subject to a Lien securing any First Lien Obligation (or the Guarantees thereof), as applicable, provide security over such property (or, in the case of a new Secured Guarantor, all of its assets that are not Excluded Assets) in favor of the Collateral Agent on a basis that would create a Lien on such terms, in each case, consistent with the Collateral Documents in effect at such time, and take such additional actions as are reasonable and appropriate or advisable to create and fully perfect in favor of the Secured Parties under the Collateral Documents relating to the Notes a valid and enforceable security interest in such Collateral (to the extent such perfection is required under the Collateral Documents), which shall be free of all other Liens except for Permitted Liens; provided that, with regard to Material Real Property, the Issuer and any Guarantor shall have 90 days (or such longer period as the Trustee may agree in its sole discretion) from the date of acquisition to execute and deliver the items described under Section 11.05 with respect to such real property and with respect to the pledge of equity interests in a Foreign Subsidiary, the Issuer and any Guarantor shall have 90 days or such longer period as the Trustee may agree in its sole discretion from the date of acquisition to provide, execute and deliver the items described in Section 11.05(b). Any security interest provided pursuant to this Section 11.04 (other than with respect to assets specified in (a) and (b) above that are automatically subject to a perfected security interest under the Collateral Documents relating to the Notes) shall be accompanied by such Opinions of Counsel to the Issuer or the Subsidiary Guarantors addressed to the Trustee and the Collateral Agent as are reasonably requested by the Trustee or the Collateral Agent and customarily given by such counsel in the relevant jurisdiction, in form and substance customary for such jurisdiction. In addition, if perfection is required by the Collateral Documents relating to the Notes (other than with respect to assets specified in (a) and (b) above that are automatically subject to a perfected security interest under the Collateral Documents related to the Notes), the Issuer shall deliver an Officer's Certificate to the Trustee and the Collateral Agent upon reasonable request by the Trustee or the Collateral Agent, certifying that the necessary measures have been taken to perfect the security interest in such property.

SECTION 11.05. Real Estate Mortgages and Filing; Pledge of Foreign Collateral.

(a) With respect to Material Real Property that secures (or will secure) the Notes or the Guarantees, the Issuer or the Secured Guarantor must provide the Trustee with filed Mortgages with respect to such owned real property within 90 days (or such longer period as the Trustee may agree in its sole discretion) of the Issue Date or 90 days (or such longer period as the Trustee may agree in its sole discretion) of the acquisition of, or, if requested by the Trustee, entry into, or renewal of, a ground lease in respect of, such real property, as the case may be, in each case together with:

- (i) evidence that counterparts of the Mortgages have been duly executed, acknowledged and delivered and are in form suitable for filing or recording in all filing or recording offices that the Trustee may deem reasonably necessary or desirable in order to create a valid and subsisting perfected Lien on the property and/or rights described therein in favor of the Trustee for the benefit of the Holders, <u>pari passu</u> with the Liens securing the Senior Credit Agreement Obligations, the Existing Secured Notes and the other First Lien Obligations as among the holders thereof in accordance with the Intercreditor Agreement, and that all filing and recording taxes and fees have been paid or otherwise provided for in a manner reasonably satisfactory to the Trustee;
- (ii) fully paid American Land Title Association Lender's Extended Coverage title insurance policies or the equivalent or other form available in each applicable jurisdiction in form and substance, with endorsements and in amount, reasonably acceptable to the Trustee (not to exceed the value of the real properties covered thereby), issued, coinsured and reinsured by title insurers reasonably acceptable to the Trustee, insuring the Mortgages to be valid subsisting Liens on the property described therein, free and clear of all defects and encumbrances, subject to Permitted Liens, and providing for such other affirmative insurance and such coinsurance and direct access reinsurance as the Trustee may reasonably request;
 - (iii) surveys with respect to such owned real property;
- (iv) opinions of local counsel for the Issuer and the Secured Guarantors in states in which the real properties are located, with respect to the enforceability and perfection of the Mortgages and any related fixture filings in form and substance reasonably satisfactory to the Trustee; and
- (v) such other evidence that all other actions that the Trustee may reasonably deem necessary or desirable in order to create valid and subsisting Liens on the property described in the Mortgages has been taken.
- (b) With respect to the equity interests of wholly owned Material Foreign Subsidiaries of Holdings III and Specified Foreign Subsidiaries that secure (or will secure) the Notes or the Guarantees, the Issuer or the Secured Guarantor must provide the Trustee within 90 days (or such longer period as the Trustee may agree in its sole discretion) of the Issue Date or 90 days (or such longer period as the Trustee may agree in its sole discretion) upon the formation or acquisition of a wholly owned Material Foreign Subsidiary of Holdings III or Specified Foreign Subsidiaries: (a) counterparts of each pledge agreement to be entered into in connection with the pledge of the equity interests of each such wholly owned Material Foreign Subsidiary of Holdings III or such Specified Foreign Subsidiary, and all other documents and instruments required by law or reasonably requested by the Trustee to be filed, registered or recorded to create the Liens in such equity interests and to perfect such Liens to the extent required by, this Indenture

and the Collateral Documents relating to the Notes; and (b) a signed copy of an opinion, addressed to the Trustee, of counsel for the Issuer and the Secured Guarantors as reasonably acceptable to the Trustee as to such matters set forth in clause (a), as the Trustee may reasonably request

SECTION 11.06. Release of Collateral.

- (a) Liens on the Collateral will be automatically released without requirement for consent or approval from the Holders, the Trustee or the Collateral Agent:
 - (i) with respect to any Collateral securing the Guarantee of the Notes of any Secured Guarantor, when such Secured Guarantor's Guarantee is released in accordance with the terms of this Indenture;
 - (ii) upon payment in full of principal, interest and all other obligations on the Notes issued under this Indenture;
 - (iii) as provided in Section 9.02;
 - (iv) in connection with any disposition of Collateral (but excluding any transaction subject to Section 5.01 where the recipient is required to become the obligor on the Notes or a Secured Guarantor) that is permitted by this Indenture;
 - (v) with respect to any particular item of Collateral, if there are outstanding Obligations under the Senior Credit Facilities, upon release by Senior Credit Agreement Collateral Agent of the Liens on such item of Collateral securing the Senior Credit Agreement Obligations and the concurrent release of the Liens on such item of Collateral securing any other First Lien Obligations; provided, however, that there is then outstanding under the Senior Credit Facilities aggregate debt and debt commitments in an amount that exceeds the aggregate principal amount of the then outstanding Notes; and provided further, however, that the Senior Credit Agreement Collateral Agent may not release all or substantially all of the Collateral without the consent of the Trustee on behalf of the Holders of the Notes;
 - (vi) with respect to any particular item of Collateral, if there are no outstanding Obligations under the Senior Credit Facilities, upon release by the collateral agent for the largest class of outstanding First Lien Obligations at such time of the Liens on such item of Collateral securing such First Lien Obligations and the concurrent release of the Liens on such item of Collateral securing any other First Lien Obligations; provided, however, that the Applicable Authorized Representative may not release all or substantially all of the Collateral without the consent of the Trustee on behalf of the Holders of the Notes;

(vii) if such property or other assets is or becomes Excluded Assets; or

(viii) upon the exercise by the Issuer of its legal defeasance or covenant defeasance options under Sections 8.02 and 8.03, respectively, or the satisfaction and discharge of the Issuer's obligations under Section 12.01.

In addition, subject to certain limitations set forth in the Collateral Documents, all Collateral used, sold, transferred or otherwise disposed of in accordance with the terms of the applicable First Lien Debt Documents, including any waiver or amendment of these documents, will automatically be released from the Lien securing the Notes or the Guarantees of the Notes so that the use, sale, transfer or other disposition may be made free of such Lien.

(b) At the request of the Issuer, the Trustee shall execute and deliver any documents, instructions or instruments evidencing the consent of the Holders of the Notes to any permitted release. The Trustee and the Collateral Agent shall take such action under this Indenture and the Collateral Documents relating to the Notes or otherwise as may be reasonably requested by the Issuer to give effect to or evidence any such release.

SECTION 11.07. <u>Authorization of Actions to be Taken by the Trustee or the Collateral Agent under the Collateral Documents relating to the Notes.</u>

- (a) Subject to the provisions of the Collateral Documents relating to the Notes and unless otherwise expressly provided herein or therein, the Trustee may, at the written direction of a majority of the Holders, direct the Collateral Agent to take all actions necessary or appropriate in order to (i) enforce any of the terms of the Collateral Documents relating to the Notes and (ii) collect and receive any and all amounts payable in respect of the Collateral in respect of the obligations of the Issuer and the Secured Guarantors hereunder and thereunder. Subject to the provisions of the Collateral Documents relating to the Notes, the Collateral Agent shall have the power to institute and to maintain such suits and proceedings in order to prevent any impairment of the Collateral by any acts that may be unlawful or in violation of the Collateral Documents relating to the Notes or this Indenture, and such suits and proceedings as are necessary to preserve or protect its interest and the interests of the Holders in the Collateral (including power to institute and maintain suits or proceedings to restrain the enforcement of or compliance with any legislative or other governmental enactment, rule or order that may be unconstitutional or otherwise invalid if the enforcement of, or compliance with, such enactment, rule or order would impair the security interest granted pursuant to any Collateral Document relating to the Notes or be prejudicial to the interests of the Holders or the Trustee).
- (b) The Trustee or the Collateral Agent shall not be responsible for the existence, genuineness or value of any of the Collateral or for the validity, perfection, priority or enforceability of the Liens in any of the Collateral, whether impaired by

operation of law or by reason of any action or omission to act on its part hereunder, except to the extent such action or omission constitutes negligence (or gross negligence in the case of the Collateral Agent) or willful misconduct on the part of the Trustee or the Collateral Agent, for the validity or sufficiency of the Collateral or any agreement or assignment contained therein, for the validity of the title of the Issuer to the Collateral, for insuring the Collateral or for the payment of taxes, charges, assessments or Liens upon the Collateral or otherwise as to the maintenance of the Collateral. Notwithstanding the foregoing, neither the Trustee nor the Collateral Agent shall have responsibility for recording, filing, re-recording or refiling any financing statement, continuation statement, document, instrument or other notice in any public office at any time or times or to otherwise take any action to perfect or maintain the perfection of any security interest granted to it under the Collateral Documents relating to the Notes or otherwise.

- (c) Where any provision of the Collateral Documents relating to the Notes requires that additional property or assets be provided as Collateral, the Issuer shall, or shall cause the applicable Secured Guarantors to, take any and all actions reasonably required to cause such additional property or assets to be provided as Collateral and to create and perfect a valid and enforceable first-priority security interest in such property or assets (subject to Permitted Liens and other exceptions in the Collateral Documents relating to the Notes) in favor of the Collateral Agent for the benefit of the Holders in accordance with and to the extent required under the Collateral Documents relating to the Notes.
- (d) The Trustee, in giving any consent or approval under this Indenture or the Collateral Documents relating to the Notes, shall be entitled to receive, as a condition to such consent or approval, an Officer's Certificate to the effect that the action or omission for which consent or approval is to be given does not violate this Indenture or the Collateral Documents relating to the Notes, and the Trustee shall be fully protected in giving such consent or approval on the basis of such Officer's Certificate.

ARTICLE XII

SATISFACTION AND DISCHARGE

SECTION 12.01. <u>Satisfaction and Discharge.</u> This Indenture shall be discharged and shall cease to be of further effect as to all Notes, when either:

- (1) all Notes heretofore authenticated and delivered, except lost, stolen or destroyed Notes which have been replaced or paid and Notes for whose payment money has heretofore been deposited in trust, have been delivered to the Trustee for cancellation; or
- (2) (A) all Notes not heretofore delivered to the Trustee for cancellation have become due and payable by reason of the making of a notice of redemption or otherwise, will become due and payable within one year or are to be called for redemption within one year under arrangements satisfactory to the Trustee for the

giving of notice of redemption by the Trustee in the name, and at the expense, of the Issuer, and the Issuer or any Guarantor has irrevocably deposited or caused to be deposited with the Trustee as trust funds in trust solely for the benefit of the Holders of the Notes, cash in U.S. dollars, U.S. dollar-denominated Government Securities, or a combination thereof, in such amounts as will be sufficient without consideration of any reinvestment of interest to pay and discharge the entire indebtedness on the Notes not heretofore delivered to the Trustee for cancellation for principal, premium, if any, and accrued interest to the date of maturity or redemption;

- (B) no Default (other than that resulting from borrowing funds to be applied to make such deposit or any similar and simultaneous deposit relating to other Indebtedness and the granting of Liens in connection therewith) with respect to this Indenture or the Notes shall have occurred and be continuing on the date of such deposit or shall occur as a result of such deposit and such deposit will not result in a breach or violation of, or constitute a default under the Senior Credit Facilities, the Existing Secured Notes, the Existing Senior Notes, the Existing Senior Subordinated Notes, the indentures pursuant to which the Existing Secured Notes were issued, the indentures pursuant to which the Existing Senior Subordinated Notes were issued or any other material agreement or instrument (other than this Indenture) to which the Issuer or any Guarantor is a party or by which the Issuer or any Guarantor is bound (other than resulting from any borrowing of funds to be applied to make such deposit and any similar and simultaneous deposit relating to other Indebtedness and the granting of Liens in connection therewith);
 - (C) the Issuer has paid or caused to be paid all sums payable by it under this Indenture; and
- (D) the Issuer has delivered irrevocable instructions to the Trustee to apply the deposited money toward the payment of the Notes at maturity or the Redemption Date, as the case may be.

In addition, the Issuer must deliver an Officer's Certificate and an Opinion of Counsel to the Trustee stating that all conditions precedent to satisfaction and discharge have been satisfied.

Notwithstanding the satisfaction and discharge of this Indenture, if money shall have been deposited with the Trustee pursuant to subclause (A) of clause (2) of this Section 12.01, the provisions of Section 12.02 and Section 8.06 hereof shall survive.

SECTION 12.02. <u>Application of Trust Money.</u> Subject to the provisions of Section 8.06 hereof, all money deposited with the Trustee pursuant to Section 12.01 hereof shall be held in trust and applied by it, in accordance with the provisions of the Notes and this Indenture, to the payment, either directly or through any Paying Agent (including the Issuer acting as its own Paying Agent) as the Trustee may determine, to the Persons entitled thereto, of the principal (and premium, if any) and interest for whose payment such money has been deposited with the Trustee; but such money need not be segregated from other funds except to the extent required by law.

If the Trustee or Paying Agent is unable to apply any money or Government Securities in accordance with Section 12.01 hereof by reason of any legal proceeding or by reason of any order or judgment of any court or governmental authority enjoining, restraining or otherwise prohibiting such application, the Issuer's and any Guarantor's obligations under this Indenture and the Notes shall be revived and reinstated as though no deposit had occurred pursuant to Section 12.01 hereof; <u>provided</u> that if the Issuer has made any payment of principal of, premium, if any, or interest on any Notes because of the reinstatement of its obligations, the Issuer shall be subrogated to the rights of the Holders of such Notes to receive such payment from the money or Government Securities held by the Trustee or Paying Agent.

ARTICLE XIII

MISCELLANEOUS

SECTION 13.01. <u>Notices.</u> Any notice or communication by the Issuer, any Guarantor or the Trustee to the others is duly given if in writing and delivered in person or mailed by first-class mail (registered or certified, return receipt requested), fax or overnight air courier guaranteeing next day delivery, to the others' address:

If to the Issuer and/or any Guarantor:

Freescale Semiconductor, Inc. 6501 William Cannon Drive West Austin, Texas 78735 Fax: (512) 996-6853 Attention: General Counsel

If to the Trustee:

Wells Fargo Bank, National Association 750 N. Saint Paul Place, Suite 1750 Dallas, Texas 75201

Fax No.: (214) 756-7401

Attn: Corporate Trustee, Municipal and Escrow Services

The Issuer, any Guarantor or the Trustee, by notice to the others, may designate additional or different addresses for subsequent notices or communications.

All notices and communications (other than those sent to Holders) shall be deemed to have been duly given: at the time delivered by hand, if personally delivered; five calendar days after being deposited in the mail, postage prepaid, if mailed by first- class mail; when receipt acknowledged, if faxed; and the next Business Day after timely delivery to the courier, if sent by overnight air courier guaranteeing next day delivery; <u>provided</u> that any notice or communication delivered to the Trustee shall be deemed effective upon actual receipt thereof.

Any notice or communication to a Holder of Definitive Notes shall be mailed by first-class mail, certified or registered, return receipt requested, or by overnight air courier guaranteeing next day delivery to its address shown on the Note Register kept by the Registrar. Any notice or communication to a Holder of Global Notes shall be sent by the Applicable Procedures. Failure to send a notice or communication to a Holder or any defect in it shall not affect its sufficiency with respect to other Holders.

If a notice or communication is sent in the manner provided above within the time prescribed, it is duly given, whether or not the addressee receives it.

If the Issuer sends a notice or communication to Holders, it shall mail a copy to the Trustee and each Agent at the same time.

SECTION 13.02. <u>Communication by Holders of Notes with Other Holders of Notes.</u> Holders may communicate with other Holders with respect to their rights under this Indenture or the Notes.

SECTION 13.03. <u>Certificate and Opinion as to Conditions Precedent.</u> Upon any request or application by the Issuer or any of the Guarantors to the Trustee to take any action under this Indenture, the Issuer or such Guarantor, as the case may be, shall furnish to the Trustee:

- (A) An Officer's Certificate of the Issuer in form and substance reasonably satisfactory to the Trustee (which shall include the statements set forth in Section 13.04 hereof) stating that, in the opinion of the signers, all conditions precedent and covenants, if any, provided for in this Indenture relating to the proposed action have been satisfied; and
- (B) An Opinion of Counsel in form and substance reasonably satisfactory to the Trustee (which shall include the statements set forth in Section 13.04 hereof) stating that, in the opinion of such counsel, all such conditions precedent and covenants have been satisfied.

SECTION 13.04. <u>Statements Required in Certificate or Opinion</u>. Each certificate or opinion with respect to compliance with a condition or covenant provided for in this Indenture shall include:

- (A) a statement that the Person making such certificate or opinion has read such covenant or condition;
- (B) a brief statement as to the nature and scope of the examination or investigation upon which the statements or opinions contained in such certificate or opinion are based;
- (C) a statement that, in the opinion of such Person, he or she has made such examination or investigation as is necessary to enable him to express an informed opinion as to whether or not such covenant or condition has been complied with (and, in the case of an Opinion of Counsel, may be limited to reliance on an Officer's Certificate as to matters of fact); and
 - (D) a statement as to whether or not, in the opinion of such Person, such condition or covenant has been complied with.

SECTION 13.05. <u>Rules by Trustee and Agents.</u> The Trustee may make reasonable rules for action by or at a meeting of Holders. The Registrar, Paying Agent or Calculation Agent may make reasonable rules and set reasonable requirements for its functions.

SECTION 13.06. No Personal Liability of Directors, Officers, Employees and Stockholders. No director, officer, employee, incorporator or stockholder of Holdings III, the Issuer or any other Guarantor (other than in the case of stockholders of the Issuer, any Parent Guarantor or any Subsidiary Guarantor, any Parent Guarantor, the Issuer or another Subsidiary Guarantor) or any of their parent companies shall have any liability for any obligations of the Issuer or the Guarantors under the Notes, the Guarantees or this Indenture or for any claim based on, in respect of, or by reason of such obligations or their creation. Each Holder by accepting Notes waives and releases all such liability. The waiver and release are part of the consideration for issuance of the Notes.

SECTION 13.07. <u>Governing Law.</u> THIS INDENTURE, THE NOTES, ANY GUARANTEE AND THE COLLATERAL DOCUMENTS RELATING TO THE NOTES WILL BE GOVERNED BY AND CONSTRUED IN ACCORDANCE WITH THE LAWS OF THE STATE OF NEW YORK.

SECTION 13.08. <u>Waiver of Jury Trial.</u> EACH OF THE ISSUER, THE GUARANTORS AND THE TRUSTEE HEREBY IRREVOCABLY WAIVES, TO THE FULLEST EXTENT PERMITTED BY APPLICABLE LAW, ANY AND ALL RIGHT TO TRIAL BY JURY IN ANY LEGAL PROCEEDING ARISING OUT OF OR RELATING TO THIS INDENTURE, THE NOTES OR THE TRANSACTIONS CONTEMPLATED HEREBY.

SECTION 13.09. <u>Force Majeure.</u> In no event shall the Trustee be responsible or liable for any failure or delay in the performance of its obligations under this Indenture arising out of or caused by, directly or indirectly, forces beyond its reasonable control, including without limitation strikes, work stoppages, accidents, acts of war or terrorism, civil or military disturbances, nuclear or natural catastrophes or acts of God, interruptions, loss or malfunctions of utilities, communications or computer (software or hardware) services or the availability of the Federal Reserve Bank.

SECTION 13.10. No Adverse Interpretation of Other Agreements. This Indenture may not be used to interpret any other indenture, loan or debt agreement of the Issuer or its Restricted Subsidiaries or of any other Person. Any such indenture, loan or debt agreement may not be used to interpret this Indenture.

- SECTION 13.11. <u>Successors.</u> All agreements of the Issuer in this Indenture and the Notes shall bind its successors. All agreements of the Trustee in this Indenture shall bind its successors, except as otherwise provided in Section 10.05 hereof.
- SECTION 13.12. <u>Severability.</u> In case any provision in this Indenture or in the Notes shall be invalid, illegal or unenforceable, the validity, legality and enforceability of the remaining provisions shall not in any way be affected or impaired thereby.
- SECTION 13.13. <u>Counterpart Originals.</u> The parties may sign any number of copies of this Indenture. Each signed copy shall be an original, but all of them together represent the same agreement.
- SECTION 13.14. <u>Table of Contents, Headings, etc.</u> The Table of Contents, Cross-Reference Table and headings of the Articles and Sections of this Indenture have been inserted for convenience of reference only, are not to be considered a part of this Indenture and shall in no way modify or restrict any of the terms or provisions hereof.

SECTION 13.15. Currency of Account; Conversion of Currency; Foreign Exchange Restrictions.

(a) U.S. dollars are the sole currency of account and payment for all sums payable by the Issuer and the Guarantors under or in connection with the Notes, the Guarantees of the Notes or this Indenture, including damages related thereto or hereto. Any amount received or recovered in a currency other than U.S. dollars by a Holder of Notes (whether as a result of, or of the enforcement of, a judgment or order of a court of any jurisdiction, in the winding-up or dissolution of the Issuer or otherwise) in respect of any sum expressed to be due to it from the Issuer shall only constitute a discharge to the

Issuer to the extent of the U.S. dollar amount, which the recipient is able to purchase with the amount so received or recovered in that other currency on the date of that receipt or recovery (or, if it is not practicable to make that purchase on that date, on the first date on which it is practicable to do so). If that U.S. dollar amount is less than the U.S. dollar amount expressed to be due to the recipient under the applicable Notes, the Issuer shall indemnify it against any loss sustained by it as a result as set forth in Section 13.15(b). In any event, the Issuer and the Guarantors shall indemnify the recipient against the cost of making any such purchase. For the purposes of this Section 13.15, it will be sufficient for the Holder of a Note to certify in a satisfactory manner (indicating sources of information used) that it would have suffered a loss had an actual purchase of U.S. dollars been made with the amount so received in that other currency on the date of receipt or recovery (or, if a purchase of U.S. dollars on such date had not been practicable, on the first date on which it would have been practicable, it being required that the need for a change of date be certified in the manner mentioned above).

- (b) The Issuer and the Guarantors, jointly and severally, covenant and agree that the following provisions shall apply to conversion of currency in the case of the Notes, the Guarantees and this Indenture:
 - (1) (A) If for the purpose of obtaining judgment in, or enforcing the judgment of, any court in any country, it becomes necessary to convert into a currency (the "<u>Judgment Currency</u>") an amount due in any other currency (the "<u>Base Currency</u>"), then the conversion shall be made at the rate of exchange prevailing on the Business Day before the day on which the judgment is given or the order of enforcement is made, as the case may be (unless a court shall otherwise determine).
 - (B) If there is a change in the rate of exchange prevailing between the Business Day before the day on which the judgment is given or an order of enforcement is made, as the case may be (or such other date as a court shall determine), and the date of receipt of the amount due, the Issuer and the Guarantors will pay such additional (or, as the case may be, such lesser) amount, if any, as may be necessary so that the amount paid in the Judgment Currency when converted at the rate of exchange prevailing on the date of receipt will produce the amount in the Base Currency originally due.
 - (2) In the event of the winding-up of the Issuer or any Guarantor at any time while any amount or damages owing under the Notes, the Guarantees and this Indenture, or any judgment or order rendered in respect thereof, shall remain outstanding, the Issuer and the Guarantors shall indemnify and hold the Holders and the Trustee harmless against any deficiency arising or resulting from any variation in rates of exchange between (i) the date as of which the Applicable Currency Equivalent of the amount due or contingently due under the Notes, the Guarantees and this Indenture (other than under this subsection (b)(2)) is calculated for the purposes of such winding-up and (ii) the final date for the filing

of proofs of claim in such winding-up. For the purpose of this subsection (b)(2), the final date for the filing of proofs of claim in the winding-up of the Issuer or any Guarantor shall be the date fixed by the liquidator or otherwise in accordance with the relevant provisions of applicable law as being the latest practicable date as at which liabilities of the Issuer or such Guarantor may be ascertained for such winding-up prior to payment by the liquidator or otherwise in respect thereto.

- (c) The obligations contained in this Section 13.15 shall constitute separate and independent obligations from the other obligations of the Issuer and the Guarantors under this Indenture, shall give rise to separate and independent causes of action against the Issuer and the Guarantors, shall apply irrespective of any waiver or extension granted by any Holder or the Trustee or either of them from time to time and shall continue in full force and effect notwithstanding any judgment or order or the filing of any proof of claim in the winding-up of the Issuer or any Guarantor for a liquidated sum in respect of amounts due hereunder (other than under subsection (b)(2) above) or under any such judgment or order. Any such deficiency as aforesaid shall be deemed to constitute a loss suffered by the Holders or the Trustee, as the case may be, and no proof or evidence of any actual loss shall be required by the Issuer or any Guarantor or the liquidator or otherwise or any of them. In the case of subsection (b)(2) above, the amount of such deficiency shall not be deemed to be reduced by any variation in rates of exchange occurring between the said final date and the date of any liquidating distribution.
- (d) The term "rate(s) of exchange" shall mean the rate of exchange quoted by Reuters at 10:00 a.m. (New York time) for spot purchases of the Base Currency with the Judgment Currency other than the Base Currency referred to in subsections (b)(1) and (b)(2) above and includes any premiums and costs of exchange payable.

SECTION 13.16. Consent to Jurisdiction and Service.

Each of Parent, Holdings II, Holdings III and Holdings IV and any Subsidiary Guarantor that is a Foreign Subsidiary shall appoint Corporation Service Company as its agent for actions relating to the Notes, this Indenture or the Collateral Documents relating to the Notes or brought under U.S. Federal or state securities laws brought in any U.S. Federal or state court located in the Borough of Manhattan in The City of New York.

Each of Issuer, Parent, Holdings II, Holdings III and Holdings IV and any Subsidiary Guarantor that is a Foreign Subsidiary and the Trustee irrevocably submit to the personal jurisdiction of any New York state or United States federal court located in the Borough of Manhattan in the City of New York in any action arising out of or relating to this Indenture, the Notes or any of the other Collateral Documents relating to the Notes to which each is or is to be a party, or for recognition or enforcement of any judgment, and Issuer, Parent, Holdings II, Holdings III and Holdings IV and any Subsidiary Guarantor that is a Foreign Subsidiary and the Trustee hereby irrevocably and

unconditionally agree that all claims in respect of such action or proceeding may be heard and determined in any such court of the State of New York or, to the extent permitted by law, in such Federal court. Issuer, Parent, Holdings II, Holdings III and Holdings IV and any Subsidiary Guarantor that is a Foreign Subsidiary and the Trustee irrevocably waive, to the fullest extent permitted by law, any objection which it may now or hereafter have to the laying of venue of any suit, action or proceeding arising out of or relating to this Indenture in such courts. Nothing in this Indenture, the Notes or any other Collateral Document shall affect any right that any party may otherwise have to bring any action or proceeding relating to this Indenture, the Notes or any other Collateral Document in the courts of any jurisdiction.

SECTION 13.17. Electronic Transmission. In respect of this Indenture, the Trustee shall not have any duty or obligation to verify or confirm that the Person sending instructions, directions, reports, notices or other communications or information by electronic transmission (including by e-mail, pdf, facsimile transmission or other similar secured or unsecured electronic methods) is, in fact, a Person authorized to give such instructions, directions, reports, notices or other communications or information on behalf of the party purporting to send such electronic transmission; and the Trustee shall not have any liability for any losses, liabilities, costs or expenses incurred or sustained by any party as a result of such reliance upon or compliance with such instructions, directions, reports, notices or other communications. Each other party agrees to assume all risks arising out of the use of such electronic methods to submit instructions, directions, reports, notices or other communications or information to the Trustee, including without limitation the risk of the Trustee acting on unauthorized instructions, notices, reports or other communications or information, and the risk of interception and misuse by third parties.

SECTION 13.18. <u>Patriot Act</u>. In order to comply with laws, rules, regulations and executive orders in effect from time to time applicable to banking institutions, including those relating to the funding of terrorist activities and money laundering ("<u>Specified Law</u>"), Wells Fargo Bank, National Association is required to obtain, verify and record certain information relating to individuals and entities which maintain a business relationship with Wells Fargo Bank, National Association. Accordingly, the Issuer agrees to provide to Wells Fargo Bank, National Association upon its request from time to time such identifying information and documentation as may be available to the Issuer in order to enable Wells Fargo Bank, National Association to comply with Specified Law.

[Signatures on following page]

FREESCALE SEMICONDUCTOR, INC.,

by

/s/ Steven P. Goel

Name: Steven P. Goel

Title: Vice President and Treasurer

FREESCALE SEMICONDUCTOR HOLDINGS V, INC.

by

/s/ Steven P. Goel

Name: Steven P. Goel Title: Treasurer

FREESCALE SEMICONDUCTOR, LTD.

by

/s/ Steven P. Goel

Name: Steven P. Goel Title: Treasurer

FREESCALE SEMICONDUCTOR HOLDINGS II, LTD.

by

/s/ Steven P. Goel

Name: Steven P. Goel Title: Treasurer

FREESCALE SEMICONDUCTOR HOLDINGS III, LTD.

by

/s/ Steven P. Goel

Name: Steven P. Goel Title: Treasurer

Signature Page to Indenture

FREESCALE SEMICONDUCTOR HOLDINGS IV, LTD.

by

/s/ Steven P. Goel

Name: Steven P. Goel Title: Treasurer

SIGMATEL, LLC

by Freescale Semiconductor, Inc., as Sole Member

/s/ Steven P. Goel

Name: Steven P. Goel Title: Treasurer

WELLS FARGO BANK, NATIONAL ASSOCIATION, AS TRUSTEE

by

/s/ Patrick T. Giordano

Name: Patrick T. Giordano Title: Vice President

Signature Page to Indenture

[Face of Note]

[Insert the Global Note Legend, if applicable pursuant to the provisions of the Indenture]

[Insert the Private Placement Legend, if applicable pursuant to the provisions of the Indenture]

[Insert the Regulation S Temporary Global Note Legend, if applicable pursuant to the provisions of the Indenture]

A-1

| CUSIP [ISIN [|]]1 |
|-------------------|---------|
| 13111 [| 1. |

[RULE 144A][REGULATION S] GLOBAL NOTE 6.000% Senior Secured Note due 2022

No. [\$

FREESCALE SEMICONDUCTOR, INC.

promises to pay to or registered assigns, the principal sum [set forth on the Schedule of Exchanges of Interests in the Global Note attached hereto] [of United States Dollars] on January 15, 2022.

Interest Payment Dates: May 15 and November 15, commencing May 15, 2014

Record Dates: May 1 and November 1

144A CUSIP: 35687M AZ0
 144A ISIN: US35687MAZ05
 Regulation S CUSIP: U31395 AN3
 Regulation S ISIN: USU31395AN38

| Dated: [|] | | |
|----------|---|-----|-------------------------------|
| | | | FREESCALE SEMICONDUCTOR, INC. |
| | | | Ву: |
| | | | Name: |
| | | | Title: |
| | | A-3 | |

IN WITNESS HEREOF, the Issuer has caused this instrument to be duly executed.

| This is one of the Notes referred to in the within-mentioned Indenture: | |
|---|---|
| | WELLS FARGO BANK, NATIONAL ASSOCIATION, |

| By:_ | | |
|------|----------------------|--|
| | Authorized Signatory | |

as Trustee

[Back of Note]

6.000% Senior Secured Note due 2022

Capitalized terms used herein shall have the meanings assigned to them in the Indenture referred to below unless otherwise indicated.

- 1. INTEREST. Freescale Semiconductor, Inc., a Delaware corporation (the "Issuer"), promises to pay interest on the principal amount of this Note at a rate per annum of 6.000% from November 1, 2013 until maturity. The Issuer will pay interest on this Note semi-annually in arrears on May 15 and November 15 of each year commencing on May 15, 2014, or if any such day is not a Business Day, on the next succeeding Business Day (each, an "Interest Payment Date"). The Issuer will make each interest payment to the Holder of record of this Note on the immediately preceding May 1 and November 1 (each, a "Record Date"). Interest on this Note will accrue from the most recent date to which interest has been paid or, if no interest has been paid, from and including November 1, 2013. The Issuer will pay interest (including post-petition interest in any proceeding under any Bankruptcy Law) on overdue principal and premium, if any, from time to time on demand at the rate borne by this Note; it shall pay interest (including post-petition interest in any proceeding under any Bankruptcy Law) on overdue installments of interest (without regard to any applicable grace periods) from time to time on demand at the rate borne by this Note. Interest will be computed on the basis of a 360-day year comprised of twelve 30-day months.
- 2. METHOD OF PAYMENT. The Issuer will pay interest on this Note to the Person who is the registered Holder of this Note at the close of business on May 1 or November 1 (whether or not a Business Day), as the case may be, next preceding the Interest Payment Date, even if this Note is canceled after such record date and on or before such Interest Payment Date, except as provided in Section 2.12 of the Indenture with respect to defaulted interest. Cash payment of interest may be made by check mailed to the Holders at their addresses set forth in the Note Register of Holders, provided that (a) all cash payments of principal, premium, if any, and interest on, Notes represented by Global Notes registered in the name of or held by DTC or its nominee will be made by wire transfer of immediately available funds to the accounts specified by the Holder or Holders thereof and (b) all cash payments of principal, premium, if any, and interest with respect to certificated Notes will be made by wire transfer to a U.S. dollar account maintained by the payee with a bank in the United States if such Holder elects payment by wire transfer by giving written notice to the Trustee or the Paying Agent to such effect designating such account no later than 30 days immediately preceding the relevant due date for payment (or such other date as the Trustee may accept in its discretion). Such payment shall be in such coin or currency of the United States of America as at the time of payment is legal tender for payment of public and private debts.
- 3. PAYING AGENT AND REGISTRAR. Initially, Wells Fargo Bank, National Association, the Trustee under the Indenture, will act as Paying Agent and Registrar. The Issuer may change any Paying Agent or Registrar without notice to the Holders. The Issuer or any of its Subsidiaries may act in any such capacity.

4. INDENTURE. The Issuer issued the Notes under an Indenture, dated as of November 1, 2013 (the "<u>Indenture</u>"), among Freescale Semiconductor, Inc., the Guarantors named therein and the Trustee. This Note is one of a duly authorized issue of notes of the Issuer designated as its 6.000% Senior Secured Notes due 2022. The Issuer shall be entitled to issue Additional Notes pursuant to Section 2.01 and 4.09 of the Indenture. The terms of the Notes include those stated in the Indenture. The Notes are subject to all such terms, and Holders are referred to the Indenture for a statement of such terms. To the extent any provision of this Note conflicts with the express provisions of the Indenture, the provisions of the Indenture shall govern and be controlling.

5. OPTIONAL REDEMPTION.

- (a) Except as described below under clauses 5(b), 5(c) and 5(d) hereof, the Notes will not be redeemable at the Issuer's option.
- (b) At any time prior to November 15, 2016, the Issuer may redeem all or a part of the Notes at a redemption price equal to 100% of the principal amount of the Notes redeemed plus the Applicable Premium as of, and accrued and unpaid interest, if any, to the date of redemption (the "Redemption Date"), subject to the rights of Holders of Notes on the relevant Record Date to receive interest due on the relevant Interest Payment Date.
- (c) Until November 15, 2016, the Issuer may, at its option, on one or more occasions redeem up to 35% of the aggregate principal amount of Notes at a redemption price equal to 106.000% of the aggregate principal amount thereof, plus accrued and unpaid interest, if any, to the Redemption Date, subject to the right of Holders of record on the relevant Record Date to receive interest due on the relevant Interest Payment Date, with the net cash proceeds received of one or more Equity Offerings; provided that at least 50% of the sum of the aggregate principal amount of Notes originally issued under the Indenture and any Additional Notes issued under the Indenture after the Issue Date remains outstanding immediately after the occurrence of each such redemption; provided further that each such redemption occurs within 180 days of the date of closing of each such Equity Offering. Notice of any redemption upon any Equity Offering may be given prior to the redemption thereof, and any such redemption or notice may, at the Issuer's discretion, be subject to one or more conditions precedent, including, but not limited to, completion of the related Equity Offering.
- (d) On and after November 15, 2016, the Issuer may redeem the Notes, in whole or in part at the redemption prices (expressed as percentages of principal amount of the Notes to be redeemed) set forth below, plus accrued and unpaid interest, if any, to the Redemption Date, subject to the right of Holders of record on the relevant Record Date to receive interest due on the relevant Interest Payment Date, if redeemed during the twelve-month period beginning on November 15 of each of the years indicated below:

| <u>Year</u> | Percentage |
|---------------------|------------|
| <u>Year</u> 2016 | 104.500% |
| 2017 | 103.000% |
| 2018 | 101.500% |
| 2019 and thereafter | 100.000% |

- (e) Any redemption pursuant to this paragraph 5 shall be made pursuant to the provisions of Sections 3.01 through 3.06 of the Indenture.
- 6. MANDATORY REDEMPTION. The Issuer shall not be required to make mandatory redemption or sinking fund payments with respect to the Notes.
- 7. NOTICE OF REDEMPTION. Subject to Section 3.03 of the Indenture, notice of redemption will be sent at least 30 days but not more than 60 days before the redemption date (except that redemption notices may be sent more than 60 days prior to a redemption date if the notice is issued in connection with Article 8 or Article 12 of the Indenture) to each Holder whose Notes are to be redeemed at its registered address. Notes in denominations larger than \$2,000 may be redeemed in part but only in whole multiples of \$1,000, unless all of the Notes held by a Holder are to be redeemed. On and after the Redemption Date, interest ceases to accrue on this Note or portions thereof called for redemption.
- 8. OFFERS TO REPURCHASE. Upon the occurrence of a Change of Control, the Issuer shall make a Change of Control Offer in accordance with Section 4.14 of the Indenture. In connection with certain Asset Sales, the Issuer shall make an Asset Sale Offer as and when provided in accordance with Section 4.10 of the Indenture.
- 9. DENOMINATIONS, TRANSFER, EXCHANGE. The Notes are in registered form without coupons in denominations of \$2,000 and integral multiples of \$1,000 thereafter. The transfer of Notes may be registered and Notes may be exchanged as provided in the Indenture. The Registrar and the Trustee may require a Holder, among other things, to furnish appropriate endorsements and transfer documents and the Issuer may require a Holder to pay any taxes and fees required by law or permitted by the Indenture. The Issuer need not exchange or register the transfer of any Note or portion of a Note selected for redemption, except for the unredeemed portion of any Note being redeemed in part. Also, the Issuer need not exchange or register the transfer of any Notes for a period of 15 days before a selection of Notes to be redeemed.
 - 10. PERSONS DEEMED OWNERS. The registered Holder of a Note may be treated as its owner for all purposes.
- 11. AMENDMENT, SUPPLEMENT AND WAIVER. The Indenture, the Guarantees or the Notes may be amended or supplemented as provided in the Indenture.
- 12. DEFAULTS AND REMEDIES. The Events of Default relating to the Notes are defined in Section 6.01 of the Indenture. If any Event of Default occurs and is continuing, the Trustee or the Holders of at least 30% in principal amount of the then outstanding Notes may declare the principal, premium, if any, interest and any other monetary obligations on

all the then outstanding Notes to be due and payable immediately. Notwithstanding the foregoing, in the case of an Event of Default arising from certain events of bankruptcy or insolvency, all outstanding Notes will become due and payable immediately without further action or notice. Holders may not enforce the Indenture, the Notes or the Guarantees except as provided in the Indenture. Subject to certain limitations, Holders of a majority in aggregate principal amount of the then outstanding Notes may direct the Trustee in its exercise of any trust or power. The Trustee may withhold from Holders notice of any continuing Default (except a Default relating to the payment of principal, premium, if any, or interest) if it determines that withholding notice is in their interest. The Holders of a majority in aggregate principal amount of the Notes then outstanding by notice to the Trustee may on behalf of the Holders of all of the Notes waive any existing Default or and its consequences under the Indenture except a continuing Default in payment of the principal of, premium, if any, or interest on, any of the Notes held by a non-consenting Holder. Holdings III is required to deliver to the Trustee annually a statement regarding compliance with the Indenture, and Holdings III is required within five (5) Business Days after becoming aware of any Default, to deliver to the Trustee a statement specifying such Default and what action the Issuer proposes to take with respect thereto.

- 13. AUTHENTICATION. This Note shall not be entitled to any benefit under the Indenture or be valid or obligatory for any purpose until authenticated by the manual signature of the Trustee.
- 14. GOVERNING LAW. THE LAWS OF THE STATE OF NEW YORK SHALL GOVERN AND BE USED TO CONSTRUE THE INDENTURE, THE NOTES, THE GUARANTEES AND THE COLLATERAL DOCUMENTS RELATING TO THE NOTES.
- 15. CUSIP AND ISIN NUMBERS. Pursuant to a recommendation promulgated by the Committee on Uniform Security Identification Procedures, the Issuer has caused CUSIP and ISIN numbers to be printed on the Notes and the Trustee may use CUSIP and ISIN numbers in notices of redemption as a convenience to Holders. No representation is made as to the accuracy of such numbers either as printed on the Notes or as contained in any notice of redemption and reliance may be placed only on the other identification numbers placed thereon.

The Issuer will furnish to any Holder upon written request and without charge a copy of the Indenture. Requests may be made to the Issuer at the following address:

Freescale Semiconductor, Inc. 6501 William Cannon Drive West Austin, Texas 78735 Fax: (512) 996-6853 Attention: General Counsel

| ASSIGNMENT FORM | |
|--|--|
| To assign this Note, fill in the form below: | |
| (I) or (we) assign and transfer this Note to: | |
| (Insert assignee' legal name) | |
| (Insert assignee's soc. sec. or tax I.D. no.) | |
| | |
| | |
| | |
| (Print or type assignee's name, address and zip code) | |
| and irrevocably appoint | |
| to transfer this Note on the books of the Issuer. The agent may substitute another to act for him. | |
| Date: | |
| Your Signature: | |
| | (Sign exactly as your name appears on the face of this Note) |
| Signature Guarantee*: | |

* Participant in a recognized Signature Guarantee Medallion Program (or other signature guarantor acceptable to the Trustee).

OPTION OF HOLDER TO ELECT PURCHASE

If you want to elect to have this Note purchased by the Issuer pursuant to Section 4.10 or 4.14 of the Indenture, check the appropriate box below:

| | [] Section 4.10 | [] Section 4.14 | |
|---|------------------------|------------------------------------|--|
| If you want to elect to have only part of this Note purchase to have purchased: | d by the Issuer pursua | ant to Section 4.10 or Section 4.1 | 4 of the Indenture, state the amount you elect |
| | \$ | | |
| Date: | | | |
| | | Your Signature: | |
| | | _ | (Sign exactly as your name appears on the face of this Note) |
| | | Tax Identification | No.: |
| Signature Guarantee*: | | | |

 $^{*\} Participant\ in\ a\ recognized\ Signature\ Guarantee\ Medallion\ Program\ (or\ other\ signature\ guarantor\ acceptable\ to\ the\ Trustee).$

SCHEDULE OF EXCHANGES OF INTERESTS IN THE GLOBAL NOTE*

| 61 1 | . The following exchanges of a part of this Global Note for an interest in r Global or Definitive Note for an interest in this Global Note, have been made: |
|------|---|
| | Principal |

| | | | Amount of | |
|------------------|---------------------|----------------|----------------|--------------|
| | | Amount of | this Global | Signature of |
| | | increase | Note | authorized |
| | | in Principal | following such | officer |
| | Amount of decrease | Amount of this | decrease or | of Trustee o |
| Date of Exchange | in Principal Amount | Global Note | increase | Custodian |
| | | <u></u> | <u></u> | <u>-</u> |

^{*}This schedule should be included only if the Note is issued in global form.

FORM OF CERTIFICATE OF TRANSFER

Freescale Semiconductor, Inc. 6501 William Cannon Drive West Austin, Texas 78735 Fax: 512-996-6853

Attention: General Counsel

Wells Fargo Bank, National Association 750 N. Saint Paul Place, Suite 1750 Dallas, Texas 75201 Fax No.: (214) 756-7401

Attn: Corporate Trustee, Municipal and Escrow Services

Re: 6.000% Senior Secured Notes due 2022

Reference is hereby made to the Indenture, dated as of November 1, 2013 (the "<u>Indenture</u>"), among Freescale Semiconductor, Inc., the Guarantors named therein and the Trustee. Capitalized terms used but not defined herein shall have the meanings given to them in the Indenture.

(the "<u>Transferor</u>") owns and proposes to transfer the Note[s] or interest in such Note[s] specified in Annex A hereto, in the principal amount of \$\frac{1}{2}\$ in such Note[s] or interests (the "<u>Transferor</u>"), to (the "<u>Transferor</u>"), as further specified in Annex A hereto. In connection with the Transfer, the Transferor hereby certifies that:

[CHECK ALL THAT APPLY]

- 1. [] CHECK IF TRANSFEREE WILL TAKE DELIVERY OF A BENEFICIAL INTEREST IN THE RELEVANT 144A GLOBAL NOTE OR RELEVANT DEFINITIVE NOTE PURSUANT TO RULE 144A. The Transfer is being effected pursuant to and in accordance with Rule 144A under the United States Securities Act of 1933, as amended (the "Securities Act"), and, accordingly, the Transferor hereby further certifies that the beneficial interest or Definitive Note is being transferred to a Person that the Transferor reasonably believes is purchasing the beneficial interest or Definitive Note for its own account, or for one or more accounts with respect to which such Person exercises sole investment discretion, and such Person and each such account is a "qualified institutional buyer" within the meaning of Rule 144A in a transaction meeting the requirements of Rule 144A and such Transfer is in compliance with any applicable blue sky securities laws of any state of the United States.
- 2. [$\,\,\,$] CHECK IF TRANSFEREE WILL TAKE DELIVERY OF A BENEFICIAL INTEREST IN THE RELEVANT REGULATION S GLOBAL NOTE OR

RELEVANT DEFINITIVE NOTE PURSUANT TO REGULATION S. The Transfer is being effected pursuant to and in accordance with Rule 903 or Rule 904 under the Securities Act and, accordingly, the Transferor hereby further certifies that (i) the Transfer is not being made to a person in the United States and (x) at the time the buy order was originated, the Transferee was outside the United States or such Transferor and any Person acting on its behalf reasonably believed and believes that the Transferee was outside the United States or (y) the transaction was executed in, on or through the facilities of a designated offshore securities market and neither such Transferor nor any Person acting on its behalf knows that the transaction was prearranged with a buyer in the United States, (ii) no directed selling efforts have been made in contravention of the requirements of Rule 903(b) or Rule 904(b) of Regulation S under the Securities Act, (iii) the transaction is not part of a plan or scheme to evade the registration requirements of the Securities Act and (iv) if the proposed transfer is being made prior to the expiration of the Restricted Period, the transfer is not being made to a U.S. Person or for the account or benefit of a U.S. Person (other than the Initial Purchasers). Upon consummation of the proposed transfer in accordance with the terms of the Indenture, the transferred beneficial interest or Definitive Note will be subject to the restrictions on Transfer enumerated in the Indenture and the Securities Act.

- 3. [] CHECK AND COMPLETE IF TRANSFEREE WILL TAKE DELIVERY OF A BENEFICIAL INTEREST IN THE RELEVANT DEFINITIVE NOTE PURSUANT TO ANY PROVISION OF THE SECURITIES ACT OTHER THAN RULE 144A OR REGULATION S. The Transfer is being effected in compliance with the transfer restrictions applicable to beneficial interests in Restricted Global Notes and Restricted Definitive Notes and pursuant to and in accordance with the Securities Act and any applicable blue sky securities laws of any state of the United States, and accordingly the Transferor hereby further certifies that (check one):
 - (a) [] such Transfer is being effected pursuant to and in accordance with Rule 144 under the Securities Act;

or

(b) [] such Transfer is being effected to the Issuer or a subsidiary thereof;

or

- (c) [] such Transfer is being effected pursuant to an effective registration statement under the Securities Act and in compliance with the prospectus delivery requirements of the Securities Act.
- 4. [] CHECK IF TRANSFEREE WILL TAKE DELIVERY OF A BENEFICIAL INTEREST IN AN UNRESTRICTED GLOBAL NOTE OR OF AN UNRESTRICTED DEFINITIVE NOTE.
- (a) [] CHECK IF TRANSFER IS PURSUANT TO RULE 144. (i) The Transfer is being effected pursuant to and in accordance with Rule 144 under the Securities Act and in compliance with the transfer restrictions contained in the Indenture and any applicable

blue sky securities laws of any state of the United States and (ii) the restrictions on transfer contained in the Indenture and the Private Placement Legend are not required in order to maintain compliance with the Securities Act. Upon consummation of the proposed Transfer in accordance with the terms of the Indenture, the transferred beneficial interest or Definitive Note will no longer be subject to the restrictions on transfer enumerated in the Private Placement Legend printed on the Restricted Global Notes, on Restricted Definitive Notes and in the Indenture.

- (b) [] CHECK IF TRANSFER IS PURSUANT TO REGULATION S. (i) The Transfer is being effected pursuant to and in accordance with Rule 903 or Rule 904 under the Securities Act and in compliance with the transfer restrictions contained in the Indenture and any applicable blue sky securities laws of any state of the United States and (ii) the restrictions on transfer contained in the Indenture and the Private Placement Legend are not required in order to maintain compliance with the Securities Act. Upon consummation of the proposed Transfer in accordance with the terms of the Indenture, the transferred beneficial interest or Definitive Note will no longer be subject to the restrictions on transfer enumerated in the Private Placement Legend printed on the Restricted Global Notes, on Restricted Definitive Notes and in the Indenture.
- (c) [] CHECK IF TRANSFER IS PURSUANT TO OTHER EXEMPTION. (i) The Transfer is being effected pursuant to and in compliance with an exemption from the registration requirements of the Securities Act other than Rule 144, Rule 903 or Rule 904 and in compliance with the transfer restrictions contained in the Indenture and any applicable blue sky securities laws of any State of the United States and (ii) the restrictions on transfer contained in the Indenture and the Private Placement Legend are not required in order to maintain compliance with the Securities Act. Upon consummation of the proposed Transfer in accordance with the terms of the Indenture, the transferred beneficial interest or Definitive Note will not be subject to the restrictions on transfer enumerated in the Private Placement Legend printed on the Restricted Global Notes or Restricted Definitive Notes and in the Indenture.

| | This certificate and the statements contained herein are made for your benefit and the benefit of the Issuer. | | |
|--------|---|--|--|
| | [Insert Name of Transferor] | | |
| | By: | | |
| | Name: | | |
| | Title: | | |
| | | | |
| Dated: | | | |

| 1. | The Transferor owns and proposes to transfer the following: | | |
|-----|---|-----------------------|--|
| | [CHEC | CK ONE OF (a) OR (b)] | |
| (a) | [] a beneficial interest in the: | | |
| | (i) [] 144A Global Note (CUSIP: [•]), or | | |
| | (ii) [] Regulation S Global Note (CUSIP: [•]) | , or | |
| (b) | [] a Restricted Definitive Note. | | |
| 2. | After the Transfer the Transferee will hold: | | |
| | | [CHECK ONE] | |
| (a) | [] a beneficial interest in the: | | |
| | (i) [] 144A Global Note (CUSIP: |), or | |
| | (ii) [] Regulation S Global Note [CUSIP: |), or | |
| | (iii) [] Unrestricted Global Note (|); or | |
| (b) | [] a Restricted Definitive Note; or | | |
| (c) | [] an Unrestricted Definitive Note, | | |

ANNEX-1

FORM OF CERTIFICATE OF EXCHANGE

Freescale Semiconductor, Inc. 6501 William Cannon Drive West Austin, Texas 78735 Fax: 512-996-6853

Attention: General Counsel

Wells Fargo Bank, National Association 750 N. Saint Paul Place, Suite 1750 Dallas, Texas 75201 Fax No.: (214) 756-7401

Attn: Corporate Trustee, Municipal and Escrow Services

Re: 6.000% Senior Secured Notes due 2022

Reference is hereby made to the Indenture, dated as of November 1, 2013 (the "<u>Indenture</u>"), among Freescale Semiconductor, Inc., the Guarantors named therein and the Trustee. Capitalized terms used but not defined herein shall have the meanings given to them in the Indenture.

- (the "Owner") owns and proposes to exchange the Note[s] or interest in such Note[s] specified herein, in the principal amount of in such Note[s] or interests (the "Exchange"). In connection with the Exchange, the Owner hereby certifies that:
- 1) EXCHANGE OF RESTRICTED DEFINITIVE NOTES OR BENEFICIAL INTERESTS IN A RESTRICTED GLOBAL NOTE FOR UNRESTRICTED DEFINITIVE NOTES OR BENEFICIAL INTERESTS IN AN UNRESTRICTED GLOBAL NOTE
 - a) [] CHECK IF EXCHANGE IS FROM BENEFICIAL INTEREST IN A RESTRICTED GLOBAL NOTE TO BENEFICIAL INTEREST IN AN UNRESTRICTED GLOBAL NOTE. In connection with the Exchange of the Owner's beneficial interest in a Restricted Global Note for a beneficial interest in an Unrestricted Global Note in an equal principal amount, the Owner hereby certifies (i) the beneficial interest is being acquired for the Owner's own account without transfer, (ii) such Exchange has been effected in compliance with the transfer restrictions applicable to the Global Notes and pursuant to and in accordance with the United States Securities Act of 1933, as amended (the "Securities Act"), (iii) the restrictions on transfer contained in the Indenture and the Private Placement Legend are not required in order to maintain compliance with the Securities Act and (iv) the beneficial interest in an Unrestricted Global Note is being acquired in compliance with any applicable blue sky securities laws of any state of the United States.

- b) [] CHECK IF EXCHANGE IS FROM BENEFICIAL INTEREST IN A RESTRICTED GLOBAL NOTE TO UNRESTRICTED DEFINITIVE NOTE. In connection with the Exchange of the Owner's beneficial interest in a Restricted Global Note for an Unrestricted Definitive Note, the Owner hereby certifies (i) the Definitive Note is being acquired for the Owner's own account without transfer, (ii) such Exchange has been effected in compliance with the transfer restrictions applicable to the Restricted Global Notes and pursuant to and in accordance with the Securities Act, (iii) the restrictions on transfer contained in the Indenture and the Private Placement Legend are not required in order to maintain compliance with the Securities Act and (iv) the Definitive Note is being acquired in compliance with any applicable blue sky securities laws of any state of the United States.
- c) [] CHECK IF EXCHANGE IS FROM RESTRICTED DEFINITIVE NOTE TO BENEFICIAL INTEREST IN AN UNRESTRICTED GLOBAL NOTE. In connection with the Owner's Exchange of a Restricted Definitive Note for a beneficial interest in an Unrestricted Global Note, the Owner hereby certifies (i) the beneficial interest is being acquired for the Owner's own account without transfer, (ii) such Exchange has been effected in compliance with the transfer restrictions applicable to Restricted Definitive Notes and pursuant to and in accordance with the Securities Act, (iii) the restrictions on transfer contained in the Indenture and the Private Placement Legend are not required in order to maintain compliance with the Securities Act and (iv) the beneficial interest is being acquired in compliance with any applicable blue sky securities laws of any state of the United States.
- d) [] CHECK IF EXCHANGE IS FROM RESTRICTED DEFINITIVE NOTE TO UNRESTRICTED DEFINITIVE NOTE. In connection with the Owner's Exchange of a Restricted Definitive Note for an Unrestricted Definitive Note, the Owner hereby certifies (i) the Unrestricted Definitive Note is being acquired for the Owner's own account without transfer, (ii) such Exchange has been effected in compliance with the transfer restrictions applicable to Restricted Definitive Notes and pursuant to and in accordance with the Securities Act, (iii) the restrictions on transfer contained in the Indenture and the Private Placement Legend are not required in order to maintain compliance with the Securities Act and (iv) the Unrestricted Definitive Note is being acquired in compliance with any applicable blue sky securities laws of any state of the United States.

| | DEFINITIVE NOTE. In connection with the Exchange of the Owner's beneficial interest in a Restricted Global Note for a Restricted Definitive Note with an equal principal amount, the Owner hereby certifies that the Restricted Definitive Note is being acquired for the Owner's own account without transfer. Upon consummation of the proposed Exchange in accordance with the terms of the Indenture, the Restricted Definitive Note issued will continue to be subject to the restrictions on transfer enumerated in the Private Placement Legend printed on the Restricted Definitive Note and in the Indenture and the Securities Act. |
|--------|--|
| | b) [] CHECK IF EXCHANGE IS FROM RESTRICTED DEFINITIVE NOTE TO BENEFICIAL INTEREST IN A RESTRICTED GLOBAL NOTE. In connection with the Exchange of the Owner's Restricted Definitive Note for a beneficial interest in the [CHECK ONE] [] 144A Global Note [] Regulation S Global Note, with an equal principal amount, the Owner hereby certifies (i) the beneficial interest is being acquired for the Owner's own account without transfer and (ii) such Exchange has been effected in compliance with the transfer restrictions applicable to the Restricted Global Notes and pursuant to and in accordance with the Securities Act, and in compliance with any applicable blue sky securities laws of any state of the United States. Upon consummation of the proposed Exchange in accordance with the terms of the Indenture, the beneficial interest issued will be subject to the restrictions on transfer enumerated in the Private Placement Legend printed on the relevant Restricted Global Note and in the Indenture and the Securities Act. |
| This | certificate and the statements contained herein are made for your benefit and the benefit of the Issuer and are dated . |
| | [Insert Name of Transferor] |
| | Ву: |
| | Name: Title: |
| Dated: | |
| | |

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2) EXCHANGE OF RESTRICTED DEFINITIVE NOTES OR BENEFICIAL INTERESTS IN RESTRICTED GLOBAL NOTES FOR

a) [] CHECK IF EXCHANGE IS FROM BENEFICIAL INTEREST IN A RESTRICTED GLOBAL NOTE TO RESTRICTED

RESTRICTED DEFINITIVE NOTES OR BENEFICIAL INTERESTS IN RESTRICTED GLOBAL NOTES

[FORM OF SUPPLEMENTAL INDENTURE TO BE DELIVERED BY SUBSEQUENT GUARANTORS]

Supplemental Indenture (this "<u>Supplemental Indenture</u>"), dated as of , among (the "<u>Guaranteeing Subsidiary</u>"), a subsidiary of Freescale Semiconductor Holdings III, Ltd., a Bermuda exempted limited liability company, Freescale Semiconductor, Inc., a Delaware corporation (the "<u>Issuer</u>"), and Wells Fargo Bank, National Association, as trustee (the "<u>Trustee</u>").

WITNESSETH

WHEREAS, each of Freescale Semiconductor, Inc. and the Guarantors (as defined in the Indenture referred to below) has heretofore executed and delivered to the Trustee an Indenture (the "Indenture"), dated as of November 1, 2013, providing for the issuance of an unlimited aggregate principal amount of 6.000% Senior Secured Notes due 2022 (the "Notes");

WHEREAS, the Indenture provides that under certain circumstances the Guaranteeing Subsidiary shall execute and deliver to the Trustee a supplemental indenture pursuant to which the Guaranteeing Subsidiary shall unconditionally guarantee all of the Issuer's Obligations under the Notes and the Indenture on the terms and conditions set forth herein and under the Indenture (the "Guarantee"); and

WHEREAS, pursuant to Section 9.01 of the Indenture, the Trustee is authorized to execute and deliver this Supplemental Indenture.

NOW THEREFORE, in consideration of the foregoing and for other good and valuable consideration, the receipt of which is hereby acknowledged, the parties mutually covenant and agree for the equal and ratable benefit of the Holders as follows:

- (1) Capitalized Terms. Capitalized terms used herein without definition shall have the meanings assigned to them in the Indenture.
- (2) Agreement to Guarantee. The Guaranteeing Subsidiary hereby agrees as follows:
- (a) Along with all other Guarantors named in the Indenture (including pursuant to any supplemental indentures), to jointly and severally unconditionally guarantee to each Holder of a Note authenticated and delivered by the Trustee and to the Trustee and its successors and assigns, irrespective of the validity and enforceability of the Indenture, the Notes, the Notes Collateral Documents or the obligations of the Issuer hereunder or thereunder, that:
 - (i) the principal of and interest and premium, if any, on the Notes shall be promptly paid in full when due, whether at maturity, by acceleration, redemption or otherwise, and interest on the overdue principal of and interest on

the Notes, if any, if lawful, and all other obligations of the Issuer to the Holders or the Trustee thereunder shall be promptly paid in full or performed, all in accordance with the terms thereof; and

- (ii) in case of any extension of time of payment or renewal of any Notes or any of such other obligations, that same shall be promptly paid in full when due or performed in accordance with the terms of the extension or renewal, whether at stated maturity, by acceleration or otherwise. Failing payment when due of any amount so guaranteed or any performance so guaranteed for whatever reason, the Guarantors and the Guaranteeing Subsidiary shall be jointly and severally obligated to pay the same immediately. This is a guarantee of payment and not a guarantee of collection.
- (b) The obligations hereunder shall be unconditional, irrespective of the validity, regularity or enforceability of the Notes or the Indenture, the absence of any action to enforce the same, any waiver or consent by any Holder of the Notes with respect to any provisions hereof or thereof, the recovery of any judgment against the Issuer or any other Guarantor, any action to enforce the same or any other circumstance which might otherwise constitute a legal or equitable discharge or defense of a guarantor.
- (c) The Guaranteeing Subsidiary hereby waives: diligence, presentment, demand of payment, filing of claims with a court in the event of insolvency or bankruptcy of the Issuer, any right to require a proceeding first against the Issuer, protest, notice and all demands whatsoever.
- (d) This Guarantee shall not be discharged except by complete performance of the obligations contained in the Notes, the Indenture and this Supplemental Indenture. The Guaranteeing Subsidiary accepts all obligations applicable to a Guarantor under the Indenture, including Article X and, if applicable, Article XI of the Indenture (which is deemed incorporated in this Supplemental Indenture and applicable to this Guarantee) and, as applicable, Section 13.16 of the Indenture. The Guaranteeing Subsidiary acknowledges that by executing this Supplemental Indenture, it will become a Subsidiary Guarantor under the Indenture and subject to all the terms and conditions applicable to Subsidiary Guarantors contained therein.
- (e) If any Holder or the Trustee is required by any court or otherwise to return to the Issuer, the Guarantors (including the Guaranteeing Subsidiary), or any custodian, trustee, liquidator or other similar official acting in relation to either the Issuer or the Guarantors, any amount paid either to the Trustee or such Holder, this Guarantee, to the extent theretofore discharged, shall be reinstated in full force and effect.
- (f) The Guaranteeing Subsidiary shall not be entitled to any right of subrogation in relation to the Holders in respect of any obligations guaranteed hereby until payment in full of all obligations guaranteed hereby.
- (g) As between the Guaranteeing Subsidiary, on the one hand, and the Holders and the Trustee, on the other hand, (x) the maturity of the obligations guaranteed hereby

may be accelerated as provided in Article 6 of the Indenture for the purposes of this Guarantee, notwithstanding any stay, injunction or other prohibition preventing such acceleration in respect of the obligations guaranteed hereby, and (y) in the event of any declaration of acceleration of such obligations as provided in Article 6 of the Indenture, such obligations (whether or not due and payable) shall forthwith become due and payable by the Guaranteeing Subsidiary for the purpose of this Guarantee.

- (h) The Guaranteeing Subsidiary shall have the right to seek contribution from any non-paying Guarantor so long as the exercise of such right does not impair the rights of the Holders under this Guarantee.
- (i) Pursuant to Section 10.02 of the Indenture, after giving effect to all other contingent and fixed liabilities that are relevant under any applicable Bankruptcy or fraudulent conveyance laws, and after giving effect to any collections from, rights to receive contribution from or payments made by or on behalf of any other Guarantor in respect of the obligations of such other Guarantor under Article 10 of the Indenture, this new Guarantee shall be limited to the maximum amount permissible such that the obligations of such Guaranteeing Subsidiary under this Guarantee will not constitute a fraudulent transfer or conveyance.
- (j) This Guarantee shall remain in full force and effect and continue to be effective should any petition be filed by or against the Issuer for liquidation, reorganization, should the Issuer become insolvent or make an assignment for the benefit of creditors or should a receiver or trustee be appointed for all or any significant part of the Issuer's assets, and shall, to the fullest extent permitted by law, continue to be effective or be reinstated, as the case may be, if at any time payment and performance of the Notes are, pursuant to applicable law, rescinded or reduced in amount, or must otherwise be restored or returned by any obligee on the Notes and Guarantee, whether as a "voidable preference", "fraudulent transfer" or otherwise, all as though such payment or performance had not been made. In the event that any payment or any part thereof, is rescinded, reduced, restored or returned, the Note shall, to the fullest extent permitted by law, be reinstated and deemed reduced only by such amount paid and not so rescinded, reduced, restored or returned.
- (k) In case any provision of this Guarantee shall be invalid, illegal or unenforceable, the validity, legality, and enforceability of the remaining provisions shall not in any way be affected or impaired thereby.
- (l) [This Guarantee shall be a secured senior obligation of such Guaranteeing Subsidiary, ranking <u>pari passu</u> in right of payment with any other future First Lien Obligations and Senior Indebtedness of the Guaranteeing Subsidiary, if any.] [This Guarantee shall be an usecured senior obligation of such Guaranteeing Subsidiary, ranking <u>pari passu</u> in right of payment with any other future Senior Indebtedness of the Guaranteeing Subsidiary, if any.]
- (m) Each payment to be made by the Guaranteeing Subsidiary in respect of this Guarantee shall be made without set-off, counterclaim, reduction or diminution of any kind or nature.

- (3) <u>Execution and Delivery</u>. The Guaranteeing Subsidiary agrees that the Guarantee shall remain in full force and effect notwithstanding the absence of the endorsement of any notation of such Guarantee on the Notes.
 - (4) Merger, Consolidation, Amalgamation or Sale of All or Substantially All Assets.
- (a) Except as otherwise provided in Section 5.01(c) of the Indenture, the Guaranteeing Subsidiary may not consolidate, amalgamate or merge with or into or wind up into (whether or not the Issuer or Guaranteeing Subsidiary is the surviving corporation), or sell, assign, transfer, lease, convey or otherwise dispose of all or substantially all of its properties or assets, in one or more related transactions, to any Person unless:
- (i) (A) the Guaranteeing Subsidiary is the surviving corporation or the Person formed by or surviving any such consolidation, amalgamation or merger (if other than the Guaranteeing Subsidiary) or to which such sale, assignment, transfer, lease, conveyance or other disposition will have been made is a corporation organized or existing under the laws of the jurisdiction of organization of the Guaranteeing Subsidiary, as the case may be, or the laws of the United States, any state thereof, the District of Columbia, or any territory thereof (the Guaranteeing Subsidiary or such Person, as the case may be, being herein called the "Successor Person");
- (B) the Successor Person, if other than the Guaranteeing Subsidiary, expressly assumes all the obligations of the Guaranteeing Subsidiary under the Indenture and the Guaranteeing Subsidiary's related Guarantee pursuant to supplemental indentures or other documents or instruments in form reasonably satisfactory to the Trustee and, if applicable, the performance of the covenants and obligations of such Guaranteeing Subsidiary under the Collateral Documents relating to the Notes and shall cause such amendments, supplements, or other instruments to be executed, filed and recorded in such jurisdictions as may be required by applicable law to preserve and protect the Lien on the Collateral owned by or transferred to the Successor Person, together with such financing statements or comparable documents as may be required to perfect any security interests in such Collateral which may be perfected by the filing of a financing statement or a similar document under the UCC or other similar statute or regulation of the relevant states or jurisdictions;
 - (C) immediately after such transaction, no Default exists; and
- (D) the Issuer shall have delivered to the Trustee an Officer's Certificate and an Opinion of Counsel, each stating that such consolidation, merger or transfer and such supplemental indentures, if any, comply with the Indenture; or
 - (ii) the transaction is made in compliance with Section 4.10 of the Indenture;
- (b) Subject to certain limitations described in the Indenture, the Successor Person will succeed to, and be substituted for, the Guaranteeing Subsidiary under the Indenture and the Guaranteeing Subsidiary's Guarantee. Notwithstanding the foregoing, the Guaranteeing Subsidiary may merge into or transfer all or part of its properties and assets to another Guarantor or the Issuer.

(5) Releases.

The Guarantee of the Guaranteeing Subsidiary shall be automatically and unconditionally released and discharged, and no further action by the Guaranteeing Subsidiary, the Issuer or the Trustee is required for the release of the Guaranteeing Subsidiary's Guarantee, upon:

- (1) (A) any sale, exchange or transfer (by merger or otherwise) of the Capital Stock of the Guaranteeing Subsidiary (including any sale, exchange or transfer), after which the Guaranteeing Subsidiary is no longer a Restricted Subsidiary or all or substantially all the assets of the Guaranteeing Subsidiary which sale, exchange or transfer is made in compliance with the applicable provisions of the Indenture;
- (B) the release or discharge of the guarantee by the Guaranteeing Subsidiary under all other First Lien Obligations (including the Senior Credit Facilities and the Existing Secured Notes) or the guarantee which resulted in the creation of the Guarantee, except a discharge or release by or as a result of payment under such guarantee;
 - (C) the proper designation of the Guaranteeing Subsidiary as an Unrestricted Subsidiary;
 - (D) the release of an Unrestricted Parent Guarantor of all Senior Credit Agreement Obligations; or
- (E) the Issuer exercising its Legal Defeasance option or Covenant Defeasance option in accordance with Article 8 of the Indenture or the Issuer's obligations under the Indenture being discharged in accordance with the terms of the Indenture; and
 - (a) (2) the Guaranteeing Subsidiary delivering to the Trustee an Officer's Certificate and an Opinion of Counsel, each stating that all conditions precedent provided for in the Indenture relating to such transaction have been complied with.
- (6) No Recourse Against Others. No director, officer, employee, incorporator or stockholder of the Guaranteeing Subsidiary shall have any liability for any obligations of the Issuer or the Guarantors (including the Guaranteeing Subsidiary) under the Notes, any Guarantees, the Indenture or this Supplemental Indenture or for any claim based on, in respect of, or by reason of, such obligations or their creation. Each Holder by accepting Notes waives and releases all such liability. The waiver and release are part of the consideration for issuance of the Notes.

- (8) <u>Counterparts</u>. The parties may sign any number of copies of this Supplemental Indenture. Each signed copy shall be an original, but all of them together represent the same agreement.
 - (9) Effect of Headings. The Section headings herein are for convenience only and shall not affect the construction hereof.
- (10) <u>The Trustee</u>. The Trustee shall not be responsible in any manner whatsoever for or in respect of the validity or sufficiency of this Supplemental Indenture or for or in respect of the recitals contained herein, all of which recitals are made solely by the Guaranteeing Subsidiary.
- (11) <u>Subrogation</u>. The Guaranteeing Subsidiary shall be subrogated to all rights of Holders of Notes against the Issuer in respect of any amounts paid by the Guaranteeing Subsidiary pursuant to the provisions of Section 2 hereof and Section 10.01 of the Indenture; <u>provided</u> that, if an Event of Default has occurred and is continuing, the Guaranteeing Subsidiary shall not be entitled to enforce or receive any payments arising out of, or based upon, such right of subrogation until all amounts then due and payable by the Issuer under the Indenture or the Notes shall have been paid in full.
- (12) <u>Benefits Acknowledged</u>. The Guaranteeing Subsidiary's Guarantee is subject to the terms and conditions set forth in the Indenture. The Guaranteeing Subsidiary acknowledges that it will receive direct and indirect benefits from the financing arrangements contemplated by the Indenture and this Supplemental Indenture and that the guarantee and waivers made by it pursuant to this Guarantee are knowingly made in contemplation of such benefits.
- (13) <u>Successors</u>. All agreements of the Guaranteeing Subsidiary in this Supplemental Indenture shall bind its Successors, except as otherwise provided in Section 2(k) hereof or elsewhere in this Supplemental Indenture. All agreements of the Trustee in this Supplemental Indenture shall bind its successors.

IN WITNESS WHEREOF, the parties hereto have caused this Supplemental Indenture to be duly executed, all as of the date first above written.

| [GUARANTEEING SUBSIDIARY] |
|--|
| By: Name: Title: |
| FREESCALE SEMICONDUCTOR, INC. |
| By: Name: Title: |
| WELLS FARGO BANK, NATIONAL ASSOCIATION, as Trustee |
| By: Name: Title: |

SECURITY AGREEMENT

dated as of

November 1, 2013

among

FREESCALE SEMICONDUCTOR, INC., as Issuer

FREESCALE SEMICONDUCTOR HOLDINGS V, INC,

FREESCALE SEMICONDUCTOR HOLDINGS IV, LTD.,

SIGMATEL, LLC

and

CITIBANK, N.A., as Notes Collateral Agent

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NOTWITHSTANDING ANYTHING HEREIN TO THE CONTRARY, THE EXERCISE OF ANY RIGHT OR REMEDY BY THE NOTES COLLATERAL AGENT WITH RESPECT TO THE LIENS, SECURITY INTERESTS AND RIGHTS GRANTED PURSUANT TO THIS AGREEMENT OR ANY OTHER COLLATERAL DOCUMENT RELATING TO THE NOTES SHALL BE AS SET FORTH IN, AND SUBJECT TO THE TERMS AND CONDITIONS OF (AND THE EXERCISE OF ANY RIGHT OR REMEDY BY THE NOTES COLLATERAL AGENT HEREUNDER OR THEREUNDER SHALL BE SUBJECT TO THE TERMS AND CONDITIONS OF), THE FIRST LIEN INTERCREDITOR AGREEMENT, DATED AS OF FEBRUARY 19, 2010 (AS AMENDED, AMENDED AND RESTATED, SUPPLEMENTED OR OTHERWISE MODIFIED FROM TIME TO TIME, THE "INTERCREDITOR AGREEMENT"), AMONG CITIBANK, N.A., AS DIRECTING AGENT; CITIBANK, N.A., AS THE SENIOR CREDIT AGREEMENT COLLATERAL AGENT; CITIBANK, N.A., AS THE SENIOR CREDIT AGREEMENT INCREMENTAL COLLATERAL AGENT; CITIBANK, N.A., AS THE INITIAL ADDITIONAL FIRST LIEN REPRESENTATIVE; AND EACH ADDITIONAL AUTHORIZED REPRESENTATIVE FROM TIME TO TIME PARTY THERETO (IN EACH CASE, AS DEFINED IN THE INTERCREDITOR AGREEMENT), AS CONSENTED TO BY THE GRANTORS HEREUNDER FROM TIME TO TIME. WITH THE EXCEPTION OF SECTIONS 2.01 AND 3.01 HEREOF, IN THE EVENT OF ANY CONFLICT BETWEEN THIS AGREEMENT, OR ANY OTHER COLLATERAL DOCUMENT RELATING TO THE NOTES AND THE INTERCREDITOR AGREEMENT, THE INTERCREDITOR AGREEMENT SHALL CONTROL.

SECURITY AGREEMENT, dated as of November 1, 2013, among FREESCALE SEMICONDUCTOR, INC., a Delaware corporation (the "Issuer"), FREESCALE SEMICONDUCTOR HOLDINGS V, INC., a Delaware corporation ("Holdings V"), FREESCALE SEMICONDUCTOR HOLDINGS IV, LTD., a Bermuda exempted limited liability company ("Holdings IV"), SIGMATEL, LLC, a Delaware limited liability company ("SigmaTel"), the Subsidiaries of FREESCALE SEMICONDUCTOR HOLDINGS III, LTD. ("Holdings III") from time to time party hereto and CITIBANK, N.A., as collateral agent for the Secured Parties (as defined below) (in such capacity, the "Notes Collateral Agent").

Reference is made to the Indenture dated as of November 1, 2013 (as amended, supplemented or otherwise modified from time to time, the "Indenture"), among the Issuer, Holdings V, Holdings IV, Holdings III, Freescale Semiconductor Holdings II, Ltd., Freescale Semiconductor, Ltd., SigmaTel and Wells Fargo Bank, National Association, as trustee (the "Trustee"), pursuant to which the Issuer has issued \$960,000,000 aggregate principal amount of 6.000% Senior Secured Notes due 2022 (the "Notes") to the holders thereof (the "Holders"). The obligations of the initial Holders to

purchase the Notes are conditioned upon, among other things, the execution and delivery of this Agreement. Each of the Issuer, Holdings IV and SigmaTel will derive substantial benefits from the execution, delivery and performance of the obligations under the Indenture and the Collateral Documents relating to the Notes and each is, therefore, willing to enter into this Agreement. Accordingly, the parties hereto agree as follows:

ARTICLE I

Definitions

SECTION 1.01. <u>Indenture</u>. (a) Capitalized terms used in this Agreement and not otherwise defined herein have the meanings specified in the Indenture. All terms defined in the New York UCC (as defined herein) and not defined in this Agreement have the meanings specified therein; the term "instrument" shall have the meaning specified in Article 9 of the New York UCC.

- (b) The rules of construction specified in Section 1.03 of the Indenture also apply to this Agreement.
 - SECTION 1.02. Other Defined Terms. As used in this Agreement, the following terms have the meanings specified below:
- "Account Debtor" means any Person who is or who may become obligated to any Grantor under, with respect to or on account of an Account.
- "Accounts" has the meaning specified in Article 9 of the New York UCC.
- "Administrative Agent" has the meaning assigned to such term in the Senior Credit Agreement.
- "Agreement" means this Security Agreement.
- "Article 9 Collateral" has the meaning assigned to such term in Section 3.01(a).
- "Claiming Party" has the meaning assigned to such term in Section 5.02.
- "Collateral" means the Article 9 Collateral and the Pledged Collateral.
- "Collateral Documents" means collectively, the Senior Credit Agreement Collateral Documents, the Additional First Lien Debt Collateral Documents and the Intercreditor Agreement.
 - "Contributing Party" has the meaning assigned to such term in Section 5.02.

"Equity Interest" means, with respect to any Person, all of the shares, interests, rights, participations or other equivalents (however designated) of capital stock of (or other ownership or profit interests or units in) such Person and all of the warrants, options or other rights for the purchase, acquisition or exchange from such Person of any of the foregoing (including through convertible securities).

"Foreign Acquisition Co." means a direct Subsidiary of Holdings III or Holdings IV formed after the Issue Date as a holding company for the Transferred Foreign Subsidiaries and other Foreign Subsidiaries of Holdings III that are not Subsidiaries of Holdings V and (i) that provides a Guarantee and (ii) all of whose stock shall be pledged by Holdings III or Holdings IV, as applicable, to secure the Obligations under the Indenture and the Notes, which Foreign Acquisition Co. shall be organized under the laws of Hungary, Luxembourg, The Netherlands, Iceland, Bermuda, Barbados, Mauritius, the British Virgin Islands, Malta, Cyprus or such other jurisdiction requested by Holdings III and reasonably acceptable to the Administrative Agent.

"Foreign Pledge Agreement" means any share pledge agreement that is not governed by the Laws of the United States, any state thereof or the District of Columbia.

"Foreign Reorganization" means the transfer of any Foreign Subsidiary of the Issuer or any transfer of any assets or property of any Foreign Subsidiary of the Issuer to Foreign Acquisition Co. or any Subsidiary thereof; *provided* that such transferred Foreign Subsidiary and any Person who holds such transferred assets or property (in each case, a "Transferred Foreign Subsidiary") shall become a Guarantor of the Obligations and Foreign Acquisition Co., shall pledge or cause to be pledged 100% of the Equity Interests of such Transferred Foreign Subsidiary to secure the Obligations (in each case, as defined in the Senior Credit Agreement).

"Foreign Subsidiary" means, with respect to any Person, any Restricted Subsidiary of such Person that is not organized or existing under the laws of the United States, any state thereof, the District of Columbia, or any territory thereof and any Restricted Subsidiary of such Foreign Subsidiary.

"General Intangibles" has the meaning specified in Article 9 of the New York UCC and includes corporate or other business records, indemnification claims, contract rights (including rights under leases, whether entered into as lessor or lessee, Swap Contracts and other agreements), goodwill, registrations, franchises, tax refund claims and any letter of credit, guarantee, claim, security interest or other security held by or granted to any Grantor, as the case may be, to secure payment by an Account Debtor of any of the Accounts; provided that General Intangibles shall not include any intellectual property and related assets subject to the Intellectual Property Security Agreement (or any intellectual property and related assets otherwise specifically excluded from the definition of "Collateral" (as defined therein)).

- "Governmental Authority" means any nation or government, any state or other political subdivision thereof, any agency, authority, instrumentality, regulatory body, court, administrative tribunal, central bank or other entity exercising executive, legislative, judicial, taxing, regulatory or administrative powers or functions of or pertaining to government.
- "Grantor" means each of Holdings IV (other than for purposes of Article III), Holdings V, the Issuer, SigmaTel and each other Restricted Subsidiary that is a Material Domestic Subsidiary.
 - "Holders" has the meaning assigned to such term in the preamble.
- **"Indemnitee"** means the Notes Collateral Agent, together with its Affiliates, and the officers, directors, employees, agents and attorneys-in-fact of the Notes Collateral Agent and Affiliates.
- "Intellectual Property Security Agreement" means the Intellectual Property Security Agreement, substantially in the form attached as Exhibit III.
 - "Intercreditor Agreement" has the meaning assigned to such term in the preamble.
- **"Material Domestic Subsidiary"** means, at any date of determination, each of Holdings III's Domestic Subsidiaries other than Holdings V and the Issuer (a) whose total assets at the last day of the most recent test period were equal to or greater than 5% of at such date or (b) whose gross revenues for such test period were equal to or greater than 5% of the consolidated gross revenues of Holdings III and the Restricted Subsidiaries for such period, determined in accordance with GAAP.
 - "New York UCC" means the Uniform Commercial Code as from time to time in effect in the State of New York.
 - "Non-Loan Party" means any Subsidiary of Holdings III that is not a Loan Party.
 - "Notes" has the meaning assigned to such term in the preamble.
 - "Notes Documents" means the Indenture, the Notes and the Collateral Documents relating to the Notes.
 - "Obligations" has the meaning assigned to such term in the Indenture.
 - "Other Parent Guarantors" means Freescale Semiconductor, Ltd. and Freescale Semiconductor Holdings II, Ltd.
- **"Perfection Certificate"** means a certificate substantially in the form of Exhibit II, completed and supplemented with the schedules and attachments contemplated thereby, and duly executed by the chief financial officer and the chief legal officer of each of Holdings III, Holdings IV Holdings V, SigmaTel and the Issuer.

- "Permitted Acquisition" has the meaning specified in Section 7.02(j) of the Senior Credit Agreement.
- "Permitted Intercompany Transfer" means any consolidation, merger, winding up, sale, assignment, transfer, lease, conveyance or other disposal of all or substantially all of the assets of any Other Parent Guarantor, Holdings III or Holdings IV with, into or to any other Person that expressly assumes all the obligations of such Other Parent Guarantor, Holdings III or Holdings IV, as applicable, under this Agreement (such Person, a "Successor Person"); provided (i) with respect to any Other Parent Guarantor, the Successor Person is any Other Parent Guarantor, Holdings IV, or Holdings IV, (ii) with respect to Holdings III, the Successor Person is Holdings IV or Holdings IV or
 - "Pledged Collateral" has the meaning assigned to such term in Section 2.01.
 - "Pledged Debt" has the meaning assigned to such term in Section 2.01.
 - "Pledged Equity" has the meaning assigned to such term in Section 2.01.
- **"Pledged Securities"** means any promissory notes, stock certificates or other securities now or hereafter included in the Pledged Collateral, including all certificates, instruments or other documents representing or evidencing any Pledged Collateral.
 - "Restricted Subsidiary" has the meaning assigned to such term in the Senior Credit Agreement.
 - "Secured Obligations" means Obligations under the Additional First Lien Debt Documents relating to the Notes.
 - "Secured Parties" means, collectively, the Notes Collateral Agent, the Holders and the Trustee to the Indenture.
 - "Security Agreement Supplement" means an instrument in the form of Exhibit I hereto.
 - "Security Interest" has the meaning assigned to such term in Section 3.01(a).
- "Senior Credit Agreement" means that Credit Agreement dated as of December 1, 2006 (as amended, supplemented or otherwise modified from time to time), among the Issuer, Holdings, IV, Holdings V, Holdings III, each lender from time to time party thereto and the Administrative Agent.

"Swap Contracts" means (a) any and all rate swap transactions, basis swaps, credit derivative transactions, forward rate transactions, commodity swaps, commodity options, forward commodity contracts, equity or equity index swaps or options, bond or bond price or bond index swaps or options or forward bond or forward bond price or forward bond index transactions, interest rate options, forward foreign exchange transactions, cap transactions, floor transactions, collar transactions, currency swap transactions, cross-currency rate swap transactions, currency options, spot contracts, or any other similar transactions or any combination of any of the foregoing (including any options to enter into any of the foregoing), whether or not any such transaction is governed by or subject to any master agreement, and (b) any and all transactions of any kind, and the related confirmations, which are subject to the terms and conditions of, or governed by, any form of master agreement published by the International Swaps and Derivatives Association, Inc., any International Foreign Exchange Master Agreement, or any other master agreement (any such master agreement, together with any related schedules, a "Master Agreement"), including any such obligations or liabilities under any Master Agreement.

"Unrestricted Subsidiary" has the meaning assigned to such term in the Senior Credit Agreement.

SECTION 1.03. <u>Notes Collateral Agent</u>. Pursuant to Section 11.01(a) of the Indenture, Citibank, N.A. hereby accepts the appointment by the Trustee and the Holders as the Notes Collateral Agent.

ARTICLE II

Pledge of Securities

SECTION 2.01. <u>Pledge</u>. As security for the payment or performance, as the case may be, in full of the Secured Obligations, including the Guarantees, each Grantor hereby assigns and pledges to the Notes Collateral Agent, its successors and assigns, for the benefit of the Secured Parties, and hereby grants to the Notes Collateral Agent, its successors and assigns, for the benefit of the Secured Parties, a security interest in, all of such Grantor's right, title and interest in, to and under (i) all Equity Interests held by it and listed on Schedule I and any other Equity Interests obtained in the future by such Grantor and the certificates representing all such Equity Interests (the "**Pledged Equity**"); *provided* that the Pledged Equity shall not include (A) more than 65% of the issued and outstanding voting Equity Interests of any Material Foreign Subsidiary that is a direct or indirect Subsidiary of Holdings V, (B) Equity Interests of any Foreign Subsidiary that is not a Material Foreign Subsidiary, (C) Equity Interests of any Unrestricted Subsidiary, (D) Equity Interests of any Subsidiary of a Foreign Subsidiary that is a direct or indirect Subsidiary of Holdings V, (E) Equity Interests of any Foreign Subsidiary that are pledged pursuant to a Foreign Pledge Agreement, (F) Equity Interests of any Subsidiary acquired pursuant to a Permitted Acquisition financed with Indebtedness incurred pursuant to Section 7.03(g) of the Senior Credit Agreement if such Equity Interests serve as security for such Indebtedness or if the terms of such Indebtedness prohibit the creation of any other lien on such Equity Interests, (G) Equity Interests of any Person that is

not an indirect, wholly owned Subsidiary of Holdings III, (H) (i) if there are outstanding Obligations under the Senior Credit Facilities, Equity Interests of any Subsidiary with respect to which the Administrative Agent has confirmed in writing to the Issuer its determination that the costs of providing a pledge of its Equity Interests or perfection thereof is excessive in view of the benefits to be obtained by the secured parties under the Senior Credit Agreement or (ii) if there are no outstanding Obligations under the Senior Credit Facilities, Equity Interests of any Subsidiary with respect to which the board of directors or the senior management of the Issuer has confirmed in writing to the Trustee and the Notes Collateral Agent its reasonable determination that the costs of providing a pledge of its Equity Interests or perfection thereof is excessive in view of the benefits to be obtained by the Secured Parties, and (I) pledges prohibited by law or by agreements containing anti-assignment clauses not overridden by applicable law; (ii) other than in the case of Holdings IV (A) the debt securities owned by it and listed opposite the name of such Grantor on Schedule I, (B) any debt securities obtained in the future by such Grantor and (C) the promissory notes and any other instruments evidencing such debt securities (the "Pledged Debt"); (iii) all other property that may be delivered to and held by the Notes Collateral Agent; (iv) subject to Section 2.06, all payments of principal or interest, dividends, cash, instruments and other property from time to time received, receivable or otherwise distributed in respect of, in exchange for or upon the conversion of, and all other Proceeds received in respect of, the securities referred to in clauses (i) and (ii) above; (v) subject to Section 2.06, all rights and privileges of such Grantor with respect to the securities and other property referred to in clauses (i), (iii) and (iv) above; and (vi) all Proceeds of any of the foregoing (the items referred to in clause

TO HAVE AND TO HOLD the Pledged Collateral, together with all right, title, interest, powers, privileges and preferences pertaining or incidental thereto, unto the Notes Collateral Agent, its successors and assigns, for the benefit of the Secured Parties, forever, subject, however, to the terms, covenants and conditions hereinafter set forth.

SECTION 2.02. <u>Delivery of the Pledged Collateral</u>. Subject to the terms of the Intercreditor Agreement:

(a) each Grantor agrees promptly to deliver or cause to be delivered to the Notes Collateral Agent, for the benefit of the Secured Parties, any and all Pledged Securities (other than any uncertificated securities, but only for so long as such securities remain uncertificated) to the extent such Pledged Securities are required to be delivered pursuant to the Intercreditor Agreement.

(b) [reserved.]

(c) upon delivery to the Notes Collateral Agent, (i) any Pledged Securities shall be accompanied by stock powers duly executed in blank or other instruments of transfer reasonably satisfactory to the Notes Collateral Agent and by such other instruments and documents as the Notes Collateral Agent may reasonably request and (ii) all other property comprising part of the Pledged Collateral shall be accompanied by proper instruments of assignment duly executed by the applicable Grantor and such other instruments or documents as the Notes Collateral Agent may reasonably request. Each delivery of Pledged Securities shall be accompanied by a schedule describing the securities, which schedule shall be attached hereto as Schedule I and made a part hereof; provided that failure to attach any such schedule hereto shall not affect the validity of such pledge of such Pledged Securities. Each schedule so delivered shall supplement any prior schedules so delivered.

SECTION 2.03. <u>Representations</u>, <u>Warranties and Covenants</u>. Holdings IV (with respect to those representations, warranties and covenants regarding Pledged Equity), Holdings V, SigmaTel and the Issuer jointly and severally represent, warrant and covenant, as to themselves and the other Grantors, to and with the Notes Collateral Agent, for the benefit of the Secured Parties, that:

- (a) Schedule I correctly sets forth the percentage of the issued and outstanding units of each class of the Equity Interests of the issuer thereof represented by the Pledged Equity and includes all Equity Interests, debt securities and promissory notes required to be pledged hereunder in order to satisfy the requirements set forth in the Indenture and the other Collateral Documents relating to the Notes;
- (b) the Pledged Equity and Pledged Debt (solely with respect to Pledged Debt issued by a Person other than Holdings III or a subsidiary of Holdings III, to the best of Holdings V's and the Issuer's knowledge) have been duly and validly authorized and issued by the issuers thereof and (i) in the case of Pledged Equity, are fully paid and nonassessable and (ii) in the case of Pledged Debt (solely with respect to Pledged Debt issued by a Person other than Holdings III or a subsidiary of Holdings III, to the best of Holdings V's and the Issuer's knowledge), are legal, valid and binding obligations of the issuers thereof;
- (c) except for the security interests granted hereunder, each of the Grantors (i) is and, subject to any transfers made in compliance with the Senior Credit Agreement and the Notes Documents, will continue to be the direct owner, beneficially and of record, of the Pledged Securities indicated on Schedule I as owned by such Grantors, (ii) holds the same free and clear of all Liens, other than (A) Liens created by this Agreement and the other Collateral Documents relating to the Notes and (B) Liens expressly permitted pursuant to Section 4.12 of the Indenture, (iii) will make no assignment, pledge, hypothecation or transfer of, or create or permit to exist any security interest in or other Lien on, the Pledged Collateral, other than (A) Liens created by this Agreement and the other Notes Documents and (B) Liens expressly permitted pursuant to Section 4.12 of the Indenture, and (iv) will defend its title or interest thereto or therein against any and all Liens (other than the Liens permitted pursuant to this Section 2.03(c)), however arising, of all Persons whomsoever;

- (d) except for restrictions and limitations imposed by the Notes Documents, the other First Lien Debt Documents or the Second Lien Facility Documents (as defined in the Senior Credit Agreement) or securities laws generally and except as described in the Perfection Certificate, the Pledged Collateral is and will continue to be freely transferable and assignable, and none of the Pledged Collateral is or will be subject to any option, right of first refusal, shareholders agreement, charter or by-law provisions or contractual restriction of any nature that might prohibit, impair, delay or otherwise affect in any manner material and adverse to the Secured Parties the pledge of such Pledged Collateral hereunder, the sale or disposition thereof pursuant hereto or the exercise by the Notes Collateral Agent of rights and remedies hereunder;
- (e) each of the Grantors has the power and authority to pledge the Pledged Collateral pledged by it hereunder in the manner hereby done or contemplated;
- (f) no consent or approval of any Governmental Authority, any securities exchange or any other Person was or is necessary to the validity of the pledge effected hereby (other than such as have been obtained and are in full force and effect);
- (g) by virtue of the execution and delivery by the Grantors of this Agreement, when any Pledged Securities are delivered to and held by or on behalf of the Notes Collateral Agent in accordance with this Agreement, the Notes Collateral Agent will obtain a legal, valid and perfected lien upon and security interest in such Pledged Securities as security for the payment and performance of the Secured Obligations; and
- (h) the pledge effected hereby is effective to vest in the Notes Collateral Agent, for the benefit of the Secured Parties, the rights of the Notes Collateral Agent in the Pledged Collateral as set forth herein.

SECTION 2.04. <u>Certification of Limited Liability Company and Limited Partnership Interests</u>. Subject to the terms of the Intercreditor Agreement, each certificate representing an interest in any limited liability company or limited partnership controlled by any Grantor and pledged under Section 2.01 shall be delivered to the Notes Collateral Agent.

SECTION 2.05. Registration in Nominee Name; Denominations. Subject to the terms of the Intercreditor Agreement, if an Event of Default shall occur and be continuing and the Notes Collateral Agent shall give the Issuer notice of its intent to exercise such rights, (a) the Notes Collateral Agent, on behalf of the Secured Parties, shall have the right (in its sole and absolute discretion) to hold the Pledged Securities in its own name as pledgee, the name of its nominee (as pledgee or as sub-agent) or the name of the applicable Grantor, endorsed or assigned in blank or in favor of the Notes Collateral Agent, and each Grantor will promptly give to the Notes Collateral Agent copies of any notices or other communications received by it with respect to Pledged Securities registered in the name of such Grantor and (b) the Notes Collateral Agent shall have the right to exchange the certificates representing Pledged Securities for certificates of smaller or larger denominations for any purpose consistent with this Agreement.

SECTION 2.06. Voting Rights; Dividends and Interest.

- (a) Unless and until an Event of Default shall have occurred and be continuing and the Notes Collateral Agent shall have notified the Issuer that the rights of the Grantors under this Section 2.06 are being suspended:
 - (i) Each Grantor shall be entitled to exercise any and all voting and/or other consensual rights and powers inuring to an owner of Pledged Securities or any part thereof for any purpose consistent with the terms of this Agreement, the Indenture and the other Notes Documents; *provided* that such rights and powers shall not be exercised in any manner that could materially and adversely affect the rights inuring to a holder of any Pledged Securities or the rights and remedies of any of the Notes Collateral Agent or the other Secured Parties under this Agreement, the Indenture or any other Notes Document or the ability of the Secured Parties to exercise the same.
 - (ii) The Notes Collateral Agent shall execute and deliver to each Grantor, or cause to be executed and delivered to each Grantor, all such proxies, powers of attorney and other instruments as each Grantor may reasonably request for the purpose of enabling such Grantor to exercise the voting and/or consensual rights and powers it is entitled to exercise pursuant to subparagraph (i) above.
 - (iii) Each Grantor shall be entitled to receive and retain any and all dividends, interest, principal and other distributions paid on or distributed in respect of the Pledged Securities to the extent and only to the extent that such dividends, interest, principal and other distributions are permitted by, and otherwise paid or distributed in accordance with, the terms and conditions of the Indenture, the other Notes Documents and applicable Laws; provided that any noncash dividends, interest, principal or other distributions that would constitute Pledged Equity or Pledged Debt, whether resulting from a subdivision, combination or reclassification of the outstanding Equity Interests of the issuer of any Pledged Securities or received in exchange for Pledged Securities or any part thereof, or in redemption thereof, or as a result of any merger, consolidation, acquisition or other exchange of assets to which such issuer may be a party or otherwise, shall be and become part of the Pledged Collateral, and, if received by any Grantor, shall not be commingled by such Grantor with any of its other funds or property but shall be held separate and apart therefrom, shall be held in trust for the benefit of the Notes Collateral Agent and the Secured Parties and shall be forthwith delivered to the Notes Collateral Agent in the same form as so received (with any necessary endorsement reasonably requested by the Notes Collateral Agent).

- (b) Subject to the terms of the Intercreditor Agreement, upon the occurrence and during the continuance of an Event of Default, after the Notes Collateral Agent shall have notified the Issuer of the suspension of the rights of the Grantors under paragraph (a)(iii) of this Section 2.06, then all rights of any Grantor to dividends, interest, principal or other distributions that such Grantor is authorized to receive pursuant to paragraph (a)(iii) of this Section 2.06 shall cease, and all such rights shall thereupon become vested in the Notes Collateral Agent, which shall have the sole and exclusive right and authority to receive and retain such dividends, interest, principal or other distributions received by any Grantor contrary to the provisions of this Section 2.06 shall be held in trust for the benefit of the Notes Collateral Agent, shall be segregated from other property or funds of such Grantor and shall be forthwith delivered to the Notes Collateral Agent upon demand in the same form as so received (with any necessary endorsement reasonably requested by the Notes Collateral Agent). Subject to the terms of the Intercreditor Agreement, any and all money and other property paid over to or received by the Notes Collateral Agent pursuant to the provisions of this paragraph (b) shall be retained by the Notes Collateral Agent in an account to be established by the Notes Collateral Agent upon receipt of such money or other property and shall be applied in accordance with Section 4.02. After all Events of Default have been cured or waived, the Notes Collateral Agent shall promptly repay to each Grantor (without interest) all dividends, interest, principal or other distributions that such Grantor would otherwise be permitted to retain pursuant to the terms of paragraph (a)(iii) of this Section 2.06 and that remain in such account.
- (c) Subject to the terms of the Intercreditor Agreement, upon the occurrence and during the continuance of an Event of Default, after the Notes Collateral Agent shall have notified the Issuer of the suspension of the rights of the Grantors under paragraph (a)(i) of this Section 2.06, then all rights of any Grantor to exercise the voting and consensual rights and powers it is entitled to exercise pursuant to paragraph (a)(i) of this Section 2.06, and the obligations of the Notes Collateral Agent under paragraph (a)(ii) of this Section 2.06, shall cease, and all such rights shall thereupon become vested in the Notes Collateral Agent, which shall have the sole and exclusive right and authority to exercise such voting and consensual rights and powers; *provided* that, unless otherwise directed by Holders of more than 50% in principal amount of the total outstanding Notes, the Notes Collateral Agent shall have the right from time to time following and during the continuance of an Event of Default to permit the Grantors to exercise such rights. After all Events of Default have been cured or waived, each Grantor shall have the exclusive right to exercise the voting and/or consensual rights and powers that such Grantor would otherwise be entitled to exercise pursuant to the terms of paragraph (a)(i) of this Section 2.06.
- (d) Any notice given by the Notes Collateral Agent to the Issuer suspending the rights of the Grantors under paragraph (a) of this Section 2.06 (i) shall be given in writing, (ii) may be given with respect to one or more of the Grantors at the same or different times and (iii) may suspend the rights of the Grantors under paragraph (a)(i) or paragraph (a)(iii) of this Section 2.06 in part without suspending all such rights (as specified by the Notes Collateral Agent in its sole and absolute discretion) and without waiving or otherwise affecting the Notes Collateral Agent's rights to give additional notices from time to time suspending other rights so long as an Event of Default has occurred and is continuing.

ARTICLE III

Security Interests in Personal Property

SECTION 3.01. Security Interest.

(a) As security for the payment or performance, as the case may be, in full of the Secured Obligations, including the Guarantees, each Grantor hereby assigns and pledges to the Notes Collateral Agent, its successors and assigns, for the benefit of the Secured Parties, and hereby grants to the Notes Collateral Agent, its successors and assigns, for the benefit of the Secured Parties, a security interest (the "Security Interest") in all right, title or interest in or to any and all of the following assets and properties now owned or at any time hereafter acquired by such Grantor or in which such Grantor now has or at any time in the future may acquire any right, title or interest (collectively, the "Article 9 Collateral"):

- (i) all Property;
- (ii) all Accounts;
- (iii) all Chattel Paper;
- (iv) all Commercial Tort Claims listed on Schedule II hereto;
- (v) all Deposit Accounts;
- (vi) all Documents;
- (vii) all Equipment;
- (viii) all General Intangibles;
- (ix) all Instruments;
- (x) all Inventory;
- (xi) all Investment Property;
- (xii) all books and records pertaining to the Article 9 Collateral; and

(xiii) to the extent not otherwise included, all Proceeds and products of any and all of the foregoing and all supporting obligations, collateral security and guarantees given by any Person with respect to any of the foregoing;

provided that notwithstanding anything to the contrary in this Agreement, this Agreement shall not constitute a grant of a security interest in (A) any letter-of-credit rights, (B) any Securitization Assets, (C) motor vehicles and other assets subject to certificates of title, (D) any Equity Interests in any Unrestricted Subsidiary or any Equity Interests of any Subsidiary acquired pursuant to a Permitted Acquisition financed with Indebtedness

incurred pursuant to Section 7.03(g) of the Senior Credit Agreement if such Equity Interests serve as security for such Indebtedness or if the terms of such Indebtedness prohibit the creation of any other lien on such Equity Interests, (E) more than 65% of the issued and outstanding voting Equity Interests of any Material Foreign Subsidiary that is a direct or indirect subsidiary of Holdings, (F) Equity Interests of any Foreign Subsidiary that is not a Material Foreign Subsidiary, (G) Equity Interests of any Subsidiary of a Foreign Subsidiary that is a direct or indirect Subsidiary of Holdings, (H) Equity Interests of any Foreign Subsidiary that are pledged pursuant to a Foreign Pledge Agreement, (I) Equity Interests of any Person that is not an indirect, wholly owned Subsidiary of Holdings III, (J) (i) if there are outstanding Obligations under the Senior Credit Facilities, any asset with respect to which the Administrative Agent has confirmed in writing to the Issuer its determination that the costs of providing a security interest in such asset or perfection thereof is excessive in view of the benefits to be obtained by the secured parties under the Senior Credit Agreement or (ii) if there are no outstanding Obligations under the Senior Credit Facilities, any asset with respect to which the board of directors or the senior management of the Issuer has confirmed in writing to the Trustee and the Notes Collateral Agent its reasonable determination that the costs of providing a security interest in such asset or perfection thereof is excessive in view of the benefits to be obtained by the Secured Parties, (K) security interests prohibited by law or by agreements containing anti-assignment clauses not overridden by the UCC or other applicable law or (L) any General Intangible, Investment Property or other rights of a Grantor arising under any contract, lease, instrument, license or other document or any assets subject thereto if (but only to the extent that) the grant of a security interest therein would (x) constitute a violation of a valid and enforceable restriction in respect of such General Intangible, Investment Property or other such rights in favor of a third party or under any law, regulation, permit, order or decree of any Governmental Authority, unless and until all required consents shall have been obtained (for the avoidance of doubt, the restrictions described herein shall not include negative pledges or similar undertakings in favor of a lender or other financial counterparty) or (y) expressly give any other party in respect of any such contract, lease, instrument, license or other document, the right to terminate its obligations thereunder, provided, however, that the limitation set forth in clause (L) above shall not affect, limit, restrict or impair the grant by a Grantor of a security interest pursuant to this Agreement in any such Collateral to the extent that an otherwise applicable prohibition or restriction on such grant is rendered ineffective by any applicable law, including the Uniform Commercial Code. Each Grantor shall, if requested to do so by the Trustee, use commercially reasonable efforts to obtain any such required consent that is reasonably obtainable with respect to Collateral which the Trustee reasonably determines to be material.

(b) Each Grantor hereby irrevocably authorizes the Notes Collateral Agent for the benefit of the Secured Parties at any time and from time to time to file in any relevant jurisdiction any initial financing statements (including fixture filings) with respect to the Article 9 Collateral or any part thereof and amendments thereto that (i) indicate the Collateral as all assets of such Grantor or words of similar effect as being of an equal or lesser scope or with greater detail, and (ii) contain the information required by Article 9 of the Uniform Commercial Code or the analogous legislation of each applicable jurisdiction for the filing of any financing statement or amendment, including

- (A) whether such Grantor is an organization, the type of organization and any organizational identification number issued to such Grantor and (B) in the case of a financing statement filed as a fixture filing, a sufficient description of the real property to which such Article 9 Collateral relates. Each Grantor agrees to provide such information to the Notes Collateral Agent promptly upon request.
- (c) The Security Interest is granted as security only and shall not subject the Notes Collateral Agent or any other Secured Party to, or in any way alter or modify, any obligation or liability of any Grantor with respect to or arising out of the Article 9 Collateral.
- (d) Notwithstanding anything to the contrary in this Agreement or the Indenture, none of the Grantors shall be required to enter into any deposit account control agreement or securities account control agreement with respect to any deposit account or securities account.
 - SECTION 3.02. <u>Representations and Warranties</u>. Holdings V, the Issuer and SigmaTel jointly and severally represent and warrant, as to themselves and the other Grantors, to the Notes Collateral Agent and the Secured Parties that:
- (a) Each Grantor has good and valid rights in and title to the Article 9 Collateral with respect to which it has purported to grant a Security Interest hereunder and has full power and authority to grant to the Notes Collateral Agent the Security Interest in such Article 9 Collateral pursuant hereto and to execute, deliver and perform its obligations in accordance with the terms of this Agreement, without the consent or approval of any other Person other than any consent or approval that has been obtained.
- (b) The Perfection Certificate has been duly prepared, completed and executed and the information set forth therein, including the exact legal name of each Grantor, is correct and complete in all material respects as of the Closing Date. The UCC financing statements (including fixture filings, as applicable) or other appropriate filings, recordings or registrations prepared by the Notes Collateral Agent based upon the information provided to the Notes Collateral Agent in the Perfection Certificate for filing in each governmental, municipal or other office specified in Schedule 6 to the Perfection Certificate (or specified by notice from the Issuer to the Notes Collateral Agent after the Closing Date in the case of filings, recordings or registrations required by the Indenture), are all the filings, recordings and registrations that are necessary to establish a legal, valid and perfected security interest in favor of the Notes Collateral Agent (for the benefit of the Secured Parties) in respect of all Article 9 Collateral in which the Security Interest may be perfected by filing, recording or registration in the United States (or any political subdivision thereof) and its territories and possessions pursuant to the Uniform Commercial Code in the relevant jurisdiction, and no further or subsequent filing, refiling, recording, rerecording, registration or reregistration is necessary in any such jurisdiction, except as provided under applicable law with respect to the filing of continuation statements.

- (c) The Security Interest constitutes (i) a legal and valid security interest in all the Article 9 Collateral securing the payment and performance of the Secured Obligations and (ii) subject to the filings described in Section 3.02(b), a perfected security interest in all Article 9 Collateral in which a security interest may be perfected by filing, recording or registering a financing statement or analogous document in the United States (or any political subdivision thereof) and its territories and possessions pursuant to the Uniform Commercial Code in the relevant jurisdiction. The Security Interest is and shall be prior to any other Lien on any of the Article 9 Collateral, other than (i) any nonconsenual Lien that is expressly permitted pursuant to Section 4.12 of the Indenture and has priority as a matter of law and (ii) Liens expressly permitted pursuant to Section 4.12 of the Indenture.
- (d) The Article 9 Collateral is owned by the Grantors free and clear of any Liens, except for Liens expressly permitted pursuant to Section 4.12 of the Indenture. None of the Grantors has filed or consented to the filing of (i) any financing statement or analogous document under the New York UCC or any other applicable laws covering any Article 9 Collateral or (ii) any assignment in which any Grantor assigns any Article 9 Collateral or any security agreement or similar instrument covering any Article 9 Collateral with any foreign governmental, municipal or other office, which financing statement or analogous document, assignment, security agreement or similar instrument is still in effect, except, in each case, for Liens expressly permitted pursuant to Section 4.12 of the Indenture.

SECTION 3.03. Covenants.

- (a) The Issuer agrees promptly to notify the Notes Collateral Agent in writing of any change (i) in legal name of any Grantor, (ii) in the identity or type of organization or corporate structure of any Grantor, or (iii) in the jurisdiction of organization of any Grantor.
- (b) Each Grantor shall, at its own expense, take any and all commercially reasonable actions necessary to defend title to the Article 9 Collateral against all Persons and to defend the Security Interest of the Notes Collateral Agent in the Article 9 Collateral and the priority thereof against any Lien not expressly permitted pursuant to Section 4.12 of the Indenture.
- (c) Each year, at the time of delivery of annual financial statements with respect to the preceding fiscal year pursuant to Section 4.03 of the Indenture, the Issuer shall deliver to the Notes Collateral Agent a certificate executed by the chief financial officer and the chief legal officer of the Issuer setting forth the information required pursuant to Sections 1(a), 1(c), 1(d), 2(b) and 12 of the Perfection Certificate or confirming that there has been no change in such information since the date of such certificate or the date of the most recent certificate delivered pursuant to this Section 3.03(c) and certifying that all UCC financing statements and other appropriate filings, recordings or registrations have been filed of record in each governmental, municipal or other appropriate office in each jurisdiction necessary to protect and perfect the Security Interests and Liens under this Agreement and the Intellectual Property Security Agreement for a period of not less than 18 months after the date of such certificate (except as noted therein with respect to any continuation statements to be filed within such period).

- (d) The Issuer and the Grantors shall, at their sole expense, do all acts which may be reasonably necessary, if requested by the Notes Collateral Agent, to confirm that the Notes Collateral Agent holds, for the benefit of the Holders, duly created, enforceable and perfected First Liens in the Collateral (subject to Permitted Liens) to the extent required by the Indenture and the Collateral Documents relating to the Notes. The Issuer agrees, on its own behalf and on behalf of each other Grantor, at its own expense, to execute, acknowledge, deliver and cause to be duly filed all such further instruments and documents and take all such actions as the Notes Collateral Agent may from time to time reasonably request to better assure, preserve, protect, perfect, transfer and confirm the Security Interest and the rights and remedies created hereby, including the payment of any fees and taxes required in connection with the execution and delivery of this Agreement, the granting of the Security Interest and the filing of any financing statements (including fixture filings) or other documents in connection herewith or therewith. Subject to the terms of the Intercreditor Agreement, if any amount payable under or in connection with any of the Article 9 Collateral that is in excess of \$10,000,000 shall be or become evidenced by any promissory note or other instrument, such note or instrument shall be promptly pledged and delivered to the Notes Collateral Agent, for the benefit of the Secured Parties, duly endorsed in a manner reasonably satisfactory to the Notes Collateral Agent.
- (e) Subject to the terms of the Intercreditor Agreement, at its option, the Notes Collateral Agent may discharge past due taxes, assessments, charges, fees, Liens, security interests or other encumbrances at any time levied or placed on the Article 9 Collateral and not permitted pursuant to Section 4.12 of the Indenture, and may pay for the maintenance and preservation of the Article 9 Collateral to the extent any Grantor fails to do so as required by the Indenture or this Agreement and within a reasonable period of time after the Notes Collateral Agent has requested that it do so, and each Grantor jointly and severally agrees to reimburse the Notes Collateral Agent within 10 days after demand for any payment made or any reasonable expense incurred by the Notes Collateral Agent pursuant to the foregoing authorization. Nothing in this paragraph shall be interpreted as excusing any Grantor from the performance of, or imposing any obligation on the Notes Collateral Agent or any Secured Party to cure or perform, any covenants or other promises of any Grantor with respect to taxes, assessments, charges, fees, Liens, security interests or other encumbrances and maintenance as set forth herein, or in the other Notes Documents.
- (f) If at any time any Grantor shall take a security interest in any property of an Account Debtor or any other Person, the value of which is in excess of \$10,000,000, to secure payment and performance of an Account, such Grantor shall promptly assign such security interest to the Notes Collateral Agent for the benefit of the Secured Parties. Such assignment need not be filed of public record unless necessary to continue the perfected status of the security interest against creditors of and transferees from the Account Debtor or other Person granting the security interest.

- (g) Each Grantor (rather than the Notes Collateral Agent or any Secured Party) shall remain liable (as between itself and any relevant counterparty) to observe and perform all the conditions and obligations to be observed and performed by it under each contract, agreement or instrument relating to the Article 9 Collateral, all in accordance with the terms and conditions thereof, and each Grantor jointly and severally agrees to indemnify and hold harmless the Notes Collateral Agent and the Secured Parties from and against any and all liability for such performance.
- (h) If any Grantor shall at any time hold or acquire a Commercial Tort Claim with a value in excess of \$10,000,000, such Grantor shall promptly notify the Notes Collateral Agent in writing signed by such Grantor of the brief details thereof and grant to the Notes Collateral Agent a security interest therein and in the Proceeds thereof, all upon the terms of this Agreement pursuant to a document in form and substance reasonably satisfactory to the Notes Collateral Agent.
 - SECTION 3.04. Other Actions. Subject to the terms of the Intercreditor Agreement, in order to further insure the attachment, perfection and priority of, and the ability of the Notes Collateral Agent to enforce, the Security Interest, each Grantor agrees, in each case at such Grantor's own expense, to take the following actions with respect to the following Article 9 Collateral:
- (a) *Instruments*. If any Grantor shall at any time hold or acquire any Instruments constituting Collateral and evidencing an amount in excess of \$10,000,000, such Grantor shall forthwith endorse, assign and deliver the same to the Notes Collateral Agent for the benefit of the Secured Parties, accompanied by such instruments of transfer or assignment duly executed in blank as the Notes Collateral Agent may from time to time reasonably request.
- (b) *Investment Property*. Except to the extent otherwise provided in Article II, if any Grantor shall at any time hold or acquire any certificated securities, such Grantor shall forthwith endorse, assign and deliver the same to the Notes Collateral Agent for the benefit of the Secured Parties, accompanied by such instruments of transfer or assignment duly executed in blank as the Notes Collateral Agent may from time to time reasonably request. If any securities now or hereafter acquired by any Grantor are uncertificated and are issued to such Grantor or its nominee directly by the issuer thereof, upon the Notes Collateral Agent's request and following the occurrence of an Event of Default such Grantor shall promptly notify the Notes Collateral Agent thereof and, at the Notes Collateral Agent's reasonable request, pursuant to an agreement in form and substance reasonably satisfactory to the Notes Collateral Agent, either (i) cause the issuer to agree to comply with instructions from the Notes Collateral Agent as to such securities, without further consent of any Grantor or such nominee, or (ii) arrange for the Notes Collateral Agent to become the registered owner of the securities. If any securities, whether certificated or uncertificated, or other investment property are held by any Grantor or its nominee through a securities intermediary or commodity intermediary, upon the Notes Collateral Agent's request and following the occurrence of an Event of Default, such Grantor shall immediately notify the Notes Collateral Agent thereof and at the Notes Collateral Agent's request and option, pursuant to an agreement in form and

substance reasonably satisfactory to the Notes Collateral Agent shall either (i) cause such securities intermediary or (as the case may be) commodity intermediary to agree to comply with entitlement orders or other instructions from the Notes Collateral Agent to such securities intermediary as to such security entitlements, or (as the case may be) to apply any value distributed on account of any commodity contract as directed by the Notes Collateral Agent to such commodity intermediary, in each case without further consent of any Grantor or such nominee, or (ii) in the case of financial assets or other Investment Property held through a securities intermediary, arrange for the Notes Collateral Agent to become the entitlement holder with respect to such Investment Property, with the Grantor being permitted, only with the consent of the Notes Collateral Agent, to exercise rights to withdraw or otherwise deal with such Investment Property. The Notes Collateral Agent agrees with each of the Grantors that the Notes Collateral Agent shall not give any such entitlement orders or instructions or directions to any such issuer, securities intermediary or commodity intermediary, and shall not withhold its consent to the exercise of any withdrawal or dealing rights by any Grantor, unless an Event of Default has occurred and is continuing. The provisions of this paragraph shall not apply to any financial assets credited to a securities account for which the Notes Collateral Agent is the securities intermediary.

ARTICLE IV

Remedies

SECTION 4.01. Remedies upon Default. Subject to the terms of the Intercreditor Agreement, upon the occurrence and during the continuance of an Event of Default, it is agreed that the Notes Collateral Agent shall have the right to exercise any and all rights afforded to a secured party with respect to the Secured Obligations under the Uniform Commercial Code or other applicable law and also may (i) require each Grantor to, and each Grantor agrees that it will at its expense and upon request of the Notes Collateral Agent forthwith, assemble all or part of the Collateral as directed by the Notes Collateral Agent and make it available to the Notes Collateral Agent at a place and time to be designated by the Notes Collateral Agent that is reasonably convenient to both parties; (ii) occupy any premises owned or, to the extent lawful and permitted, leased by any of the Grantors where the Collateral or any part thereof is assembled or located for a reasonable period in order to effectuate its rights and remedies hereunder or under law, without obligation to such Grantor in respect of such occupation; provided that the Notes Collateral Agent shall provide the applicable Grantor with notice thereof prior to or promptly after such occupancy; (iii) exercise any and all rights and remedies of any of the Grantors under or in connection with the Collateral, or otherwise in respect of the Collateral; provided that the Notes Collateral Agent shall provide the applicable Grantor with notice thereof prior to or promptly after such exercise; and (iv) subject to the mandatory requirements of applicable law and the notice requirements described below, sell or otherwise dispose of all or any part of the Collateral securing the Secured Obligations at a public or private sale or at any broker's board or on any securities exchange, for cash, upon credit or for future delivery as the Notes Collateral Agent shall deem appropriate.

Notes Collateral Agent shall be authorized at any such sale of securities (if it deems it advisable to do so) to restrict the prospective bidders or purchasers to Persons who will represent and agree that they are purchasing the Collateral for their own account for investment and not with a view to the distribution or sale thereof, and upon consummation of any such sale the Notes Collateral Agent shall have the right to assign, transfer and deliver to the purchaser or purchasers thereof the Collateral so sold. Each such purchaser at any sale of Collateral shall hold the property sold absolutely, free from any claim or right on the part of any Grantor, and each Grantor hereby waives (to the extent permitted by law) all rights of redemption, stay and appraisal which such Grantor now has or may at any time in the future have under any rule of law or statute now existing or hereafter enacted.

The Notes Collateral Agent shall give the applicable Grantors 10 days' written notice (which each Grantor agrees is reasonable notice within the meaning of Section 9-611 of the New York UCC or its equivalent in other jurisdictions) of the Notes Collateral Agent's intention to make any sale of Collateral. Such notice, in the case of a public sale, shall state the time and place for such sale and, in the case of a sale at a broker's board or on a securities exchange, shall state the board or exchange at which such sale is to be made and the day on which the Collateral, or portion thereof, will first be offered for sale at such board or exchange. Any such public sale shall be held at such time or times within ordinary business hours and at such place or places as the Notes Collateral Agent may fix and state in the notice (if any) of such sale. At any such sale, the Collateral, or portion thereof, to be sold may be sold in one lot as an entirety or in separate parcels, as the Notes Collateral Agent may (in its sole and absolute discretion) determine. The Notes Collateral Agent shall not be obligated to make any sale of any Collateral if it shall determine not to do so, regardless of the fact that notice of sale of such Collateral shall have been given. The Notes Collateral Agent may, without notice or publication, adjourn any public or private sale or cause the same to be adjourned from time to time by announcement at the time and place fixed for sale, and such sale may, without further notice, be made at the time and place to which the same was so adjourned. In case any sale of all or any part of the Collateral is made on credit or for future delivery, the Collateral so sold may be retained by the Notes Collateral Agent until the sale price is paid by the purchaser or purchasers thereof, but the Notes Collateral Agent shall not incur any liability in case any such purchaser or purchasers shall fail to take up and pay for the Collateral so sold and, in case of any such failure, such Collateral may be sold again upon like notice. At any public (or, to the extent permitted by law, private) sale made pursuant to this Agreement, any Secured Party may bid for or purchase, free (to the extent permitted by law) from any right of redemption, stay, valuation or appraisal on the part of any Grantor (all said rights being also hereby waived and released to the extent permitted by law), the Collateral or any part thereof offered for sale and may make payment on account thereof by using any claim then due and payable to such Secured Party from any Grantor as a credit against the purchase price, and such Secured Party may, upon compliance with the terms of sale, hold, retain and dispose of such property without further accountability to any Grantor therefor. For purposes hereof, a written agreement to purchase the Collateral or any portion thereof shall be treated as a sale thereof; the Notes Collateral Agent shall be free to carry out such sale pursuant to such agreement and no Grantor shall be entitled to the return of the Collateral

or any portion thereof subject thereto, notwithstanding the fact that after the Notes Collateral Agent shall have entered into such an agreement all Events of Default shall have been remedied and the Secured Obligations paid in full. As an alternative to exercising the power of sale herein conferred upon it, the Notes Collateral Agent may proceed by a suit or suits at law or in equity to foreclose this Agreement and to sell the Collateral or any portion thereof pursuant to a judgment or decree of a court or courts having competent jurisdiction or pursuant to a proceeding by a court appointed receiver. Any sale pursuant to the provisions of this Section 4.01 shall be deemed to conform to the commercially reasonable standards as provided in Section 9-610(b) of the New York UCC or its equivalent in other jurisdictions.

Each Grantor irrevocably makes, constitutes and appoints the Notes Collateral Agent (and all officers, employees or agents designated by the Notes Collateral Agent) as such Grantor's true and lawful agent (and attorney-in-fact) during the continuance of an Event of Default and after notice to the Issuer of its intent to exercise such rights, for the purpose of (i) making, settling and adjusting claims in respect of Article 9 Collateral under policies of insurance, endorsing the name of such Grantor on any check, draft, instrument or other item of payment for the proceeds of such policies of insurance, (ii) making all determinations and decisions with respect thereto and (iii) obtaining or maintaining the policies of insurance required by the Collateral Documents or paying any premium in whole or in part relating thereto. All sums disbursed by the Notes Collateral Agent in connection with this paragraph, including reasonable attorneys' fees, court costs, expenses and other charges relating thereto, shall be payable, within 10 days of demand, by the Grantors to the Notes Collateral Agent and shall be additional Secured Obligations secured hereby.

SECTION 4.02. Application of Proceeds.

(a) Subject to the terms of the Intercreditor Agreement, the Notes Collateral Agent shall apply the proceeds of any collection or sale of Collateral, including any Collateral consisting of cash, as follows:

<u>First</u>, to pay Secured Obligations in respect of incurred and unpaid fees and expenses of the Notes Collateral Agent and the Trustee under the Notes Documents;

<u>Second</u>, towards payment of amounts then due and owing and remaining unpaid in respect of the Secured Obligations, *pro rata* among the Secured Parties according to the amounts of the Secured Obligations then due and owing and remaining unpaid to the Secured Parties.

<u>Third</u>, towards payment of any remaining Secured Obligations, *pro rata* among the Secured Parties according to the amounts of the Secured Obligations then held by the Secured Parties; and

<u>Last</u>, any balance remaining after the Secured Obligations shall have been paid in full shall be paid over to the Issuer or to whomsoever may be lawfully entitled to receive the same.

The Notes Collateral Agent shall have absolute discretion as to the time of application of any such proceeds, moneys or balances in accordance with this Agreement. Upon any sale of Collateral by the Notes Collateral Agent (including pursuant to a power of sale granted by statute or under a judicial proceeding), the receipt of the Notes Collateral Agent or of the officer making the sale shall be a sufficient discharge to the purchaser or purchasers of the Collateral so sold and such purchaser or purchasers shall not be obligated to see to the application of any part of the purchase money paid over to the Notes Collateral Agent or such officer or be answerable in any way for the misapplication thereof.

(b) In making the determinations and allocations required by this Section 4.02, the Notes Collateral Agent may conclusively rely upon information supplied by the Trustee as to the amounts of unpaid principal and interest and other amounts outstanding with respect to the Secured Obligations, and the Notes Collateral Agent shall have no liability to any of the Secured Parties for actions taken in reliance on such information, *provided* that nothing in this sentence shall prevent any Grantor from contesting any amounts claimed by any Secured Party in any information so supplied. All distributions made by the Notes Collateral Agent pursuant to this Section 4.02 shall be (subject to any decree of any court of competent jurisdiction) final (absent manifest error), and the Notes Collateral Agent shall have no duty to inquire as to the application by the Trustee of any amounts distributed to it.

ARTICLE V

Indemnity, Subrogation and Subordination

SECTION 5.01. <u>Indemnity</u>. In addition to all such rights of indemnity and subrogation as the Grantors may have under applicable law (but subject to Section 5.03), the Issuer agrees that, in the event any assets of any Grantor shall be sold pursuant to this Agreement or any other Collateral Document relating to the Notes to satisfy in whole or in part an Obligation owed to any Secured Party, the Issuer shall indemnify such Grantor in an amount equal to the greater of the book value or the fair market value of the assets so sold.

SECTION 5.02. Contribution and Subrogation. Each Grantor (a "Contributing Party") agrees (subject to Section 5.03) that, in the event assets of any other Grantor shall be sold pursuant to any Collateral Document relating to the Notes to satisfy any Secured Obligation owed to any Secured Party, and such other Grantor (the "Claiming Party") shall not have been fully indemnified by the Issuer as provided in Section 5.01, the Contributing Party shall indemnify the Claiming Party in an amount equal to the greater of the book value or the fair market value of such assets, in each case multiplied by a fraction of which the numerator shall be the net worth of the Contributing Party on the date hereof and the denominator shall be the aggregate net worth of all the Contributing Parties together with the net worth of the Claiming Party on the date hereof (or, in the case of any Grantor becoming a party hereto pursuant to Section 6.14, the date of the Security Agreement Supplement hereto executed and delivered by such Grantor). Any Contributing Party making any payment to a Claiming Party pursuant to this Section 5.02 shall be subrogated to the rights of such Claiming Party to the extent of such payment.

SECTION 5.03. Subordination.

- (a) Notwithstanding any provision of this Agreement to the contrary, all rights of the Grantors under Sections 5.01 and 5.02 and all other rights of indemnity, contribution or subrogation under applicable law or otherwise shall be fully subordinated to the indefeasible payment in full in cash of the Secured Obligations. No failure on the part of the Issuer or any Grantor to make the payments required by Sections 5.01 and 5.02 (or any other payments required under applicable law or otherwise) shall in any respect limit the obligations and liabilities of any Grantor with respect to its obligations hereunder, and each Grantor shall remain liable for the full amount of the obligations of such Grantor hereunder.
- (b) Each Grantor hereby agrees that upon the occurrence and during the continuance of an Event of Default and after notice from the Notes Collateral Agent all Indebtedness owed by it to any Subsidiary shall be fully subordinated to the indefeasible payment in full in cash of the Secured Obligations.

ARTICLE VI

Miscellaneous

SECTION 6.01. Notices. All communications and notices hereunder, other than with respect to the Notes Collateral Agent, shall (except as otherwise expressly permitted herein) be in writing and given as provided in Section 13.01 of the Indenture. All communications and notices hereunder to any Grantor shall be given to it in care of the Issuer as provided in Section 13.01 of the Indenture. All communications and notices hereunder to the Notes Collateral Agent is duly given if in writing and delivered in person or mailed by first-class mail (registered or certified, return receipt requested), fax or overnight air courier guaranteeing next day delivery, to the Notes Collateral Agent's address:

Citibank, N.A. 390 Greenwich Street New York, NY 10013 Facsimile: 646-308-6528 Telephone: 212-816-5457

Email: peter.t.baumann@citi.com

Additional Email: oploanswebadmin@citigroup.com

Attention: Peter Baumann

SECTION 6.02. Waivers; Amendment.

- (a) No failure or delay by the Notes Collateral Agent or any Secured Party in exercising any right or power hereunder or under any other Notes Document shall operate as a waiver thereof, nor shall any single or partial exercise of any such right or power, or any abandonment or discontinuance of steps to enforce such a right or power, preclude any other or further exercise thereof or the exercise of any other right or power. The rights and remedies of the Notes Collateral Agent and the Secured Parties hereunder and under the other Notes Documents are cumulative and are not exclusive of any rights or remedies that they would otherwise have. No waiver of any provision of this Agreement or consent to any departure by any Grantor therefrom shall in any event be effective unless the same shall be permitted by paragraph (b) of this Section 6.02, and then such waiver or consent shall be effective only in the specific instance and for the purpose for which given. Without limiting the generality of the foregoing, the issuance of any Additional First Lien Debt shall not be construed as a waiver of any Default, regardless of whether the Notes Collateral Agent or any Secured Party may have had notice or knowledge of such Default at the time. No notice or demand on any Grantor in any case shall entitle any Grantor to any other or further notice or demand in similar or other circumstances.
- (b) Subject to the terms of the Intercreditor Agreement and except as otherwise provided in the Indenture, neither this Agreement nor any provision hereof may be waived, amended or modified except pursuant to an agreement or agreements in writing entered into by the Notes Collateral Agent and the Grantor or Grantors with respect to which such waiver, amendment or modification is to apply, subject to any consent required in accordance with Section 9.02 of the Indenture.

SECTION 6.03. Notes Collateral Agent's Fees and Expenses.

(a) The parties hereto agree that the Notes Collateral Agent shall be entitled to reimbursement of its expenses incurred hereunder. Without limitation of its indemnification obligations under the other Notes Documents, the Issuer agrees to indemnify the Notes Collateral Agent and the other Indemnitees against, and hold each Indemnitee harmless from, any and all losses, claims, damages, liabilities and related expenses, including the reasonable fees, charges and disbursements of any counsel for any Indemnitee, incurred by or asserted against any Indemnitee arising out of, in connection with, or as a result of, the execution, delivery or performance of this Agreement or any claim, litigation, investigation or proceeding relating to any of the foregoing agreement or instrument contemplated hereby, or to the Collateral, whether or not any Indemnitee is a party thereto; *provided* that such indemnity shall not, as to any Indemnitee, be available to the extent that such liabilities, obligations, losses, damages, penalties, claims, demands, actions, judgments, suits, costs, expenses or disbursements resulted from the gross negligence or willful misconduct of such Indemnitee or of any Affiliate, director, officer, employee, counsel, agent or attorney-in-fact of such Indemnitee.

(b) Any such amounts payable as provided hereunder shall be additional Secured Obligations secured hereby and by the other Collateral Documents relating to the Notes. The provisions of this Section 6.03 shall remain operative and in full force and effect regardless of the termination of this Agreement or any other Notes Document, the consummation of the transactions contemplated hereby, the repayment of any of the Secured Obligations, the invalidity or unenforceability of any term or provision of this Agreement or any other Notes Document, or any investigation made by or on behalf of the Notes Collateral Agent or any other Secured Party. All amounts due under this Section 6.03 shall be payable within 10 days of written demand therefor.

SECTION 6.04. <u>Successors and Assigns</u>. Whenever in this Agreement any of the parties hereto is referred to, such reference shall be deemed to include the permitted successors and assigns of such party; and all covenants, promises and agreements by or on behalf of any Grantor or the Notes Collateral Agent that are contained in this Agreement shall bind and inure to the benefit of their respective successors and assigns.

SECTION 6.05. <u>Survival of Agreement</u>. All covenants, agreements, representations and warranties made by the Grantors in the Notes Documents and in the certificates or other instruments prepared or delivered in connection with or pursuant to this Agreement or any other Notes Document shall be considered to have been relied upon by the Secured Parties and shall survive the execution and delivery of the Notes Documents and the issuance of any Additional First Lien Debt, regardless of any investigation made by any Secured Party or on its behalf and notwithstanding that the Notes Collateral Agent or any Secured Party may have had notice or knowledge of any Default or incorrect representation or warranty at the time any securities are issued under the Indenture, and shall continue in full force and effect as long as the principal of or any accrued interest on any Note is outstanding and unpaid.

SECTION 6.06. Counterparts; Effectiveness; Several Agreement. This Agreement may be executed in counterparts, each of which shall constitute an original but all of which when taken together shall constitute a single contract. Delivery of an executed signature page to this Agreement by facsimile transmission or other electronic communication shall be as effective as delivery of a manually signed counterpart of this Agreement. This Agreement shall become effective as to any Grantor when a counterpart hereof executed on behalf of such Grantor shall have been delivered to the Notes Collateral Agent and a counterpart hereof shall have been executed on behalf of the Notes Collateral Agent, and thereafter shall be binding upon such Grantor and the Notes Collateral Agent and their respective permitted successors and assigns, and shall inure to the benefit of such Grantor, the Notes Collateral Agent and the other Secured Parties and their respective successors and assigns, except that no Grantor shall have the right to assign or transfer its rights or obligations hereunder or any interest herein or in the Collateral (and any such assignment or transfer shall be void) except as expressly contemplated by this Agreement or the Indenture. This Agreement shall be construed as a separate agreement with respect to each Grantor and may be amended, modified, supplemented, waived or released with respect to any Grantor without the approval of any other Grantor and without affecting the obligations of any other Grantor hereunder.

SECTION 6.07. Severability. Any provision of this Agreement held to be invalid, illegal or unenforceable in any jurisdiction shall, as to such jurisdiction, be ineffective to the extent of such invalidity, illegality or unenforceability without affecting the validity, legality and enforceability of the remaining provisions hereof; and the invalidity of a particular provision in a particular jurisdiction shall not invalidate such provision in any other jurisdiction. The parties shall endeavor in good faith negotiations to replace the invalid, illegal or unenforceable provisions with valid provisions the economic effect of which comes as close as possible to that of the invalid, illegal or unenforceable provisions.

SECTION 6.08. Right of Set-Off. Subject to the terms of the Intercreditor Agreement, in addition to any rights and remedies of the Secured Parties provided by Law, upon the occurrence and during the continuance of any Event of Default, each Secured Party and its Affiliates is authorized at any time and from time to time, without prior notice to the Issuer or any other Grantor, any such notice being waived by the Issuer (on its own behalf and on behalf of each Grantor and its Subsidiaries) to the fullest extent permitted by applicable Law, to set off and apply any and all deposits (general or special, time or demand, provisional or final) at any time held by, and other Indebtedness at any time owing by, such Secured Party and its Affiliates, as the case may be, to or for the credit or the account of the respective Grantors and their Subsidiaries against any and all Secured Obligations owing to such Secured Party and its Affiliates hereunder or under any other Notes Document, now or hereafter existing, irrespective of whether or not such Secured Party or Affiliate shall have made demand under this Agreement or any other Notes Document and although such Secured Obligations may be contingent or unmatured or denominated in a currency different from that of the applicable deposit or Indebtedness. Each Secured Party agrees promptly to notify the Issuer and the Trustee after any such set off and application made by such Secured Party; provided that the failure to give such notice shall not affect the validity of such setoff and application. The rights of the Trustee and each Secured Party under this Section 6.08 are in addition to other rights and remedies (including other rights of setoff) that the Trustee and such Secured Party may have.

SECTION 6.09. Governing Law; Jurisdiction; Consent to Service of Process.

- (a) This Agreement shall be construed in accordance with and governed by the law of the State of New York.
- (b) Each of the Grantors hereby irrevocably and unconditionally submits, for itself and its property, to the exclusive jurisdiction of the Supreme Court of the State of New York sitting in New York City and of the United States District Court of the Southern District of New York, and any appellate court from any thereof, in any action or

proceeding arising out of or relating to this Agreement or any other Notes Document, or for recognition or enforcement of any judgment, and each of the parties hereto hereby irrevocably and unconditionally agrees that all claims in respect of any such action or proceeding may be heard and determined in such New York State or, to the extent permitted by law, in such Federal court. Each of the parties hereto agrees that a final judgment in any such action or proceeding shall be conclusive and may be enforced in other jurisdictions by suit on the judgment or in any other manner provided by law. Nothing in this Agreement or any other Notes Document shall affect any right that the Notes Collateral Agent or any Secured Party may otherwise have to bring any action or proceeding relating to this Agreement or any other Notes Document against any Grantor or its properties in the courts of any jurisdiction.

- (c) Each of the Grantors hereby irrevocably and unconditionally waives, to the fullest extent it may legally and effectively do so, any objection which it may now or hereafter have to the laying of venue of any suit, action or proceeding arising out of or relating to this Agreement or any other Notes Document in any court referred to in paragraph (b) of this Section 6.09. Each of the parties hereto hereby irrevocably waives, to the fullest extent permitted by law, the defense of an inconvenient forum to the maintenance of such action or proceeding in any such court.
- (d) Each party to this Agreement irrevocably consents to service of process in the manner provided for notices in Section 6.01. Nothing in this Agreement or any other Notes Document will affect the right of any party to this Agreement to serve process in any other manner permitted by law.

SECTION 6.10. WAIVER OF JURY TRIAL. EACH PARTY HERETO HEREBY WAIVES, TO THE FULLEST EXTENT PERMITTED BY APPLICABLE LAW, ANY RIGHT IT MAY HAVE TO A TRIAL BY JURY IN ANY LEGAL PROCEEDING DIRECTLY OR INDIRECTLY ARISING OUT OF OR RELATING TO THIS AGREEMENT, ANY OTHER NOTES DOCUMENT OR THE TRANSACTIONS CONTEMPLATED HEREBY (WHETHER BASED ON CONTRACT, TORT OR ANY OTHER THEORY). EACH PARTY HERETO (A) CERTIFIES THAT NO REPRESENTATIVE, AGENT OR ATTORNEY OF ANY OTHER PARTY HAS REPRESENTED, EXPRESSLY OR OTHERWISE, THAT SUCH OTHER PARTY WOULD NOT, IN THE EVENT OF LITIGATION, SEEK TO ENFORCE THE FOREGOING WAIVER AND (B) ACKNOWLEDGES THAT IT AND THE OTHER PARTIES HERETO HAVE BEEN INDUCED TO ENTER INTO THIS AGREEMENT BY, AMONG OTHER THINGS, THE MUTUAL WAIVERS AND CERTIFICATIONS IN THIS SECTION 6.10.

SECTION 6.11. <u>Headings</u>. Article and Section headings and the Table of Contents used herein are for convenience of reference only, are not part of this Agreement and are not to affect the construction of, or to be taken into consideration in interpreting, this Agreement.

SECTION 6.12. Security Interest Absolute. All rights of the Notes Collateral Agent hereunder, the Security Interest, the grant of a security interest in the Pledged Collateral and all obligations of each Grantor hereunder shall be absolute and unconditional irrespective of (a) any lack of validity or enforceability of the Indenture, any other Notes Document, any agreement with respect to any of the Secured Obligations or any other agreement or instrument relating to any of the foregoing, (b) any change in the time, manner or place of payment of, or in any other term of, all or any of the Secured Obligations, or any other amendment or waiver of or any consent to any departure from the Indenture, any other Notes Document or any other agreement or instrument, (c) any exchange, release or non-perfection of any Lien on other collateral, or any release or amendment or waiver of or consent under or departure from any guarantee, securing or guaranteeing all or any of the Secured Obligations or (d) any other circumstance that might otherwise constitute a defense available to, or a discharge of, any Grantor in respect of the Secured Obligations or this Agreement.

SECTION 6.13. Termination or Release.

- (a) This Agreement, the Security Interest and all other security interests granted hereby shall terminate with respect to all Secured Obligations (other than (x) obligations under Secured Hedge Agreements not yet due and payable, (y) Cash Management Obligations not yet due and payable and (z) contingent indemnification obligations not yet accrued and payable) when all the outstanding Secured Obligations have been indefeasibly paid in full.
- (b) A Grantor shall automatically be released from its obligations hereunder and the Security Interest in the Collateral of such Grantor shall be automatically released upon the consummation of any transaction permitted by the Indenture as a result of which such Grantor ceases to be a Subsidiary or is designated as an Unrestricted Subsidiary of Holdings III; *provided* that Holders of more than 50% in principal amount of the total outstanding Notes shall have consented to such transaction (to the extent required by the Indenture) and the terms of such consent did not provide otherwise.
- (c) Upon any sale or other transfer by any Grantor of any Collateral that is permitted under the Indenture, or upon the effectiveness of any written consent to the release of the security interest granted hereby in any Collateral pursuant to Section 11.02 of the Indenture, the security interest of such Grantor in such Collateral shall be automatically released.
- (d) A Grantor (other than Holdings V and the Issuer) shall automatically be released from its obligations hereunder and the Security Interest in the Collateral of such Grantor shall be automatically released if such Grantor ceases to be a Material Domestic Subsidiary.

- (e) If the security interest on any Collateral is released pursuant to Section 2.04 of the Intercreditor Agreement and such release results in the release of the security interest on such Collateral under this Agreement or any Collateral Document relating to the Notes, the security interest on such Collateral granted hereunder or under any such Collateral Document relating to the Notes shall be automatically released.
- (f) In connection with any termination or release pursuant to paragraph (a), (b), (c) or (e) of this Section 6.13, the Notes Collateral Agent shall execute and deliver to any Grantor, at such Grantor's expense, all documents that such Grantor shall reasonably request to evidence such termination or release. Any execution and delivery of documents pursuant to this Section 6.13 shall be without recourse to or warranty by the Notes Collateral Agent.
- (g) In the event that any of the Collateral shall be transferred by any Grantor in connection with the Foreign Reorganization, the security interest granted hereunder on such Collateral shall automatically be discharged and released and all rights to such Collateral shall revert to the applicable Grantor without any further action by the Notes Collateral Agent or any other Person. Without prejudice to the foregoing, upon the request of the applicable Grantor, the Notes Collateral Agent, at the expense of such Grantor, shall promptly execute and deliver to such Grantor, all releases, termination statements, stock certificates, any certificated securities or any other documents necessary or desirable for the release of the security interest on such Collateral.
- (h) Notwithstanding anything to the contrary set forth herein or in any other Notes Document, so long as no Default or Event of Default shall have occurred and be continuing, in the event that the Foreign Reorganization is not consummated and to the extent that any Permitted Intercompany Transfer has occurred (or will occur concurrently with such release described in the Indenture), any security interests granted hereunder by Holdings IV on any Collateral shall automatically be discharged and released without any further action by the Notes Collateral Agent or any other Person. Subject to the terms of the Intercreditor Agreement, in connection with the foregoing, upon the request of the Issuer, the Notes Collateral Agent, at the expense of Issuer, shall promptly execute and deliver to Holdings IV, Holdings V or SigmaTel, as applicable, all releases, termination statements, stock certificates, any certificated securities or any other documents necessary or desirable for the release of the security interest on such Collateral.

SECTION 6.14. Additional Restricted Subsidiaries. Pursuant to Section 11.05 of the Indenture, certain Restricted Subsidiaries of Holdings III that were not in existence or not Secured Guarantors on the date of the Indenture are required to enter in this Agreement as Grantors upon becoming Secured Guarantors. Upon execution and delivery by the Notes Collateral Agent and a Restricted Subsidiary of a Security Agreement Supplement, such Restricted Subsidiary shall become a Grantor hereunder with the same force and effect as if originally named as a Grantor herein. The execution and delivery of any such instrument shall not require the consent of any other Grantor hereunder. The rights and obligations of each Grantor hereunder shall remain in full force and effect notwithstanding the addition of any new Grantor as a party to this Agreement.

SECTION 6.15. Notes Collateral Agent Appointed Attorney-in-Fact. Each Grantor hereby appoints the Notes Collateral Agent the attorney-in-fact of such Grantor for the purpose of carrying out the provisions of this Agreement and taking any action and executing any instrument that the Notes Collateral Agent may deem necessary or advisable to accomplish the purposes hereof at any time after and during the continuance of an Event of Default, which appointment is irrevocable (until termination of the Indenture) and coupled with an interest. Without limiting the generality of the foregoing, the Notes Collateral Agent shall have the right, upon the occurrence and during the continuance of an Event of Default and notice by the Notes Collateral Agent to the Issuer of its intent to exercise such rights, with full power of substitution either in the Notes Collateral Agent's name or in the name of such Grantor (a) to receive, endorse, assign and/or deliver any and all notes, acceptances, checks, drafts, money orders or other evidences of payment relating to the Collateral or any part thereof; (b) to demand, collect, receive payment of, give receipt for and give discharges and releases of all or any of the Collateral; (c) to sign the name of any Grantor on any invoice or bill of lading relating to any of the Collateral; (d) to send verifications of Accounts Receivable to any Account Debtor; (e) to commence and prosecute any and all suits, actions or proceedings at law or in equity in any court of competent jurisdiction to collect or otherwise realize on all or any of the Collateral or to enforce any rights in respect of any Collateral; (f) to settle, compromise, compound, adjust or defend any actions, suits or proceedings relating to all or any of the Collateral; (g) to notify, or to require any Grantor to notify, Account Debtors to make payment directly to the Notes Collateral Agent; and (h) to use, sell, assign, transfer, pledge, make any agreement with respect to or otherwise deal with all or any of the Collateral, and to do all other acts and things necessary to carry out the purposes of this Agreement, as fully and completely as though the Notes Collateral Agent were the absolute owner of the Collateral for all purposes; provided that nothing herein contained shall be construed as requiring or obligating the Notes Collateral Agent to make any commitment or to make any inquiry as to the nature or sufficiency of any payment received by the Notes Collateral Agent, or to present or file any claim or notice, or to take any action with respect to the Collateral or any part thereof or the moneys due or to become due in respect thereof or any property covered thereby. The Notes Collateral Agent and the other Secured Parties shall be accountable only for amounts actually received as a result of the exercise of the powers granted to them herein, and neither they nor their officers, directors, employees or agents shall be responsible to any Grantor for any act or failure to act hereunder, except for their own gross negligence or willful misconduct or that of any of their Affiliates, directors, officers, employees, counsel, agents or attorneys-in-fact.

SECTION 6.16. <u>General Authority of the Notes Collateral Agent</u>. By acceptance of the benefits of this Agreement and any other Collateral Documents relating to the Notes, each Secured Party (whether or not a signatory hereto) shall be deemed irrevocably (a) to consent to the appointment of the Notes Collateral Agent as its agent hereunder and under such other Collateral Documents relating to the Notes, (b) to confirm that the Notes Collateral Agent

shall have the authority to act as the exclusive agent of such Secured Party for the enforcement of any provisions of this Agreement and such other Collateral Documents relating to the Notes against any Grantor, the exercise of remedies hereunder or thereunder and the giving or withholding of any consent or approval hereunder or thereunder relating to any Collateral or any Grantor's obligations with respect thereto, (c) to agree that it shall not take any action to enforce any provisions of this Agreement or any other Collateral Document relating to the Notes against any Grantor, to exercise any remedy hereunder or thereunder or to give any consents or approvals hereunder or thereunder except as expressly provided in this Agreement or any other Collateral Document relating to the Notes and (d) to agree to be bound by the terms of this Agreement and any other Collateral Documents relating to the Notes.

IN WITNESS WHEREOF, the parties hereto have duly executed this Agreement as of the day and year first above written.

FREESCALE SEMICONDUCTOR, INC.

By: /s/ Steven P. Goel

Name: Steven P. Goel

Title: Vice President and Treasurer

FREESCALE SEMICONDUCTOR HOLDINGS V, INC.

By: /s/ Steven P. Goel

Name: Steven P. Goel Title: Treasurer

FREESCALE SEMICONDUCTOR HOLDINGS IV, LTD.

By: /s/ Steven P. Goel

Name: Steven P. Goel Title: Treasurer

SIGMATEL, LLC

By: Freescale Semiconductor, Inc. as Sole Member

By: /s/ Steven P. Goel

Name: Steven P. Goel Title: Treasurer

[Security Agreement]

CITIBANK, N.A., as Notes Collateral Agent

By: /s/ Matthew Burke

Name: Matthew Burke Title: Vice President

[Security Agreement]

Pledged Equity

| Issuer | Number of Certificate | Registered Owner | Number and Class of Equity Interests | Percentage of Equity Interests |
|--|--------------------------|-------------------------|--|--------------------------------------|
| Freescale Semiconductor Holdings V, Inc. | 3 | Freescale Semiconductor | 491,282.86 | |
| | | Holdings IV, Ltd. | shares of | |
| | | | Common | |
| | | | Stock, \$0.01 | |
| | | | par value | |
| | | | per share | 100% |
| Freescale Semiconductor, Inc. | 1 | Freescale Semiconductor | 1,000 shares of | |
| | | Holdings V, Inc. (f/k/a | Common Stock, \$0.01 | |
| | | Freescale Acquisition | par value per share | |
| | | Holdings Corp.) | | 100% |
| SigmaTel, LLC | Uncertificated | Freescale | All limited liability | |
| | | Semiconductor, Inc. | company interests | 100% |

Pledged Debt

Debt Instruments

| | | Amount | | |
|---|-----------|------------------|----------------|--------------|
| <u>Lender</u> | Borrower | Outstanding | Facility Start | Facility End |
| Freescale Semiconductor Holdings IV, Ltd. | Freescale | | | |
| | Cayman | | | |
| | Holdings, | | | |
| | Ltd. | \$116,834,105.13 | 4/27/2013 | 4/27/2014 |

Schedule I-1

COMMERCIAL TORT CLAIMS

None.

Schedule II-1

EXHIBIT I TO THE SECURITY AGREEMENT

SUPPLEMENT NO. dated as of [], to the Security Agreement dated as of November 1, 2013, among FREESCALE SEMICONDUCTOR, INC., a Delaware corporation (the "Issuer"), FREESCALE SEMICONDUCTOR HOLDINGS V, INC., a Delaware corporation ("Holdings V"), FREESCALE SEMICONDUCTOR HOLDINGS IV, LTD. ("Holdings IV"), a Bermuda exempted limited liability company, SIGMATEL, LLC, a Delaware limited liability company ("SigmaTel"), the subsidiaries of Freescale Semiconductor Holdings, III, Ltd. ("Holdings III") from time to time party thereto and CITIBANK, N.A., as collateral agent for the Secured Parties (as defined below) (in such capacity, the "Notes Collateral Agent").

- A. Reference is made to the Indenture dated as of November 1, 2013 (as amended, supplemented or otherwise modified from time to time, the "Indenture"), among the Issuer, Holdings V, Holdings IV, Holdings III, Freescale Semiconductor Holdings II, Ltd., Freescale Semiconductor, Ltd., SigmaTel and Wells Fargo Bank, National Association, as trustee (the "Trustee").
- B. Capitalized terms used herein and not otherwise defined herein shall have the meanings assigned to such terms in the Indenture and the Security Agreement referred to therein.
- C. The Grantors have entered into the Security Agreement in order to induce the Holders to purchase the Notes and the Trustee to enter into the Indenture. Section 6.14 of the Security Agreement provides that additional Restricted Subsidiaries of Holdings III may become Grantors under the Security Agreement by execution and delivery of an instrument in the form of this Supplement. The undersigned Restricted Subsidiary (the "New Subsidiary") is executing this Supplement in accordance with the requirements of Indenture to become a Grantor under the Security Agreement.

Accordingly, the Notes Collateral Agent and the New Subsidiary agree as follows:

SECTION 1. In accordance with Section 6.14 of the Collateral Agreement, the New Subsidiary by its signature below becomes a Grantor under the Security Agreement with the same force and effect as if originally named therein as a Grantor and the New Subsidiary hereby (a) agrees to all the terms and provisions of the Security Agreement applicable to it as a Grantor thereunder and (b) represents and warrants that the representations and warranties made by it as a Grantor thereunder are true and correct on and as of the date hereof. In furtherance of the foregoing, the New Subsidiary, as security for the payment and performance in full of the Secured Obligations does hereby create and grant to the Notes Collateral Agent, its successors and assigns, for the benefit of the Secured Parties, their successors and assigns, a security interest in and lien on all of the New Subsidiary's right, title and interest in and to the Collateral (as defined in the Security Agreement) of the New Subsidiary. Each reference to a "Grantor" in the Security Agreement shall be deemed to include the New Subsidiary. The Security Agreement is hereby incorporated herein by reference.

Exhibit I-1

SECTION 2. The New Subsidiary represents and warrants to the Notes Collateral Agent and the other Secured Parties that this Supplement has been duly authorized, executed and delivered by it and constitutes its legal, valid and binding obligation, enforceable against it in accordance with its terms, except as such enforceability may be limited by Debtor Relief Laws and by general principles of equity.

SECTION 3. This Supplement may be executed in counterparts (and by different parties hereto on different counterparts), each of which shall constitute an original, but all of which when taken together shall constitute a single contract. This Supplement shall become effective when the Notes Collateral Agent shall have received a counterpart of this Supplement that bears the signature of the New Subsidiary, and the Notes Collateral Agent has executed a counterpart hereof. Delivery of an executed signature page to this Supplement by facsimile transmission or other electronic communication shall be as effective as delivery of a manually signed counterpart of this Supplement.

SECTION 4. The New Subsidiary hereby represents and warrants that (a) set forth on Schedule I attached hereto is a true and correct schedule of the location of any and all Collateral of the New Subsidiary and (b) set forth under its signature hereto is the true and correct legal name of the New Subsidiary, its jurisdiction of formation and the location of its chief executive office.

SECTION 5. Except as expressly supplemented hereby, the Security Agreement shall remain in full force and effect.

SECTION 6. THIS SUPPLEMENT SHALL BE GOVERNED BY, AND CONSTRUED IN ACCORDANCE WITH, THE LAWS OF THE STATE OF NEW YORK.

SECTION 7. In case any one or more of the provisions contained in this Supplement should be held invalid, illegal or unenforceable in any respect, the validity, legality and enforceability of the remaining provisions contained herein and in the Security Agreement shall not in any way be affected or impaired thereby (it being understood that the invalidity of a particular provision in a particular jurisdiction shall not in and of itself affect the validity of such provision in any other jurisdiction). The parties hereto shall endeavor in good-faith negotiations to replace the invalid, illegal or unenforceable provisions with valid provisions the economic effect of which comes as close as possible to that of the invalid, illegal or unenforceable provisions.

SECTION 8. All communications and notices hereunder shall be in writing and given as provided in Section 6.01 of the Security Agreement.

SECTION 9. The New Subsidiary agrees to reimburse the Notes Collateral Agent for its reasonable out-of-pocket expenses in connection with this Supplement, including the reasonable fees, other charges and disbursements of counsel for the Notes Collateral Agent.

Exhibit I-2

| IN WITNESS WHEREOF, the New Subsidiary and the Notes of the day and year first above written. | Collateral Agent have duly executed this Supplement to the Security Agreement as |
|---|--|
| | [NAME OF NEW SUBSIDIARY] |
| | By: |
| | Name: |
| | Title: |
| | Jurisdiction of Formation: |
| | Address Of Chief Executive Office: |
| | CITIBANK, N.A., as Notes Collateral Agent |

By:

Name: Title:

Exhibit I-3

SCHEDULE I TO SUPPLEMENT NO TO THE SECURITY AGREEMENT

LOCATION OF COLLATERAL

<u>Description</u> <u>Location</u>

EQUITY INTERESTS

Number of Number of Certificate Number of Owner Number of Equity Interests Equity Interests

DEBT SECURITIES

<u>Issuer</u> <u>Principal Amount</u> <u>Date of Note</u> <u>Maturity Date</u>

Schedule I-1

Exhibit II to the Security Agreement

FORM OF PERFECTION CERTIFICATE

Exhibit II-1

PERFECTION CERTIFICATE

[•], 2013

Reference is made to the Indenture (as amended, supplemented or otherwise modified from time to time, the "Indenture") dated as of November 1, 2013, among Freescale Semiconductor, Inc., as issuer ("Freescale"), SigmaTel, LLC ("SigmaTel"), Freescale Semiconductor Holdings V, Inc. ("Holdings"), Freescale Semiconductor Holdings IV, Ltd., ("Foreign Holdings"), Freescale Semiconductor Holdings III, Ltd. ("Parent" and, together with Freescale, SigmaTel, Holdings and Foreign Holdings, the "Grantors"), Freescale Semiconductor Holdings II, Ltd. and Freescale Semiconductor, Ltd., as guarantors, and Wells Fargo Bank, National Association, as trustee. Capitalized terms used but not defined herein have the meanings set forth in either the Indenture or the Security Agreement referred to therein, as applicable.

The undersigned Responsible Officers of each of the Grantors hereby certify to the Notes Collateral Agent and each other Secured Party as follows:

1. <u>Names.</u> (a) The exact legal name of each Grantor, as such name appears in its respective certificate of incorporation or certificate of formation, as applicable, is as follows:

Exact Legal Name of Each Grantor

Other Legal Name in Past 5

Date of Name

(b) Set forth below is each other legal name each Grantor has had in the past five years, together with the date of the relevant change:

Grantor
Years
Change

(c) Except as set forth in Schedule 1 hereto, no Grantor has changed its identity or corporate structure in any way within the past five years. Changes in

(c) Except as set forth in Schedule 1 hereto, no Grantor has changed its identity or corporate structure in any way within the past five years. Changes in identity or corporate structure would include mergers, consolidations and acquisitions, as well as any change in the form, nature or jurisdiction of organization. If any such change has occurred, include in Schedule 1 the information required by Sections 1 and 2 of this certificate as to each acquiree or constituent party to a merger or consolidation.

(d) Set forth below is the Organizational Identification Number, if any, issued by the jurisdiction of formation of each Grantor that is a registered organization:

Grantor Organizational Identification Number

2. <u>Current Locations.</u> (a) The chief executive office of each Grantor is located at the address set forth opposite its name below:

Grantor Mailing Address County State

(b) The jurisdiction of formation of each Grantor that is a registered organization is set forth opposite its name below:

<u>Grantor</u> <u>Jurisdiction</u>

(c) Set forth below is a list of all domestic real property owned by each Grantor, the name of the Grantor that owns said property and the book value apportioned to each site:

| <u>Address</u> | Entity | of Real Estate at 9/27/13 | Net Book Value of Equipment at 9/27/13 |
|----------------|--------|--|--|
| Address | Entity | Net Book Value of Real Estate at 9/27/13 | Net Book Value of |

- (d) Attached hereto as Schedule 2 is a schedule setting forth opposite the name of each Grantor are the names and locations of all Persons other than such Grantor that have possession of any of the Collateral of such Grantor, in each case in an amount exceeding \$1,000,000:
- 3. <u>Unusual Transactions.</u> All Accounts have been originated by the Grantors and all Inventory has been acquired by the Grantors in the ordinary course of business.
- 4. <u>File Search Reports.</u> File search reports have been obtained from each Uniform Commercial Code filing office identified with respect to such Grantor in Section 6 hereof, and such search reports reflect no liens against any of the Collateral other than those permitted under the Indenture.

- 5. <u>UCC Filings</u>. Financing statements in substantially the form of Schedule 5 hereto have been prepared for filing in the proper Uniform Commercial Code filing office in the jurisdiction in which each Grantor is located.
- 6. <u>Schedule of Filings</u>. Attached hereto as Schedule 6 is a schedule setting forth, with respect to the filings described in Section 5 above, each filing and the filing office in which such filing is to be made.
- 7. Stock Ownership and other Equity Interests. Attached hereto as Schedule 7 is a true and correct list of all the issued and outstanding stock, partnership interests, limited liability company membership interests or other Equity Interests held by, directly or indirectly, any Grantor and the record and beneficial owners of such stock, partnership interests, membership interests or other Equity Interests. Also set forth on Schedule 7 is each equity investment held by, directly or indirectly, any Grantor that represents 50% or less of the Equity Interests of the entity in which such investment was made.
- 8. <u>Debt Instruments.</u> Attached hereto as Schedule 8 is a true and correct list of all promissory notes and other evidence of indebtedness held by any Grantor that are required to be pledged under the Security Agreement, including all intercompany notes held by any Grantor.
- 9. <u>Assignment of Claims Act.</u> Attached hereto as Schedule 9 is a true and correct list of all written contracts between the Borrower or any Material Domestic Subsidiary and the United States government or any department or agency thereof that have a remaining value of at least \$5,000,000, setting forth the contract number, name and address of contracting officer (or other party to whom a notice of assignment under the Assignment of Claims Act should be sent), contract start date and end date, agency with which the contract was entered into, and a description of the contract type.
- 10. <u>Advances.</u> Attached hereto as Schedule 10 is (a) a true and correct list of all advances made by any Grantor to any Subsidiary of Parent who is not a Grantor (other than those identified on Schedule 8), which advances will be on and after the date hereof evidenced by one or more intercompany notes pledged to the Notes Collateral Agent under the Security Agreement and (b) a true and correct list of all unpaid intercompany transfers of goods sold and delivered by any Grantor to any Subsidiary of Parent who is not a Grantor.
- 11. <u>Mortgage Filings.</u> Attached hereto as Schedule 11 is a schedule setting forth, with respect to each Material Real Property, (a) the exact name of the person that owns such property as such name appears in its certificate of incorporation or other organizational document, (b) if different from the name identified pursuant to clause (a), the exact name of the current record owner of such property reflected in the records of the filing office for such property identified pursuant to the following clause and (c) the filing office in which a mortgage with respect to such Material Real Property must be filed or recorded in order for the Notes Collateral Agent to obtain a perfected security interest therein.

- 12. <u>Intellectual Property.</u> Attached hereto as Schedule 12A in proper form for filing with the United States Patent and Trademark Office is a schedule setting forth all of each Grantor's Patents and Trademarks, including the name of the registered owner and the registration number of each Patent and Trademark owned by any Grantor. Attached hereto as Schedule 12B in proper form for filing with the United States Copyright Office is a schedule setting forth all of each Grantor's Copyrights, including the name of the registered owner and the registration number of each Copyright owned by any Grantor.
- 13. <u>Commercial Tort Claims</u>. Attached hereto as Schedule 13 is a true and correct list of commercial tort claims in excess of \$5,000,000 held by any Grantor, including a brief description thereof.

IN WITNESS WHEREOF, the undersigned have duly executed this certificate on the date first written above.

| | By: |
|-----|--|
| | Name: |
| | Title: |
| | Title. |
| | FREESCALE SEMICONDUCTOR HOLDINGS V, INC. |
| | By: |
| | Name: |
| | Title: |
| | |
| | FREESCALE SEMICONDUCTOR HOLDINGS IV, LTD. |
| | By: |
| | Name: |
| | Title: |
| | FREESCALE SEMICONDUCTOR HOLDINGS III, LTD. |
| | By: |
| | Name: |
| | Title: |
| | SIGMATEL, LLC |
| | By: Freescale Semiconductor, Inc., |
| | as Sole Member |
| | as soic Member |
| | By: |
| | Name: |
| | Title: |
| | |
| 6 6 | |

FREESCALE SEMICONDUCTOR, INC.

[Perfection Certificate]

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SCHEDULE 12A

Patents, Patent Licenses, Trademarks and Trademark Licenses

Sched. 12B-1

SCHEDULE 12B

Copyrights and Copyright Licenses

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Commercial Tort Claims

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INTELLECTUAL PROPERTY SECURITY AGREEMENT

dated as of

November 1, 2013

among

FREESCALE SEMICONDUCTOR, INC., as Issuer

FREESCALE SEMICONDUCTOR HOLDINGS V, INC,

SIGMATEL, LLC

and

CITIBANK, N.A., as Notes Collateral Agent

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NOTWITHSTANDING ANYTHING HEREIN TO THE CONTRARY, THE EXERCISE OF ANY RIGHT OR REMEDY BY THE NOTES COLLATERAL AGENT WITH RESPECT TO THE LIENS, SECURITY INTERESTS AND RIGHTS GRANTED PURSUANT TO THIS AGREEMENT OR ANY OTHER COLLATERAL DOCUMENT RELATING TO THE NOTES SHALL BE AS SET FORTH IN, AND SUBJECT TO THE TERMS AND CONDITIONS OF (AND THE EXERCISE OF ANY RIGHT OR REMEDY BY THE NOTES COLLATERAL AGENT HEREUNDER OR THEREUNDER SHALL BE SUBJECT TO THE TERMS AND CONDITIONS OF), THE FIRST LIEN INTERCREDITOR AGREEMENT, DATED AS OF FEBRUARY 19, 2010 (AS AMENDED, AMENDED AND RESTATED, SUPPLEMENTED OR OTHERWISE MODIFIED FROM TIME TO TIME, THE "INTERCREDITOR AGREEMENT"), AMONG CITIBANK, N.A., AS DIRECTING AGENT; CITIBANK, N.A., AS THE SENIOR CREDIT AGREEMENT COLLATERAL AGENT; CITIBANK, N.A., AS THE SENIOR CREDIT AGREEMENT INCREMENTAL COLLATERAL AGENT; CITIBANK, N.A., AS THE INITIAL ADDITIONAL FIRST LIEN REPRESENTATIVE; AND EACH ADDITIONAL AUTHORIZED REPRESENTATIVE FROM TIME TO TIME PARTY THERETO (IN EACH CASE, AS DEFINED IN THE INTERCREDITOR AGREEMENT), AS CONSENTED TO BY THE GRANTORS HEREUNDER FROM TIME TO TIME. WITH THE EXCEPTION OF SECTION 2.01 HEREOF, IN THE EVENT OF ANY CONFLICT BETWEEN THIS AGREEMENT OR ANY OTHER COLLATERAL DOCUMENT RELATING TO THE NOTES AND THE INTERCREDITOR AGREEMENT, THE INTERCREDITOR AGREEMENT SHALL CONTROL.

INTELLECTUAL PROPERTY SECURITY AGREEMENT, dated as of November 1, 2013, among FREESCALE SEMICONDUCTOR, INC., a Delaware corporation (the "Issuer"), FREESCALE SEMICONDUCTOR HOLDINGS V, INC., a Delaware corporation ("Holdings V"), SIGMATEL, LLC, a Delaware limited liability company ("SigmaTel"), the Subsidiaries of FREESCALE SEMICONDUCTOR HOLDINGS III, LTD. ("Holdings III") from time to time party hereto and CITIBANK, N.A., as collateral agent for the Secured Parties (as defined below) (in such capacity, the "Notes Collateral Agent").

Reference is made to the Indenture dated as of November 1, 2013 (as amended, supplemented or otherwise modified from time to time, the **"Indenture"**), among the Issuer, Holdings V, SigmaTel, the other Guarantors named therein and Wells Fargo Bank, National Association, as trustee (the **"Trustee"**), pursuant to which the Issuer has issued \$960,000,000 aggregate principal amount of 6.000% Senior Secured Notes due 2022 (the **"Notes"**) to the holders thereof (the **"Holders"**). The obligations of the initial Holders to purchase the Notes are conditioned upon, among other things, the execution and delivery of this Agreement. Each of the Issuer, Holdings V and SigmaTel will derive substantial benefits from the execution, delivery and performance of the obligations under the Indenture and the Collateral Documents relating to the Notes and each is, therefore, willing to enter into this Agreement. Accordingly, the parties hereto agree as follows:

ARTICLE I

DEFINITIONS

SECTION 1.01. Indenture.

- (a) Capitalized terms used in this Agreement and not otherwise defined herein have the meanings specified in the Indenture. All terms defined in the New York UCC (as defined herein) and not defined in this Agreement have the meanings specified therein; the term "instrument" shall have the meaning specified in Article 9 of the New York UCC.
 - (b) The rules of construction specified in Section 1.03 of the Indenture also apply to this Agreement.
 - SECTION 1.02. Other Defined Terms. As used in this Agreement, the following terms have the meanings specified below:
 - "Agreement" means this Intellectual Property Security Agreement.
 - "Claiming Party" has the meaning assigned to such term in Section 4.02.
 - "Collateral" has the meaning assigned to such term in Section 2.01.
- "Collateral Documents" means collectively, the Senior Credit Agreement Collateral Documents, the Additional First Lien Debt Collateral Documents and the Intercreditor Agreement.
 - "Contributing Party" has the meaning assigned to such term in Section 4.02.
- "Copyright License" means any written agreement, now or hereafter in effect, granting any right to any third party under any copyright now or hereafter owned by any Grantor or that such Grantor otherwise has the right to license, or granting any right to any Grantor under any copyright now or hereafter owned by any third party, and all rights of such Grantor under any such agreement.
- "Copyrights" means all of the following now owned or hereafter acquired by any Grantor: (a) all copyright rights in any work subject to the copyright laws of the United States or any other country, whether as author, assignee, transferee or otherwise, and (b) all registrations and applications for registration of any such copyright in the United States or any other country, including registrations, recordings, supplemental registrations and pending applications for registration in the United States Copyright Office, including those listed on Schedule I.
 - "Grantor" means each of Holdings V, the Issuer, SigmaTel and each other Restricted Subsidiary that is a Material Domestic Subsidiary.
 - "Holders" has the meaning assigned to such term in the preliminary statement of this Agreement.

- "Holdings III" has the meaning assigned to such term in the preliminary statement of this Agreement.
- "Holdings V" has the meaning assigned to such term in the preliminary statement of this Agreement.
- "Indemnitee" means the Notes Collateral Agent, together with its Affiliates, and the officers, directors, employees, agents and attorneys-in-fact of the Notes Collateral Agent and Affiliates.
 - "Indenture" has the meaning assigned to such term in the preliminary statement of this Agreement.
- "Intellectual Property" means all intellectual and similar property of every kind and nature now owned or hereafter acquired by any Grantor, including inventions, designs, Patents, Copyrights, Licenses, Trademarks, trade secrets, confidential or proprietary technical and business information, know-how, show-how or other data or information, the intellectual property rights in software and databases and related documentation, and all additions, improvements and accessions to, and books and records describing any of the foregoing.
 - "Intellectual Property Security Agreement Supplement" means an instrument in the form of Exhibit I hereto.
 - "Intercreditor Agreement" has the meaning assigned to such term in the preliminary statement of this Agreement.
 - "Issuer" has the meaning assigned to such term in the preliminary statement of this Agreement.
- **"License"** means any Patent License, Trademark License, Copyright License or other Intellectual Property license or sublicense agreement to which any Grantor is a party.
 - "New York UCC" means the Uniform Commercial Code as from time to time in effect in the State of New York.
 - "Notes" has the meaning assigned to such term in the preliminary statement of this Agreement.
 - "Notes Collateral Agent" has the meaning assigned to such term in the preliminary statement of this Agreement.
 - "Notes Documents" means the Indenture, the Notes and the Collateral Documents relating to the Notes.
 - "Obligations" has the meaning assigned to such term in the Indenture.

"Patent License" means any written agreement, now or hereafter in effect, granting to any third party any right to make, use or sell any invention on which a patent, now or hereafter owned by any Grantor or that any Grantor otherwise has the right to license, is in existence, or granting to any Grantor any right to make, use or sell any invention on which a patent, now or hereafter owned by any third party, is in existence, and all rights of any Grantor under any such agreement.

"Patents" means all of the following now owned or hereafter acquired by any Grantor: (a) all letters patent of the United States or the equivalent thereof in any other country, all registrations and recordings thereof, and all applications for letters patent of the United States or the equivalent thereof in any other country, including registrations, recordings and pending applications in the United States Patent and Trademark Office or any similar offices in any other country, including those listed on Schedule I, and (b) all reissues, continuations, divisions, continuations-in-part, renewals or extensions thereof, and the inventions disclosed or claimed therein, including the right to make, use and/or sell the inventions disclosed or claimed therein.

"Perfection Certificate" means a certificate substantially in the form of Exhibit II to the Security Agreement, completed and supplemented with the schedules and attachments contemplated thereby, and duly executed by the chief financial officer and the chief legal officer of each of Holdings III, Holdings IV, Holdings V, SigmaTel and the Issuer.

- "Proceeds" has the meaning specified in Section 9-102 of the New York UCC.
- "Secured Parties" means, collectively, the Notes Collateral Agent, the Holders and the Trustee to the Indenture.
- "Security Interest" has the meaning assigned to such term in Section 2.01(a).
- "SigmaTel" has the meaning assigned to such term in the preliminary statement of this Agreement.

"Trademark License" means any written agreement, now or hereafter in effect, granting to any third party any right to use any trademark now or hereafter owned by any Grantor or that any Grantor otherwise has the right to license, or granting to any Grantor any right to use any trademark now or hereafter owned by any third party, and all rights of any Grantor under any such agreement.

"Trademarks" means all of the following now owned or hereafter acquired by any Grantor: (a) all trademarks, service marks, trade names, corporate names, company names, business names, fictitious business names, trade styles, trade dress, logos, other source or business identifiers, designs and general intangibles of like nature, now existing or hereafter adopted or acquired, all registrations and recordings thereof, and all registration and recording applications filed in connection therewith, including registrations and registration applications in the United States Patent and Trademark Office or any similar offices in any State of the United States or any other country or any political subdivision thereof, and all extensions or renewals thereof, including those listed on Schedule I, (b) all goodwill connected with the use of and symbolized thereby and (c) all other assets, rights and interests that uniquely reflect or embody such goodwill.

ARTICLE II

SECURITY INTERESTS

SECTION 2.01. Security Interest. (a) As security for the payment or performance, as the case may be, in full of the Obligations, including the Guarantees, each Grantor hereby assigns and pledges to the Notes Collateral Agent, its successors and assigns, for the benefit of the Secured Parties, and hereby grants to the Notes Collateral Agent, its successors and assigns, for the benefit of the Secured Parties, a security interest (the "Security Interest") in all right, title or interest in or to any and all of the following assets and properties now owned or at any time hereafter acquired by such Grantor or in which such Grantor now has or at any time in the future may acquire any right, title or interest (collectively, the "Collateral"):

- (i) all Copyrights;
- (ii) all Patents:
- (iii) all Trademarks;
- (iv) all Licenses;
- (v) all other Intellectual Property; and
- (vi) all Proceeds and products of any and all of the foregoing and all collateral security and guarantees given by any Person with respect to any of the foregoing.

provided, however, that notwithstanding any of the other provisions herein (and notwithstanding any recording of the Notes Collateral Agent's Lien made in the U.S. Patent and Trademark Office, U.S. Copyright Office, or other IP registry office), this Agreement shall not constitute a grant of a security interest in any property to the extent that such grant of a security interest is prohibited by any rule of law, statute or regulation or is prohibited by, or constitutes a breach or default under or results in the termination of any contract, license, agreement, instrument or other document evidencing or giving rise to such property, or would result in the forfeiture of the Grantors' rights in the property including, without limitation, any Trademark applications filed in the United States Patent and Trademark Office on the basis of such Grantor's "intent-to-use" such trademark, unless and until acceptable evidence of use of the Trademark has been filed with the United States Patent and Trademark Office pursuant to Section 1(c) or Section 1(d) of the Lanham Act (15 U.S.C. 1051, et seq.), to the extent that granting a lien in such Trademark application prior to such filing would adversely affect the enforceability or validity of such Trademark application.

(b) Each Grantor hereby irrevocably authorizes the Notes Collateral Agent for the benefit of the Secured Parties at any time and from time to time to file in any relevant jurisdiction any initial financing statements with respect to the Collateral or any part thereof and amendments thereto that contain the information required by Article 9 of the Uniform

Commercial Code or the analogous legislation of each applicable jurisdiction for the filing of any financing statement or amendment, including whether such Grantor is an organization, the type of organization and any organizational identification number issued to such Grantor. Each Grantor agrees to provide such information to the Notes Collateral Agent promptly upon request.

The Notes Collateral Agent is further authorized to file with the United States Patent and Trademark Office or United States Copyright Office (or any successor office or any similar office in any other country) such documents as may be necessary or advisable for the purpose of perfecting, confirming, continuing, enforcing or protecting the Security Interest granted by each Grantor, without the signature of any Grantor, and naming any Grantor or the Grantors as debtors and the Notes Collateral Agent as secured party.

(c) The Security Interest is granted as security only and shall not subject the Notes Collateral Agent or any other Secured Party to, or in any way alter or modify, any obligation or liability of any Grantor with respect to or arising out of the Collateral.

SECTION 2.02. *Representations and Warranties*. Holdings V, the Issuer and SigmaTel jointly and severally represent and warrant, as to themselves and the other Grantors, to the Notes Collateral Agent and the other Secured Parties that:

- (a) Except as would not be expected to have a Material Adverse Effect, each Grantor has good and valid rights in and title to (or with respect to the Patents set forth on Schedule II hereto, a joint ownership interest in) the Collateral with respect to which it has purported to grant a Security Interest hereunder and has full power and authority to grant to the Notes Collateral Agent the Security Interest in such Collateral pursuant hereto and to execute, deliver and perform its obligations in accordance with the terms of this Agreement, without the consent or approval of any other Person other than any consent or approval that has been obtained.
 - (i) The Perfection Certificate has been duly prepared, completed and executed and the information set forth therein, including the exact legal name of each Grantor, is correct and complete in all material respects as of the Closing Date.
 - (ii) The Uniform Commercial Code financing statements (including fixture filings, as applicable) or other appropriate filings, recordings or registrations prepared by the Notes Collateral Agent based upon the information provided to the Notes Collateral Agent in the Perfection Certificate for filing in each governmental, municipal or other office specified in Schedule 6 to the Perfection Certificate (or specified by notice from the Issuer to the Notes Collateral Agent after the Closing Date in the case of filings, recordings or registrations required by the Indenture), are all the filings, recordings and registrations (other than filings required to be made in the United States Patent and Trademark Office and the United States Copyright Office in order to perfect the Security Interest in Collateral consisting of United States Patents, Trademarks and Copyrights) that are necessary to establish a valid and perfected security interest in favor of the Notes Collateral Agent (for the benefit of the Secured Parties) in respect of all Collateral in which the Security Interest may be perfected by filing, recording or registration in the United States (or any political subdivision thereof) and its territories and possessions, and no further or subsequent filing, refiling, recording, rerecording, registration or reregistration is necessary in any such jurisdiction, except as provided under applicable law with respect to the filing of continuation statements.

(iii) Each Grantor represents and warrants that a fully executed agreement in the form hereof and containing a description of all Collateral consisting of United States Patents and United States registered Trademarks (and Trademarks for which United States registration applications are pending) and United States registered Copyrights have been delivered to the Notes Collateral Agent for recording by the United States Patent and Trademark Office and the United States Copyright Office pursuant to 35 U.S.C. § 261, 15 U.S.C. § 1060 or 17 U.S.C. § 205 and the regulations thereunder, as applicable, and otherwise as may be required pursuant to the laws of any other necessary jurisdiction, to establish a valid and perfected security interest in favor of the Notes Collateral Agent (for the benefit of the Secured Parties) in respect of all Collateral consisting of Patents, Trademarks and Copyrights in which a security interest may be perfected by filing, recording or registration in the United States (or any political subdivision thereof) and its territories and possessions under the Federal intellectual property laws, and no further or subsequent filing, refiling, recording, rerecording, registration or reregistration is necessary (other than such filings and actions as are necessary to perfect the Security Interest with respect to (i) any Collateral consisting of Patents, Trademarks and Copyrights (or registration or application for registration thereof) acquired or developed by any Grantor after the date hereof), (ii) as may be required under the laws of jurisdictions outside the United States with respect to Collateral created under such laws, and (iii) the Uniform Commercial Code financing and continuation statements contemplated in subsection (i) of this Section 2.02(a).

(b) The Security Interest constitutes (i) a valid security interest in all the Collateral securing the payment and performance of the Obligations, (ii) subject to the filings described in Section 2.02(b), a perfected security interest in all Collateral in which a security interest may be perfected by filing, recording or registering a financing statement or analogous document in the United States (or any political subdivision thereof) and its territories and possessions pursuant to the Uniform Commercial Code and (iii) a security interest that shall be perfected in all Collateral in which a security interest may be perfected upon the receipt and recording of this Agreement (or a fully executed short form agreement in form and substance reasonably satisfactory to the Notes Collateral Agent and the Issuer) with the United States Patent and Trademark Office and the United States Copyright Office, as applicable, within the three-month period (commencing as of the date hereof) pursuant to 35 U.S.C. § 261 or 15 U.S.C. § 1060 or the one-month period (commencing as of the date hereof) pursuant to 17 U.S.C. § 205 and otherwise as may be required pursuant to the laws of any other necessary jurisdiction. The Security Interest is and shall be prior to any other Lien on any of the Collateral, other than (i) any nonconsensual Lien that is expressly permitted pursuant to Section 4.12 of the Indenture.

(c) The Collateral, which is purported to be owned in whole or in part by the Grantors, is owned by the Grantors free and clear of any Lien, except for Liens expressly permitted pursuant to Section 4.12 of the Indenture. None of the Grantors has filed or consented to the filing of (i) any financing statement or analogous document under the Uniform Commercial Code or any other applicable laws covering any Collateral, (ii) any assignment in which any Grantor assigns any Collateral or any security agreement or similar instrument covering any Collateral with the United States Patent and Trademark Office or the United States Copyright Office or (iii) any assignment in which any Grantor assigns any Collateral or any security agreement or similar instrument covering any Collateral with any foreign governmental, municipal or other office, which financing statement or analogous document, assignment, security agreement or similar instrument is still in effect, except, in each case, for Liens expressly permitted pursuant to Section 4.12 of the Indenture and Liens that are no longer effective.

SECTION 2.03. Covenants.

- (a) The Issuer agrees promptly to notify the Notes Collateral Agent in writing of any change (i) in legal name of any Grantor, (ii) in the identity or type of organization or corporate structure of any Grantor, or (iii) in the jurisdiction of organization of any Grantor.
- (b) Each Grantor shall, at its own expense, take any and all commercially reasonable actions necessary to defend title to the Collateral against all Persons and to defend the Security Interest of the Notes Collateral Agent in the Collateral and the priority thereof against any Lien not expressly permitted pursuant to Section 4.12 of the Indenture.
- (c) Each year, at the time of delivery of annual financial statements with respect to the preceding fiscal year pursuant to Section 4.03 of the Indenture, the Issuer shall deliver to the Notes Collateral Agent a certificate executed by the chief financial officer and the chief legal officer of the Issuer setting forth the information required pursuant to Sections 1(a), 1(c), 1(d), 2(b) and 12 of the Perfection Certificate or confirming that there has been no change in such information since the date of such certificate or the date of the most recent certificate delivered pursuant to this Section 2.03(c).
- (d) The Issuer agrees, on its own behalf and on behalf of each other Grantor, at its own expense, to execute, acknowledge, deliver and cause to be duly filed all such further instruments and documents and take all such actions as the Notes Collateral Agent may from time to time reasonably request to better assure, preserve, protect and perfect the Security Interest and the rights and remedies created hereby, including the payment of any fees and taxes required in connection with the execution and delivery of this Agreement, the granting of the Security Interest and the filing of any financing statements or other documents in connection herewith or therewith. Subject to the terms of the Intercreditor Agreement, if any amount payable under or in connection with any of the Collateral that is in excess of \$10,000,000 shall be or become evidenced by any promissory note or other instrument, such note or instrument shall be promptly pledged and delivered to the Notes Collateral Agent, for the benefit of the Secured Parties, duly endorsed in a manner reasonably satisfactory to the Notes Collateral Agent.

Without limiting the generality of the foregoing, each Grantor hereby authorizes the Notes Collateral Agent, with prompt notice thereof to the Grantors, to supplement this Agreement by supplementing Schedule I or adding additional schedules hereto to specifically identify any asset or item that may constitute Copyrights, Patents or Trademarks; provided that

any Grantor shall have the right, exercisable within 10 days after it has been notified by the Notes Collateral Agent of the specific identification of such Collateral, to advise the Notes Collateral Agent in writing of any inaccuracy of the representations and warranties made by such Grantor hereunder with respect to such Collateral. Each Grantor agrees that it will use its best efforts to take such action as shall be necessary in order that all representations and warranties hereunder shall be true and correct with respect to such Collateral within 30 days after the date it has been notified by the Notes Collateral Agent of the specific identification of such Collateral.

- (e) Subject to the terms of the Intercreditor Agreement, at its option, the Notes Collateral Agent may discharge past due taxes, assessments, charges, fees, Liens, security interests or other encumbrances at any time levied or placed on the Collateral and not permitted pursuant to Section 4.12 of the Indenture, and may pay for the maintenance and preservation of the Collateral to the extent any Grantor fails to do so as required by the Indenture or this Agreement and within a reasonable period of time after the Notes Collateral Agent has requested that it do so, and each Grantor jointly and severally agrees to reimburse the Notes Collateral Agent within 10 days after demand for any payment made or any reasonable expense incurred by the Notes Collateral Agent pursuant to the foregoing authorization; *provided*, *however*, Grantors shall not be obligated to reimburse the Notes Collateral Agent with respect to any Intellectual Property Collateral which any Grantor has failed to maintain or pursue, or otherwise allowed to lapse, terminate or be put into the public domain, in accordance with Section 2.04(f). Nothing in this paragraph shall be interpreted as excusing any Grantor from the performance of, or imposing any obligation on the Notes Collateral Agent or any Secured Party to cure or perform, any covenants or other promises of any Grantor with respect to taxes, assessments, charges, fees, Liens, security interests or other encumbrances and maintenance as set forth herein or in the other Notes Documents.
- (f) Each Grantor (rather than the Notes Collateral Agent or any Secured Party) shall remain liable (as between itself and any relevant counterparty) to observe and perform all the conditions and obligations to be observed and performed by it under each contract, agreement or instrument relating to the Collateral, all in accordance with the terms and conditions thereof, and each Grantor jointly and severally agrees to indemnify and hold harmless the Notes Collateral Agent and the other Secured Parties from and against any and all liability for such performance.

SECTION 2.04. Additional Covenants.

(a) Except to the extent failure to act could not reasonably be expected to have a Material Adverse Effect, with respect to registration or pending application of each item of its Collateral for which such Grantor has standing to do so, each Grantor agrees to take, at its expense, all reasonable steps, including, without limitation, in the U.S. Patent and Trademark Office, the U.S. Copyright Office and any other governmental authority located in the United States, to (i) maintain the validity and enforceability of any registered Collateral (or applications therefor) and maintain such Collateral in full force and effect, and (ii) pursue the registration and maintenance of each Patent, Trademark, or Copyright registration or application, now or hereafter included in such Collateral of such Grantor, including, without limitation, the payment of required fees and taxes, the filing of responses to office actions issued by the U.S. Patent and Trademark Office, the U.S. Copyright Office or other governmental authorities, the filing of

applications for renewal or extension, the filing of affidavits under Sections 8 and 15 or the U.S. Trademark Act, the filing of divisional, continuation, continuation-in-part, reissue and renewal applications or extensions, the payment of maintenance fees and the participation in interference, reexamination, opposition, cancellation, infringement and misappropriation proceedings.

- (b) Except as could not reasonably be expected to have a Material Adverse Effect, no Grantor shall do or permit any act or knowingly omit to do any act whereby any of its Collateral may lapse, be terminated, or become invalid or unenforceable or placed in the public domain (or in the case of a trade secret, becomes publicly known).
- (c) Except where failure to do so could not reasonably be expected to have a Material Adverse Effect, each Grantor shall take all reasonable steps to preserve and protect each item of its Collateral, including, without limitation, maintaining the quality of any and all products or services used or provided in connection with any of the Trademarks, consistent with the quality of the products and services as of the date hereof, and taking all reasonable steps necessary to ensure that all licensed users of any of the Trademarks abide by the applicable license's terms with respect to the standards of quality.
- (d) Each Grantor agrees that, should it obtain an ownership or other interest in any Collateral after the Closing Date ("After-Acquired Intellectual Property") (i) the provisions of this Agreement shall automatically apply thereto, and (ii) any such After-Acquired Intellectual Property shall automatically become part of the Collateral subject to the terms and conditions of this Agreement with respect thereto.
- (e) Once every fiscal quarter of the Issuer, with respect to issued or registered Patents (or published applications therefor), Trademarks (or applications therefor), and registered Copyrights, each Grantor shall sign and deliver to the Notes Collateral Agent an appropriate supplemental Intellectual Property Security Agreement with respect to all applicable Intellectual Property owned by it as of the last day of such period, to the extent that such Intellectual Property is not covered by any previous Intellectual Property Security Agreement so signed and delivered by it. In each case, it will promptly cooperate as reasonably necessary to enable the Notes Collateral Agent to make any necessary or reasonably desirable recordations with the U.S. Copyright Office or the U.S. Patent and Trademark Office, as appropriate.
- (f) Nothing in this Agreement prevents any Grantor from disposing of, discontinuing the use or maintenance of, failing to pursue, or otherwise allowing to lapse, terminate or be put into the public domain, any of its Collateral to the extent permitted by the Indenture if such Grantor determines in its reasonable business judgment that such discontinuance is desirable in the conduct of its business.

ARTICLE III

REMEDIES

SECTION 3.01. *Remedies Upon Default*. Subject to the terms of the Intercreditor Agreement, if an Event of Default occurs and is continuing, each Grantor agrees to deliver each item of Collateral to the Notes Collateral Agent on demand, and it is agreed that the

Notes Collateral Agent shall have the right, at the same or different times, with respect to any Collateral, on demand, to cause the Security Interest to become an assignment, transfer and conveyance of any of or all such Collateral by the applicable Grantors to the Notes Collateral Agent, or to license or sublicense, whether general, special or otherwise, and whether on an exclusive or nonexclusive basis, any such Collateral throughout the world on such terms and conditions and in such manner as the Notes Collateral Agent shall determine (other than in violation of any then-existing licensing arrangements to the extent that waivers cannot be obtained), and, generally, to exercise any and all rights afforded to a secured party with respect to the Obligations under the Uniform Commercial Code or other applicable law. Without limiting the generality of the foregoing, each Grantor agrees that the Notes Collateral Agent shall have the right, subject to the mandatory requirements of applicable law and the notice requirements described below, to sell or otherwise dispose of all or any part of the Collateral securing the Obligations at a public or private sale, for cash, upon credit or for future delivery as the Notes Collateral Agent shall deem appropriate. Each such purchaser at any sale of Collateral shall hold the property sold absolutely, free from any claim or right on the part of any Grantor, and each Grantor hereby waives (to the extent permitted by law) all rights of redemption, stay and appraisal which such Grantor now has or may at any time in the future have under any rule of law or statute now existing or hereafter enacted.

The Notes Collateral Agent shall give the applicable Grantors 10 days' written notice (which each Grantor agrees is reasonable notice within the meaning of Section 9-611 of the New York UCC or its equivalent in other jurisdictions) of the Notes Collateral Agent's intention to make any sale of Collateral. Such notice, in the case of a public sale, shall state the time and place for such sale. Any such public sale shall be held at such time or times within ordinary business hours and at such place or places as the Notes Collateral Agent may fix and state in the notice (if any) of such sale. At any such sale, the Collateral, or portion thereof, to be sold may be sold in one lot as an entirety or in separate parcels, as the Notes Collateral Agent may (in its sole and absolute discretion) determine. The Notes Collateral Agent shall not be obligated to make any sale of any Collateral if it shall determine not to do so, regardless of the fact that notice of sale of such Collateral shall have been given. The Notes Collateral Agent may, without notice or publication, adjourn any public or private sale or cause the same to be adjourned from time to time by announcement at the time and place fixed for sale, and such sale may, without further notice, be made at the time and place to which the same was so adjourned. In case any sale of all or any part of the Collateral is made on credit or for future delivery, the Collateral so sold may be retained by the Notes Collateral Agent until the sale price is paid by the purchaser or purchasers thereof, but the Notes Collateral Agent shall not incur any liability in case any such purchaser or purchasers shall fail to take up and pay for the Collateral so sold and, in case of any such failure, such Collateral may be sold again upon like notice. At any public (or, to the extent permitted by law, private) sale made pursuant to this Agreement, any Secured Party may bid for or purchase, free (to the extent permitted by law) from any right of redemption, stay, valuation or appraisal on the part of any Grantor (all said rights being also hereby waived and released to the extent permitted by law), the Collateral or any part thereof offered for sale and may make payment on account thereof by using any claim then due and payable to such Secured Party from any Grantor as a credit against the purchase price, and such Secured Party may, upon compliance with the terms of sale, hold, retain and dispose of such property without further accountability to any Grantor therefor. For purposes hereof, a written agreement to purchase the Collateral or any portion thereof shall be treated as a sale thereof; the Notes Collateral Agent

shall be free to carry out such sale pursuant to such agreement and no Grantor shall be entitled to the return of the Collateral or any portion thereof subject thereto, notwithstanding the fact that after the Notes Collateral Agent shall have entered into such an agreement all Events of Default shall have been remedied and the Obligations paid in full. As an alternative to exercising the power of sale herein conferred upon it, the Notes Collateral Agent may proceed by a suit or suits at law or in equity to foreclose this Agreement and to sell the Collateral or any portion thereof pursuant to a judgment or decree of a court or courts having competent jurisdiction or pursuant to a proceeding by a court-appointed receiver. Any sale pursuant to the provisions of this Section 3.01 shall be deemed to conform to the commercially reasonable standards as provided in Section 9-610(b) of the New York UCC or its equivalent in other jurisdictions.

SECTION 3.02. Application of Proceeds.

(a) Subject to the terms of the Intercreditor Agreement, the Notes Collateral Agent shall apply the proceeds of any collection or sale of Collateral, including any Collateral consisting of cash, as follows:

<u>First</u>, to pay Obligations in respect of incurred and unpaid fees and expenses of the Notes Collateral Agent and the Trustee under the Notes Documents;

<u>Second</u>, towards payment of amounts then due and owing and remaining unpaid in respect of the Obligations, pro rata among the Secured Parties according to the amounts of the Obligations then due and owing and remaining unpaid to the Secured Parties.

Third, towards payment of any remaining Obligations, pro rata among the Secured Parties according to the amounts of the Obligations then held by the Secured Parties; and

<u>Last</u>, any balance remaining after the Obligations shall have been paid in full shall be paid over to the Issuer or to whomsoever may be lawfully entitled to receive the same.

The Notes Collateral Agent shall have absolute discretion as to the time of application of any such proceeds, moneys or balances in accordance with this Agreement. Upon any sale of Collateral by the Notes Collateral Agent (including pursuant to a power of sale granted by statute or under a judicial proceeding), the receipt of the Notes Collateral Agent or of the officer making the sale shall be a sufficient discharge to the purchaser or purchasers of the Collateral so sold and such purchaser or purchasers shall not be obligated to see to the application of any part of the purchase money paid over to the Notes Collateral Agent or such officer or be answerable in any way for the misapplication thereof.

(b) In making the determinations and allocations required by this Section 3.02, the Notes Collateral Agent may conclusively rely upon information supplied by the Trustee as to the amounts of unpaid principal and interest and other amounts outstanding with respect to the Obligations, and the Notes Collateral Agent shall have no liability to any of the Secured Parties for actions taken in reliance on such information, provided that nothing in this sentence shall prevent any Grantor from contesting any amounts claimed by any Secured Party in any information so supplied. All distributions made by the Notes Collateral Agent pursuant to this Section 3.02 shall be (subject to any decree of any court of competent jurisdiction) final (absent manifest error), and the Notes Collateral Agent shall have no duty to inquire as to the application by the Trustee of any amounts distributed to it.

SECTION 3.03. *Grant of License to Use Intellectual Property*. For the purpose of enabling the Notes Collateral Agent to exercise rights and remedies under this Agreement at such time as the Notes Collateral Agent shall be lawfully entitled to exercise such rights and remedies, each Grantor shall, upon request by the Notes Collateral Agent at any time after and during the continuance of an Event of Default, grant to the Notes Collateral Agent an irrevocable (until the termination of the Indenture) nonexclusive license (exercisable without payment of royalty or other compensation to the Grantors) to use, license or sublicense any of the Collateral now owned or hereafter acquired by such Grantor, and wherever the same may be located, and including in such license reasonable access to all media in which any of the licensed items may be recorded or stored and to all computer software and programs used for the compilation or printout thereof; *provided*, *however*, that nothing in this Section 3.03 shall require Grantors to grant any license that is prohibited by any rule of law, statute or regulation or is prohibited by, or constitutes a breach or default under or results in the termination of any contract, license, agreement, instrument or other document evidencing, giving rise to or theretofore granted, to the extent permitted by the Indenture, with respect to such property; *provided*, *further*, that such licenses to be granted hereunder with respect to Trademarks shall be subject to the maintenance of quality standards with respect to the goods and services on which such Trademarks are used sufficient to preserve the validity of such Trademarks. The use of such license by the Notes Collateral Agent may be exercised, at the option of the Notes Collateral Agent, during the continuation of an Event of Default; *provided* that any license, sublicense or other transaction entered into by the Notes Collateral Agent in accordance herewith shall be binding upon the Grantors notwithstanding any subsequent cure of an Ev

ARTICLE IV

INDEMNITY, SUBROGATION AND SUBORDINATION

SECTION 4.01. *Indemnity*. In addition to all such rights of indemnity and subrogation as the Grantors may have under applicable law (but subject to Section 4.03), the Issuer agrees that, in the event any assets of any Grantor shall be sold pursuant to this Agreement or any other Collateral Document relating to the Notes to satisfy in whole or in part an Obligation owed to any Secured Party, the Issuer shall indemnify such Grantor in an amount equal to the greater of the book value or the fair market value of the assets so sold.

SECTION 4.02. *Contribution and Subrogation*. Each Grantor (a "Contributing Party") agrees (subject to Section 4.03) that, in the event assets of any other Grantor shall be sold pursuant to any Collateral Document relating to the Notes to satisfy any Obligation owed to any Secured Party, and such other Grantor (the "Claiming Party") shall not have been fully indemnified by the Issuer as provided in Section 4.01, the Contributing Party shall indemnify the Claiming Party in an amount equal to the greater of the book value or the fair market value of such assets, in each case multiplied by a fraction of which the numerator shall be the net worth of the Contributing Party on the date hereof and the denominator shall be the aggregate net worth of all the Contributing Parties together with the net worth of the Claiming Party on the date hereof

(or, in the case of any Grantor becoming a party hereto pursuant to Section 5.14, the date of the Intellectual Property Security Agreement Supplement executed and delivered by such Grantor). Any Contributing Party making any payment to a Claiming Party pursuant to this Section 4.02 shall be subrogated to the rights of such Claiming Party to the extent of such payment.

SECTION 4.03. Subordination.

- (a) Notwithstanding any provision of this Agreement to the contrary, all rights of the Grantors under Sections 4.01 and 4.02 and all other rights of indemnity, contribution or subrogation under applicable law or otherwise shall be fully subordinated to the indefeasible payment in full in cash of the Obligations. No failure on the part of the Issuer or any Grantor to make the payments required by Sections 4.01 and 4.02 (or any other payments required under applicable law or otherwise) shall in any respect limit the obligations and liabilities of any Grantor with respect to its obligations hereunder, and each Grantor shall remain liable for the full amount of the obligations of such Grantor hereunder.
- (b) Each Grantor hereby agrees that upon the occurrence and during the continuance of an Event of Default and after notice from the Notes Collateral Agent all Indebtedness owed by it to any Subsidiary shall be fully subordinated to the indefeasible payment in full in cash of the Obligations.

ARTICLE V

MISCELLANEOUS

SECTION 5.01. *Notices*. All communications and notices hereunder, other than with respect to the Notes Collateral Agent, shall (except as otherwise expressly permitted herein) be in writing and given as provided in Section 13.01 of the Indenture. All communications and notices hereunder to any Grantor shall be given to it in care of the Issuer as provided in Section 13.01 of the Indenture. All communications and notices hereunder to the Notes Collateral Agent is duly given if in writing and delivered in person or mailed by first-class mail (registered or certified, return receipt requested), fax or overnight air courier guaranteeing next day delivery, to the Notes Collateral Agent's address:

Citibank, N.A. 390 Greenwich Street New York, NY 10013 Facsimile: 646-291-1629 Telephone: 212-723-5457

Email: peter.t.baumann@citi.com

Additional Email: oploanswebadmin@citigroup.com

Attention: Peter Baumann

SECTION 5.02. Waivers; Amendment.

- (a) (a) No failure or delay by the Notes Collateral Agent or any Secured Party in exercising any right or power hereunder or under any other Notes Document shall operate as a waiver thereof, nor shall any single or partial exercise of any such right or power, or any abandonment or discontinuance of steps to enforce such a right or power, preclude any other or further exercise thereof or the exercise of any other right or power. The rights and remedies of the Notes Collateral Agent and the Secured Parties hereunder and under the other Notes Documents are cumulative and are not exclusive of any rights or remedies that they would otherwise have. No waiver of any provision of this Agreement or consent to any departure by any Grantor therefrom shall in any event be effective unless the same shall be permitted by paragraph (b) of this Section 5.02, and then such waiver or consent shall be effective only in the specific instance and for the purpose for which given. Without limiting the generality of the foregoing, the issuance of any Additional First Lien Debt shall not be construed as a waiver of any Default, regardless of whether the Notes Collateral Agent or any Secured Party may have had notice or knowledge of such Default at the time. No notice or demand on any Grantor in any case shall entitle any Grantor to any other or further notice or demand in similar or other circumstances.
- (b) Subject to the terms of the Intercreditor Agreement and except as otherwise provided in the Indenture, neither this Agreement nor any provision hereof may be waived, amended or modified except pursuant to an agreement or agreements in writing entered into by the Notes Collateral Agent and the Grantor or Grantors with respect to which such waiver, amendment or modification is to apply, subject to any consent required in accordance with Section 9.02 of the Indenture.

SECTION 5.03. Notes Collateral Agent's Fees and Expenses; Indemnification.

- (a) The parties hereto agree that the Notes Collateral Agent shall be entitled to reimbursement of its expenses incurred hereunder.
- (b) Without limitation of its indemnification obligations under the other Notes Documents, the Issuer agrees to indemnify the Notes Collateral Agent and the other Indemnitees against, and hold each Indemnitee harmless from, any and all losses, claims, damages, liabilities and related expenses, including the reasonable fees, charges and disbursements of any counsel for any Indemnitee, incurred by or asserted against any Indemnitee arising out of, in connection with, or as a result of, the execution, delivery or performance of this Agreement or any claim, litigation, investigation or proceeding relating to any of the foregoing agreement or instrument contemplated hereby, or to the Collateral, whether or not any Indemnitee is a party thereto; *provided* that such indemnity shall not, as to any Indemnitee, be available to the extent that such losses, claims, damages, liabilities or related expenses are determined by a court of competent jurisdiction by final and nonappealable judgment to have resulted from the gross negligence or willful misconduct of such Indemnitee or any Affiliate, director, officer, employee, counsel, agent or attorney-in-fact of such Indemnitee.
- (c) Any such amounts payable as provided hereunder shall be additional Obligations secured hereby and by the other Collateral Documents relating to the Notes. The provisions of this Section 5.03 shall remain operative and in full force and effect regardless of the termination of this Agreement or any other Notes Document, the consummation of the

transactions contemplated hereby, the repayment of any of the Obligations, the invalidity or unenforceability of any term or provision of this Agreement or any other Notes Document, or any investigation made by or on behalf of the Notes Collateral Agent or any other Secured Party. All amounts due under this Section 5.03 shall be payable within 10 days of written demand therefor.

SECTION 5.04. *Successors and Assigns*. Whenever in this Agreement any of the parties hereto is referred to, such reference shall be deemed to include the permitted successors and assigns of such party; and all covenants, promises and agreements by or on behalf of any Grantor or the Notes Collateral Agent that are contained in this Agreement shall bind and inure to the benefit of their respective successors and assigns.

SECTION 5.05. *Survival of Agreement*. All covenants, agreements, representations and warranties made by the Grantors in the Notes Documents and in the certificates or other instruments prepared or delivered in connection with or pursuant to this Agreement or any other Notes Document shall be considered to have been relied upon by the Secured Parties and shall survive the execution and delivery of the Notes Documents and the issuance of any Additional First Lien Debt, regardless of any investigation made by any Secured Party or on its behalf and notwithstanding that the Notes Collateral Agent or any Secured Party may have had notice or knowledge of any Default or incorrect representation or warranty at the time any securities are issued under the Indenture, and shall continue in full force and effect as long as the principal of or any accrued interest on any Note is outstanding and unpaid.

SECTION 5.06. Counterparts; Effectiveness; Several Agreement. This Agreement may be executed in counterparts, each of which shall constitute an original but all of which when taken together shall constitute a single contract. Delivery of an executed signature page to this Agreement by facsimile transmission or other electronic communication shall be as effective as delivery of a manually signed counterpart of this Agreement. This Agreement shall become effective as to any Grantor when a counterpart hereof executed on behalf of such Grantor shall have been delivered to the Notes Collateral Agent and a counterpart hereof shall have been executed on behalf of the Notes Collateral Agent, and thereafter shall be binding upon such Grantor and the Notes Collateral Agent and their respective permitted successors and assigns, and shall inure to the benefit of such Grantor, the Notes Collateral Agent and the other Secured Parties and their respective successors and assigns, except that no Grantor shall have the right to assign or transfer its rights or obligations hereunder or any interest herein or in the Collateral (and any such assignment or transfer shall be void) except as expressly contemplated by this Agreement or the Indenture. This Agreement shall be construed as a separate agreement with respect to each Grantor and may be amended, modified, supplemented, waived or released with respect to any Grantor without the approval of any other Grantor and without affecting the obligations of any other Grantor hereunder.

SECTION 5.07. Severability. Any provision of this Agreement held to be invalid, illegal or unenforceable in any jurisdiction shall, as to such jurisdiction, be ineffective to the extent of such invalidity, illegality or unenforceability without affecting the validity, legality and enforceability of the remaining provisions hereof; and the invalidity of a particular provision in a particular jurisdiction shall not invalidate such provision in any other jurisdiction. The parties shall endeavor in good-faith negotiations to replace the invalid, illegal or unenforceable provisions with valid provisions the economic effect of which comes as close as possible to that of the invalid, illegal or unenforceable provisions.

SECTION 5.08. *Right of Set-Off.* Subject to the terms of the Intercreditor Agreement, in addition to any rights and remedies of the Secured Parties provided by Law, upon the occurrence and during the continuance of any Event of Default, each Secured Party and its Affiliates is authorized at any time and from time to time, without prior notice to the Issuer or any other Grantor, any such notice being waived by the Issuer (on its own behalf and on behalf of each Grantor and its Subsidiaries) to the fullest extent permitted by applicable Law, to set off and apply any and all deposits (general or special, time or demand, provisional or final) at any time held by, and other Indebtedness at any time owing by, such Secured Party and its Affiliates, as the case may be, to or for the credit or the account of the respective Grantors and their Subsidiaries against any and all Obligations owing to such Secured Party and its Affiliates hereunder or under any other Notes Document, now or hereafter existing, irrespective of whether or not such Secured Party or Affiliate shall have made demand under this Agreement or any other Notes Document and although such Obligations may be contingent or unmatured or denominated in a currency different from that of the applicable deposit or Indebtedness. Each Secured Party agrees promptly to notify the Issuer and the Trustee after any such set off and application made by such Secured Party; provided that the failure to give such notice shall not affect the validity of such setoff and application. The rights of the Trustee and each Secured Party under this Section 5.08 are in addition to other rights and remedies (including other rights of setoff) that the Trustee and such Secured Party may have.

SECTION 5.09. Governing Law; Jurisdiction; Consent to Service of Process.

- (a) This Agreement shall be construed in accordance with and governed by the law of the State of New York.
- (b) Each of the Grantors hereby irrevocably and unconditionally submits, for itself and its property, to the exclusive jurisdiction of the Supreme Court of the State of New York sitting in New York City and of the United States District Court of the Southern District of New York, and any appellate court from any thereof, in any action or proceeding arising out of or relating to this Agreement or any other Notes Document, or for recognition or enforcement of any judgment, and each of the parties hereto hereby irrevocably and unconditionally agrees that all claims in respect of any such action or proceeding may be heard and determined in such New York State or, to the extent permitted by law, in such Federal court. Each of the parties hereto agrees that a final judgment in any such action or proceeding shall be conclusive and may be enforced in other jurisdictions by suit on the judgment or in any other manner provided by law. Nothing in this Agreement or any other Notes Document shall affect any right that the Notes Collateral Agent or any Secured Party may otherwise have to bring any action or proceeding relating to this Agreement or any other Notes Document against any Grantor or its properties in the courts of any jurisdiction.
- (c) Each of the Grantors hereby irrevocably and unconditionally waives, to the fullest extent it may legally and effectively do so, any objection which it may now or hereafter have to the laying of venue of any suit, action or proceeding arising out of or relating to this Agreement or any other Notes Document in any court referred to in paragraph (b) of this Section 5.09. Each of the parties hereto hereby irrevocably waives, to the fullest extent permitted by law, the defense of an inconvenient forum to the maintenance of such action or proceeding in any such court.

(d) Each party to this Agreement irrevocably consents to service of process in the manner provided for notices in Section 5.01. Nothing in this Agreement or any other Notes Document will affect the right of any party to this Agreement to serve process in any other manner permitted by law.

SECTION 5.10. WAIVER OF JURY TRIAL. EACH PARTY HERETO HEREBY WAIVES, TO THE FULLEST EXTENT PERMITTED BY APPLICABLE LAW, ANY RIGHT IT MAY HAVE TO A TRIAL BY JURY IN ANY LEGAL PROCEEDING DIRECTLY OR INDIRECTLY ARISING OUT OF OR RELATING TO THIS AGREEMENT, ANY OTHER NOTES DOCUMENT OR THE TRANSACTIONS CONTEMPLATED HEREBY (WHETHER BASED ON CONTRACT, TORT OR ANY OTHER THEORY). EACH PARTY HERETO (A) CERTIFIES THAT NO REPRESENTATIVE, AGENT OR ATTORNEY OF ANY OTHER PARTY HAS REPRESENTED, EXPRESSLY OR OTHERWISE, THAT SUCH OTHER PARTY WOULD NOT, IN THE EVENT OF LITIGATION, SEEK TO ENFORCE THE FOREGOING WAIVER AND (B) ACKNOWLEDGES THAT IT AND THE OTHER PARTIES HERETO HAVE BEEN INDUCED TO ENTER INTO THIS AGREEMENT BY, AMONG OTHER THINGS, THE MUTUAL WAIVERS AND CERTIFICATIONS IN THIS SECTION 5.10.

SECTION 5.11. *Headings*. Article and Section headings and the Table of Contents used herein are for convenience of reference only, are not part of this Agreement and are not to affect the construction of, or to be taken into consideration in interpreting, this Agreement.

SECTION 5.12. Security Interest Absolute. All rights of the Notes Collateral Agent hereunder, the Security Interest, the grant of a security interest in the Pledged Collateral and all obligations of each Grantor hereunder shall be absolute and unconditional irrespective of (a) any lack of validity or enforceability of the Indenture, any other Notes Document, any agreement with respect to any of the Obligations or any other agreement or instrument relating to any of the foregoing, (b) any change in the time, manner or place of payment of, or in any other term of, all or any of the Obligations, or any other amendment or waiver of or any consent to any departure from the Indenture, any other Notes Document or any other agreement or instrument, (c) any exchange, release or non-perfection of any Lien on other collateral, or any release or amendment or waiver of or consent under or departure from any guarantee, securing or guaranteeing all or any of the Obligations or (d) any other circumstance that might otherwise constitute a defense available to, or a discharge of, any Grantor in respect of the Obligations or this Agreement.

SECTION 5.13. Termination or Release.

(a) This Agreement, the Security Interest and all other security interests granted hereby shall terminate with respect to all Obligations (other than (x) obligations under Secured Hedge Agreements not yet due and payable, (y) Cash Management Obligations not yet due and payable and (z) contingent indemnification obligations not yet accrued and payable) when all the outstanding Obligations have been indefeasibly paid in full.

- (b) A Grantor shall automatically be released from its obligations hereunder and the Security Interest in the Collateral of such Grantor shall be automatically released upon the consummation of any transaction permitted by the Indenture as a result of which such Grantor ceases to be a Subsidiary or is designated as an Unrestricted Subsidiary of Holdings III; provided that Holders of more than 50% in principal amount of the total outstanding Notes shall have consented to such transaction (to the extent required by the Indenture) and the terms of such consent did not provide otherwise.
- (c) Upon any sale or other transfer by any Grantor of any Collateral (other than any transfer to another Grantor) that is permitted under the Indenture, or upon the effectiveness of any written consent to the release of the security interest granted hereby in any Collateral pursuant to Section 11.02 of the Indenture, the security interest of such Grantor in such Collateral shall be automatically released.
- (d) A Grantor (other than Holdings V and the Issuer) shall automatically be released from its obligations hereunder and the Security Interest in the Collateral of such Grantor shall be automatically released if such Grantor ceases to be a Material Domestic Subsidiary.
- (e) If the security interest on any Collateral is released pursuant to Section 2.04 of the Intercreditor Agreement and such release results in the release of the security interest on such Collateral under this Agreement or any Collateral Document relating to the Notes, the security interest on such Collateral granted hereunder or under any such Collateral Document relating to the Notes shall be automatically released.
- (f) In connection with any termination or release pursuant to paragraph (a), (b) or (c) of this Section 5.13, the Notes Collateral Agent shall execute and deliver to any Grantor, at such Grantor's expense, all documents that such Grantor shall reasonably request to evidence such termination or release. Any execution and delivery of documents pursuant to this Section 6.13 shall be without recourse to or warranty by the Notes Collateral Agent.
- (g) In the event that any of the Collateral shall be transferred by any Grantor in connection with the Foreign Reorganization, the Security Interest granted hereunder on such Collateral shall automatically be discharged and released and all rights to such Collateral shall revert to the applicable Grantor without any further action by the Notes Collateral Agent or any other Person. Without prejudice to the foregoing, upon the request of the applicable Grantor, the Notes Collateral Agent, at the expense of such Grantor, shall promptly execute and deliver to such Grantor, all releases, termination statements, stock certificates, any certificated securities or any other documents necessary or desirable for the release of the Security Interest on such Collateral.

SECTION 5.14. *Additional Restricted Subsidiaries*. Pursuant to Section 11.05 of the Indenture, certain Restricted Subsidiaries of Holdings III that were not in existence or not Secured Guarantors on the date of the Indenture are required to enter in this Agreement as Grantors upon becoming Secured Guarantors. Upon execution and delivery by the Notes

Collateral Agent and a Restricted Subsidiary of an Intellectual Property Security Agreement Supplement, such Restricted Subsidiary shall become a Grantor hereunder with the same force and effect as if originally named as a Grantor herein. The execution and delivery of any such instrument shall not require the consent of any other Grantor hereunder. The rights and obligations of each Grantor hereunder shall remain in full force and effect notwithstanding the addition of any new Grantor as a party to this Agreement.

SECTION 5.15. *General Authority of the Notes Collateral Agent*. By acceptance of the benefits of this Agreement and any other Collateral Documents relating to the Notes, each Secured Party (whether or not a signatory hereto) shall be deemed irrevocably (a) to consent to the appointment of the Notes Collateral Agent as its agent hereunder and under such other Collateral Documents relating to the Notes, (b) to confirm that the Notes Collateral Agent shall have the authority to act as the exclusive agent of such Secured Party for the enforcement of any provisions of this Agreement and such other Collateral Documents relating to the Notes against any Grantor, the exercise of remedies hereunder or thereunder and the giving or withholding of any consent or approval hereunder or thereunder relating to any Collateral or any Grantor's obligations with respect thereto, (c) to agree that it shall not take any action to enforce any provisions of this Agreement or any other Collateral Document relating to the Notes against any Grantor, to exercise any remedy hereunder or thereunder or to give any consents or approvals hereunder or thereunder except as expressly provided in this Agreement or any other Collateral Document relating to the Notes and (d) to agree to be bound by the terms of this Agreement and any other Collateral Documents relating to the Notes.

SECTION 5.16. *Notes Collateral Agent Appointed Attorney-in-Fact*. Each Grantor hereby appoints the Notes Collateral Agent the attorney-in-fact of such Grantor for the purpose of carrying out the provisions of this Agreement and taking any action and executing any instrument that the Notes Collateral Agent may deem necessary or advisable to accomplish the purposes hereof at any time after and during the continuance of an Event of Default, which appointment is irrevocable (until the termination of the Indenture) and coupled with an interest. Without limiting the generality of the foregoing, the Notes Collateral Agent shall have the right, upon the occurrence and during the continuance of an Event of Default and notice by the Notes Collateral Agent to the Issuer of its intent to exercise such rights, with full power of substitution either in the Notes Collateral Agent's name or in the name of such Grantor (a) to receive, endorse, assign and/or deliver any and all notes, acceptances, checks, drafts, money orders or other evidences of payment relating to the Collateral or any part thereof; (b) to demand, collect, receive payment of, give receipt for and give discharges and releases of all or any of the Collateral; (c) to commence and prosecute any and all suits, actions or proceedings at law or in equity in any court of competent jurisdiction to collect or otherwise realize on all or any of the Collateral or to enforce any rights in respect of any Collateral; (d) to settle, compromise, compound, adjust or defend any actions, suits or proceedings relating to all or any of the Collateral; and (e) to use, sell, assign, transfer, pledge, make any agreement with respect to or otherwise deal with all or any of the Collateral, and to do all other acts and things necessary to carry out the purposes of this Agreement, as fully and completely as though the Notes Collateral Agent were the absolute owner of the Collateral for all purposes; *provided* that nothing herein contained shall be construed as requiring or obligating t

respect to the Collateral or any part thereof or the moneys due or to become due in respect thereof or any property covered thereby. The Notes Collateral Agent and the other Secured Parties shall be accountable only for amounts actually received as a result of the exercise of the powers granted to them herein, and neither they nor their officers, directors, employees or agents shall be responsible to any Grantor for any act or failure to act hereunder, except for their own gross negligence or wilful misconduct or that of any of their Affiliates, directors, officers, employees, counsel, agents or attorneys-in-fact.

IN WITNESS WHEREOF, the parties hereto have duly executed this Agreement as of the day and year first above written.

FREESCALE SEMICONDUCTOR INC.,

By: /s/ Steven P. Goel

Name: Steven P. Goel

Title: Vice President and Treasurer

FREESCALE SEMICONDUCTOR HOLDINGS V, INC.,

By: /s/ Steven P. Goel

Name: Steven P. Goel Title: Treasurer

SIGMATEL, LLC,

By: Freescale Semiconductor, Inc.,

as its Sole Member

By: /s/ Steven P. Goel

Name: Steven P. Goel Title: Treasurer

[Intellectual Property Security Agreement]

CITIBANK, N.A. as Notes Collateral Agent

By: /s/ Matthew Burke

Name: Matthew Burke Title: Vice President

[Intellectual Property Security Agreement]

COPYRIGHTS

Freescale Semiconductor, Inc. – Copyrights; United States

| Owner | Country | Title | Reg. No. |
|-------------------------------|---------|---|--------------|
| Freescale Semiconductor, Inc. | US | PEG WindowBuilder Manual | TX0007366227 |
| Freescale Semiconductor, Inc. | US | PEG Programming Manual | TX0007366228 |
| Freescale Semiconductor, Inc. | US | PEG API Reference Manual | TX0007366230 |
| Freescale Semiconductor, Inc. | US | PEG software (1.8.2) | TX0007366580 |
| Freescale Semiconductor, Inc. | US | C/PEG software (1.6.4) | TX0007368278 |
| Freescale Semiconductor, Inc. | US | WindowBuilder software tool (1.94) | TX0007368374 |
| Freescale Semiconductor, Inc. | US | WindowBuilder software tool (C/PEG, 1.6.4) | TX0007368401 |
| Freescale Semiconductor, Inc. | US | WindowBuilder software tool (PEG 1803) | TX0007368438 |
| Freescale Semiconductor, Inc. | US | C/PEG software | TX0007368460 |
| Freescale Semiconductor, Inc. | US | PEG software (2.3.7) | TX0007368557 |
| Freescale Semiconductor, Inc. | US | WindowBuilder software tool | TX0007369069 |
| Freescale Semiconductor, Inc. | US | PEG software | TX0007369215 |
| Freescale Semiconductor, Inc. | US | Simulot software (2010) | TXu001828658 |
| Freescale Semiconductor, Inc. | US | Factory Scheduling Tool (FaST) software (2010) | TXu001828670 |
| Freescale Semiconductor, Inc. | US | OpStation software (2010) | TXu001828679 |
| Freescale Semiconductor, Inc. | US | Graphical Manufacturing Monitor Systems (GraMMs) software (2010) | TXu001828696 |
| Freescale Semiconductor, Inc. | US | Flowview software (2010) | TXu001828701 |
| Freescale Semiconductor, Inc. | US | Java Graphical Manufacturing Monitor Systems (GraMMs) software (2010) | TXu001828704 |
| Freescale Semiconductor, Inc. | US | OpStation software | TXu001830003 |
| Freescale Semiconductor, Inc. | US | Flowview software | TXu001830005 |
| Freescale Semiconductor, Inc. | US | Factory Scheduling Tool (FaST) software | TXu001830009 |
| Freescale Semiconductor, Inc. | US | Simulot software | TXu001830010 |
| Freescale Semiconductor, Inc. | US | Java Graphical Manufacturing Monitor Systems (GraMMs) software | TXu001830012 |
| Freescale Semiconductor, Inc. | US | Graphical Manufacturing Monitor Systems (GraMMs) software | TXu001830013 |
| Freescale Semiconductor, Inc. | US | Hero chip | VA0001372428 |
| | | | |

SCHEDULE 1A (Copyrights)

SigmaTel, Inc. – Copyrights; United States

| <u>Title</u> | Reg. No. | Reg. Date | Copyright Claimant |
|---|--------------|------------|--------------------|
| Sigma Tel host audio driver 0205 software | TX0005355465 | 2001-06-07 | SigmaTel, LLC |
| Sigma Tel host audio driver wdm 7085 general software | TX0005355469 | 2001-06-07 | SigmaTel, LLC |
| SigmaTel host audio NT driver 4.5049 | TX0005377822 | 2001-06-12 | SigmaTel, LLC |
| SigmaTel host audio unified NT driver 6004 | TX0005431336 | 2001-06-12 | SigmaTel, LLC |
| STIR4200 coinstaller | TX0005385381 | 2001-06-12 | SigmaTel, LLC |
| STIr4200 NDIS miniport device driver is a computer program with trade secrets | TX0005377823 | 2001-06-12 | SigmaTel, LLC |
| STMP3400 audio player firmware ATLM-0117 | TX0005338511 | 2001-06-11 | SigmaTel, LLC |
| STMP3400 boot loader boot ROM A4-03 : general release | TX0005338512 | 2001-06-11 | SigmaTel, LLC |
| STMP3400 booty booter: ver booty-01 | TX0005338509 | 2001-06-11 | SigmaTel, LLC |
| STMP3400 device control class firmware ver DCC.017 | TX0005338510 | 2001-06-11 | SigmaTel, LLC |
| STMP3400 host firmware update utility | TX0005329066 | 2001-06-11 | SigmaTel, LLC |
| STMP3400 host formatter utility | TX0005329065 | 2001-06-11 | SigmaTel, LLC |
| STMP3400 host SCSI miniport driver | TX0005329058 | 2001-06-11 | SigmaTel, LLC |
| STMP3400 host USB device driver : general release | TX0005338508 | 2001-06-11 | SigmaTel, LLC |

SCHEDULE 1A (Copyrights)

PATENTS Freescale Semiconductor, Inc. – Registered Patents; United States

| Owner | Patent # | Description |
|-------------------------------|----------|--|
| FREESCALE SEMICONDUCTOR, INC. | 5339266 | PARALLEL METHOD AND APPARATUS FOR DETECTING AND COMPLETING F LOATING POINT OPERATIONS INVOL VING SPECIAL OPERANDS |
| FREESCALE SEMICONDUCTOR, INC. | 5371394 | DOUBLE IMPLANTED LATERALLY DIF FUSED MOS DEVICE AND METHOD TH EREOF |
| FREESCALE SEMICONDUCTOR, INC. | 5381114 | A CONTINUOUS TIME COMMON MODE FEEDBACK AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 5386341 | SEMICONDUCTOR CARRIER ASSEMBLY |
| FREESCALE SEMICONDUCTOR, INC. | 5387913 | RECEIVER WITH DIGITAL TUNING A ND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5391397 | METHOD OF ADHESION TO A POLYMI DE SURFACE BY FORMATION OF COV ALENT BONDS |
| FREESCALE SEMICONDUCTOR, INC. | 5391999 | GLITCHLESS SWITCHED-CAPACITOR BIQUAD LOW PASS FILTER |
| FREESCALE SEMICONDUCTOR, INC. | 5394027 | HIGH VOLTAGE CHARGE PUMP AND R ELATED CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | 5396296 | VIDEO FEEDBACK MATCHING CIRCUI T AND METHOD THERE |
| FREESCALE SEMICONDUCTOR, INC. | 5399507 | FABRICATION OF MIXED THIN-FILM AND BULK SEMICONDUCTOR SUBSTRA TE FOR INTEGRATED CIRCUIT APPL ICATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 5399887 | MODULATION DOPED FIELD EFFECT TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 5400274 | MEMORY HAVING LOOPED GLOBAL DA TA LINES FOR PROPAGATION DELAY MATCHING |
| FREESCALE SEMICONDUCTOR, INC. | 5404386 | PROGRAMMABLE CLOCK FOR AN ANAL OG CONVERTER IN A DATA PROCESS OR AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5416744 | MEMORY HAVING BIT LINE LOAD WI TH AUTOMATIC BIT LINE PRECHARG E AND EQUALIZATION |
| FREESCALE SEMICONDUCTOR, INC. | 5424245 | CIRCUIT AND METHOD OF FORMING VIAS THROUGH TWO-SIDED SUBSTRA TE |
| FREESCALE SEMICONDUCTOR, INC. | 5426263 | ELECTRONIC ASSEMBLY HAVING A DOUBLE-SIDED LEADLESS COMPONENT |
| FREESCALE SEMICONDUCTOR, INC. | 5427964 | INSULATED GATE FIELD EFFECT TR ANSISTOR AND METHOD FOR FABRIC ATING |
| FREESCALE SEMICONDUCTOR, INC. | 5429293 | SOLDERING PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 5435481 | SOLDERING PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 5436203 | SHIELDED LIQUID ENCAPSULATED S EMICONDUCTOR DEVICE AND METHOD FOR MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5437189 | DUAL ABSOLUTE PRESSURE SENSOR AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 5441914 | METHOD OF FORMING CONDUCTIVE I NTERCONNECT STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 5442240 | METHOD OF ADHESION TO A POLYMI DE SURFACE BY FORMATION OF COV ALENT BONDS |
| FREESCALE SEMICONDUCTOR, INC. | 5442628 | LOCAL AREA NETWORK DATA PROCES SING SYSTEM CONTAINING A QUAD ELASTIC BUFFER AND LAYER MANAG EMENT (ELM) INTEGRATED CIRCUIT AND METHOD OF SWITCHING |
| FREESCALE SEMICONDUCTOR, INC. | 5446625 | CHIP CARRIER AND METHOD FOR MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 5447874 | A METHOD FOR MAKING A SEMICOND UCTOR DEVICE GATE |
| FREESCALE SEMICONDUCTOR, INC. | 5451274 | REFLOW OF MULTI-LAYER METAL BU MPS |
| FREESCALE SEMICONDUCTOR, INC. | 5451543 | STRAIGHT SIDEWALL PROFILE CONT ACT OPENING TO UNDERLYING INTE RCONNECT AND METHOD FOR MAKING THE SAME |

| Owner | Patent # | Description |
|-------------------------------|----------|---|
| FREESCALE SEMICONDUCTOR, INC. | 5454270 | HERMETICALLY SEALED PRESSURE S ENSOR AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 5460704 | FERRITE FILM AND METHOD OF DEPOSITING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5461007 | PROCESS FOR POLISHING AND ANAL YZING A LAYER OVER A PATTERNED SEMICONDUCTOR SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 5463353 | RESISTORLESS VCO INCLUDING CUR RENT SOURCE AND SINK CONTROLL NG A CURRENT CONTROLLED OSCILL ATOR |
| FREESCALE SEMICONDUCTOR, INC. | 5465626 | PRESSURE SENSOR WITH STRESS IS OLATION PLATFORM HERMETICALLY SEALED TO PROTECT SENSOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | 5467253 | SEMICONDUCTOR DEVICE AND METHO D OF FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 5467455 | DATA PROCESSING SYSTEM AND MET HOD FOR PERFORMING DYNAMIC BUS TERMINATION |
| FREESCALE SEMICONDUCTOR, INC. | 5468999 | LIQUID ENCAPSULATED BALL GRID ARRAY SEMICONDUCTOR DEVICE WIT H FINE PITCH WIRE BONDING |
| FREESCALE SEMICONDUCTOR, INC. | 5469476 | SPIKE FILTER CIRCUIT AND METHO D THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5470787 | SEMICONDUCTOR DEVICE SOLDER BU MP HAVING INTRINSIC POTENTIAL FOR FORMING AN EXTENDED EUTECT IC REGION AND METHOD FOR MAKIN G AND USING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5471422 | EEPROM CELL WITH ISOLATION TRA NSISTOR AND METHODS FOR MAKING AND OPERATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5473569 | A METHOD FOR OPERATING A FLASH MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 5475255 | CIRCUIT DIE HAVING IMPROVED SUBSTRATE NOISE ISOLATION |
| FREESCALE SEMICONDUCTOR, INC. | 5476816 | PROCESS FOR ETCHING AN INSULAT ING LAYER AFTER A METAL ETCHIN G STEP |
| FREESCALE SEMICONDUCTOR, INC. | 5478436 | SELECTIVE CLEANING PROCESS FOR FABRICATING A SEMICONDUCTOR D EVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5482878 | INSULATED GATE FIELD EFFECT TR ANSISTOR HAVING SUBTHRESHOLD S WING AND METHOD FOR FABRICATIN G |
| FREESCALE SEMICONDUCTOR, INC. | 5484740 | III-V SEMICONDUCTOR GATE STRUC TURE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 5485487 | RECONFIGURALE COUNTER AND PULS E WIDTH MODULATOR (PWM) USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5485602 | INTEGRATED CIRCUIT HAVING A CO NTROL SIGNAL FOR IDENTIFYING C OINCIDING ACTIVE EDGES OF TWO CLOCK SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 5486792 | METHOD AND APPARATUS FOR CALCU LATING A DIVIDER IN A DIGITAL PHASE LOCK LOOP |
| FREESCALE SEMICONDUCTOR, INC. | 5486824 | DATA PROCESSOR WITH A HARDWARE KEYSCAN CIRCUIT, HARDWARE KEYS CAN CIRCUIT, AND METHOD THEREF OR |
| FREESCALE SEMICONDUCTOR, INC. | 5488688 | DATA PROCESSOR WITH REAL-TIME DIAGNOSTIC CAPABILTIY |
| FREESCALE SEMICONDUCTOR, INC. | 5489988 | ENVIRONMENTAL SENSOR AND METHO D THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5492223 | INTERLOCKING AND INVERTIBLE SE MICONDUCTOR DEVICE TRAY AND TE ST CONTACTOR MATING THERETO |
| FREESCALE SEMICONDUCTOR, INC. | 5492863 | METHOD FOR FORMING CONDUCTIVE BUMPS ON A SEMICONDUCTOR DEVIC E |
| FREESCALE SEMICONDUCTOR, INC. | 5496438 | METHOD OF REMOVING PHOTO RESIS T |
| FREESCALE SEMICONDUCTOR, INC. | 5498767 | METHOD FOR POSITIONING BOND PA DS IN A SEMICONDUCTOR DIE LAYO UT |
| FREESCALE SEMICONDUCTOR, INC. | 5500543 | SENSOR FOR DETERMINING A RATIO OF MATERIALS IN A MIXTURE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5501943 | METHOD OF PATTERNING AN INORGANIC OVERCOAT FOR A LIQUID CRYSTAL DISPLAY ELECTRODE |
| FREESCALE SEMICONDUCTOR, INC. | 5502406 | LOW POWER LEVEL SHIFT CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5506544 | BIAS CIRCUIT FOR DEPLETION MOD E FIELD EFFECT TRANSISTORS |
| | | |

| Owner | Patent # | Description |
|-------------------------------|----------|---|
| FREESCALE SEMICONDUCTOR, INC. | 5510645 | SEMICONDUCTOR STRUCTURE HAVING AN AIR REGION AND METHOD OF FO RMING THE SEMICONDUCTOR STRUCT URE |
| FREESCALE SEMICONDUCTOR, INC. | 5512518 | METHOD OF MANUFACTURE OF MULTI LAYER DIELECTRIC ON A III-V SU BSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 5513358 | METHOD AND APPARATUS FOR POWER -UP STATE INITIALIZATION IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5514891 | N-TYPE HIGFET AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5514892 | ELECTROSTATIC DISCHARGE PROTEC TION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5515232 | STATIC PROTECTION CIRCUIT FOR A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5519340 | LINE DRIVER HAVING MAXIMUM OUT PUT VOLTAGE CAPACITY |
| FREESCALE SEMICONDUCTOR, INC. | 5525920 | COMPARATOR CIRCUIT AND METHOD THEREFOF |
| FREESCALE SEMICONDUCTOR, INC. | 5527424 | PRECONDITIONER FOR A POLISHING PAD AND METHOD FOR USING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5528692 | FREQUENCY INVERSION SCRAMBLER WITH INTEGRATED HIGH-PASS FILT ER |
| FREESCALE SEMICONDUCTOR, INC. | 5529682 | METHOD FOR MAKING SEMICONDUCTO R DEVICES HAVING ELECTROPLATED LEADS |
| FREESCALE SEMICONDUCTOR, INC. | 5530383 | METHOD AND APPARATUS FOR A FRE QUENCY DETECTION CIRCUIT FOR U SE IN A PHASE LOCKED LOOP |
| FREESCALE SEMICONDUCTOR, INC. | 5530676 | METHOD AND APPARATUS FOR REDUC ING POWER CONSUMPTION IN MEMOR Y CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 5530804 | SUPERSCALAR PROCESSOR WITH PLU RAL PIPELINED EXECUTION UNITS EACH UNIT SELECTIVELY HAVING B OTH NORMAL AND DEBUG MODES |
| FREESCALE SEMICONDUCTOR, INC. | 5530824 | ADDRESS TRANSLATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5530825 | DATA PROCESSOR WITH BRANCH TAR GET ADDRESS CACHE AND METHOD O F OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 5532509 | SEMICONDUCTOR INVERTER LAYOUT HAVING IMPROVED ELECTROMIGRATI ON CHARACTERISTICS IN THE OUTP UT MODE |
| FREESCALE SEMICONDUCTOR, INC. | 5532899 | VOLTAGE PROTECTION STRUCTURE F OR SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 5534462 | METHOD FOR FORMING A PLUG AND SEMICONDUCTOR DEVICE HAVING TH E SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5534784 | METHOD FOR PROBING A SEMICONDU CTOR WAFER |
| FREESCALE SEMICONDUCTOR, INC. | 5534819 | CIRCUIT AND METHOD FOR REDUCIN G VOLTAGE ERROR WHEN CHARGING AND DISCHARGING A VARIABLE CAP ACITOR THROUGH A SWITCH |
| FREESCALE SEMICONDUCTOR, INC. | 5535349 | A DATA PROCESSING SYSTEM AND M ETHOD FOR PROVIDING CHIP SELEC TS TO PERIPHERAL DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 5536962 | SEMICONDUCTOR DEVICE HAVING A BURIED CHANNEL TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 5539200 | INTEGRATED OPTOELECTRONIC SUBS TRATE |
| FREESCALE SEMICONDUCTOR, INC. | 5539351 | CIRCUIT AND METHOD FOR REDUCIN G A GATE VOLTAGE OF A TRANSMIS SION GATE WITHIN A CHARGE PUMP CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5539733 | METHOD FOR SWITCHING DATA FLOW IN A FIBER DISTRIBUTED DATA I NTERFACE (FDDI) SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5539892 | ADDRESS TRANSLATION LOOKASIDE BUFFER REPLACEMENT APPARATUS A ND METHOD WITH USER OVERIDE |
| FREESCALE SEMICONDUCTOR, INC. | 5541135 | METHOD OF FABRICATING A FLIP C HIP SEMICONDUCTOR DEVICE HAVIN G AN INDUCTOR |
| FREESCALE SEMICONDUCTOR, INC. | 5541450 | LOW-PROFILE BALL-GRID ARRAY SE MICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 5545359 | METHOD OF MAKING A PLASTIC MOL DED OPTOELECTRONIC INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | 5545574 | PROCESS FOR FORMING A SEMICOND UCTOR DEVICE HAVING A METALSE MICONDUCTOR COMPOUND |
| FREESCALE SEMICONDUCTOR, INC. | 5545912 | ELECTRONIC DEVICE ENCLOSURE IN CLUDING A CONDUCTIVE CAP AND S |

UBSTRATE

| Owner | Patent # | Description |
|-------------------------------|----------|---|
| FREESCALE SEMICONDUCTOR, INC. | 5546047 | METHOD AND APPARATUS OF AN OPE RATIONAL AMPLIFIER WITH A WIDE DYNAMIC RANGE |
| FREESCALE SEMICONDUCTOR, INC. | 5546333 | A DATA PROCESSOR HAVING A DATA TABLE FOR PERFORMING A DUAL F UNCTION OF ALPHANUMERIC NOTICE AND NUMERICAL CALCULATION |
| FREESCALE SEMICONDUCTOR, INC. | 5548794 | DATA PROCESSOR AND METHOD FOR PROVIDING SHOW CYCLES ON A FAST MULTIPLEXED BUS |
| FREESCALE SEMICONDUCTOR, INC. | 5550090 | METHOD FOR FABRICATING A MONOL ITHIC SEMICONDUCTOR DEVICE WIT H INTEGRATED SURFACE MICROMACH INED STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | 5550503 | CIRCUIT AND METHOD FOR REDUCIN G VOLTAGE ERROR WHEN CHARGING AND DISCHARGING A CAPACITOR TH ROUGH A TRANSMISSION GATE |
| FREESCALE SEMICONDUCTOR, INC. | 5550774 | MEMORY CACHE WITH LOW POWER CO NSUMPTION AND METHOD OF OPERAT ION |
| FREESCALE SEMICONDUCTOR, INC. | 5551076 | CIRCUIT AND METHOD OF SERIES B IASING A SINGLE-ENDED MIXER |
| FREESCALE SEMICONDUCTOR, INC. | 5551627 | ALLOY SOLDER CONNECT ASSEMBLY AND METHOD OF CONNECTION |
| FREESCALE SEMICONDUCTOR, INC. | 5552332 | PROCESS FOR FABRICATING A MOSF ET DEVICE HAVING REDUCED REVER SE SHORT CHANNEL EFFECTS |
| FREESCALE SEMICONDUCTOR, INC. | 5553019 | WRITE ONCE READ MANY MEMORY USING EEPROM CELLS |
| FREESCALE SEMICONDUCTOR, INC. | 5553236 | METHOD AND APPARATUS FOR TESTI NG A CLOCK STOPPING/STARTING F UNCTION OF A LOW POWER MODE IN A DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 5553566 | HIGHLY DOPED N+ SUBSTRATES AND METHOD FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 5554869 | ELECTRICALLY PROGRAMMABLE READ -ONLY MEMORY AND ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | 5554940 | BUMPED SEMICONDUCTOR DEVICE AN D METHOD FOR PROBING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5559054 | METHOD FOR BALL BUMPING A SEMI CONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5559359 | MICROWAVE INTEGRATED CIRCUIT P ASSIVE ELEMENT STRUCTURE AND M ETHOD FOR REDUCING SIGNAL PROP AGATION LOSSES |
| FREESCALE SEMICONDUCTOR, INC. | 5559500 | OVERCURRENT SENSE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5559981 | PSEUDO STATIC MASK OPTION REGI STER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5561302 | ENHANCED PERFORMANCE MOSFET |
| FREESCALE SEMICONDUCTOR, INC. | 5561738 | A DATA PROCESSOR FOR EXECUTING A FUZZY LOGIC OPERATION AND M ETHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5564091 | METHOD AND APPARATUS FOR OPERA TING AN AUTOMATIC FREQUENCY CO NTROL IN A RADIO |
| FREESCALE SEMICONDUCTOR, INC. | 5565690 | METHOD FOR DOPING STRAINED HET ERO JUNCTION SEMICONDUCTOR DEV ICES AND STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 5565813 | APPARATUS FOR A LOW VOLTAGE DI FFERENTIAL AMPLIFIER INCORPORA TING SWITCHED CAPACITORS |
| FREESCALE SEMICONDUCTOR, INC. | 5567648 | INTERCONNECT BUMP APPARATUS AN D METHOD FOR FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5570310 | METHOD AND DATA PROCESSOR FO R FINDING A LOGARITHM OF A NUMBER |
| FREESCALE SEMICONDUCTOR, INC. | 5571374 | METHOD OF ETCHING SILICON CARB IDE |
| FREESCALE SEMICONDUCTOR, INC. | 5571734 | METHOD FOR FORMING A DIELECTRI C HAVING IMPROVED PERFORMANCE |
| FREESCALE SEMICONDUCTOR, INC. | 5572066 | LEAD-ON-CHIP SEMICONDUCTOR DEV ICE AND METHOD FOR ITS FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 5572467 | ADDRESS COMPARISON IN AN INTEG RATED CIRCUIT MEMORY |
| | | |

5574457

SWITCHED CAPACITOR GAIN STAGE

FREESCALE SEMICONDUCTOR, INC.

| Owner | Patent # | Description |
|-------------------------------|----------|--|
| FREESCALE SEMICONDUCTOR, INC. | 5574515 | VOLTAGE CONTROLLED OSCILLATOR CIRCUIT AND AUTOMATIC FINE TU NING CIRCUIT FOR TV |
| FREESCALE SEMICONDUCTOR, INC. | 5578167 | SUBSTRATE HOLDER AND METHOD OF USE |
| FREESCALE SEMICONDUCTOR, INC. | 5578860 | MONOLITHIC HIGH FREQUENCY INTE GRATED CIRCUIT STRUCTURE HAVIN G A GROUNDED SOURCE CONFIGURAT ION |
| FREESCALE SEMICONDUCTOR, INC. | 5579257 | METHOD FOR READING AND RESTORI NG DATA IN A DATA STORAGE ELEM ENT |
| FREESCALE SEMICONDUCTOR, INC. | 5579492 | DATA PROCESSING SYSTEM AND A M ETHOD FOR DYNAMICALLY IGNORING BUS TRANSFER TERMINATION CONTR OL SIGNALS FOR A PREDETERMINED AMOUNT OF TIME |
| FREESCALE SEMICONDUCTOR, INC. | 5580815 | PROCESS FOR FORMING FIELD ISOL ATION AND A STRUCTURE OVER A S EMICONDUCTOR SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 5581215 | VOLTAGE CONTROLLED OSCILLATOR HAVING FREQUENCY AND AMPLITUD E CONTROLLING LOOPS |
| FREESCALE SEMICONDUCTOR, INC. | 5581432 | CLAMP CIRCUIT AND METHOD FOR I DENTIFYING A SAFE OPERATING AR EA |
| FREESCALE SEMICONDUCTOR, INC. | 5581775 | A HISTORY BUFFER SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5583068 | PROCESS FOR FORMING A CAPACITO R HAVING A METAL-OXIDE DIELECT RIC |
| FREESCALE SEMICONDUCTOR, INC. | 5583350 | FULL COLOR LIGHT EMITTING DIOD E DISPLAY ASSEMBLY |
| FREESCALE SEMICONDUCTOR, INC. | 5583370 | TAB SEMICONDUCTOR DEVICE HAVIN G DIE EDGE PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 5583964 | COMPUTER UTILIZING NEURAL NETW ORK AND METHOD OF USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5584031 | SYSTEM AND METHOD FOR EXECUTIN G A LOW POWER DELAY INSTRUCTIO N |
| FREESCALE SEMICONDUCTOR, INC. | 5584059 | DC OFFSET REDUCTION IN A ZERO-IF TRANSMITTER |
| FREESCALE SEMICONDUCTOR, INC. | 5587342 | METHOD OF FORMING AN ELECTRICA L INTERCONNECT |
| FREESCALE SEMICONDUCTOR, INC. | 5589423 | PROCESS FOR FABRICATING A NON- SILICIDED REGION IN AN INTEGRA TED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5590232 | OPTIC PACKAGE AND METHOD OF MA KING |
| FREESCALE SEMICONDUCTOR, INC. | 5590241 | SPEECH PROCESSING SYSTEM AND M ETHOD FOR ENHANCING SPEECH SIG NALS IN A NOISY ENVIRONMENT |
| FREESCALE SEMICONDUCTOR, INC. | 5592025 | PAD ARRAY SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5592493 | SERIAL SCAN CHAIN ARCHITECTURE FOR A DATA PROCESSING SYSTEM AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 5592634 | A ZERO-CYCLE MULTI-STATE BRANC H CACHE PREDICTION DATA PROCES SING SYSTEM AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 5593538 | METHOD FOR ETCHING A DIELECTRI C LAYER ON A SEMICONDUCTOR |
| FREESCALE SEMICONDUCTOR, INC. | 5593903 | METHOD OF FORMING CONTACT PADS FOR WAFER LEVEL TESTING AND B URN-IN OF SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5594273 | APPARATUS FOR PERFORMING WAFER LEVEL-TESTING OF INTEGRATED CI RCUITS WHERE TESTPADS LIE WITH IN INTEGRATED CIRCUIT DIE BUT OVERLY NO ACTIVE CIRCUITRY FOR IMPROVED YIELD |
| FREESCALE SEMICONDUCTOR, INC. | 5595602 | DIFFUSER FOR UNIFORM GAS DISTR IBUTION IN SEMICONDUCTOR PROCE SSING AND METHOD FOR USING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5597110 | METHOD FOR FORMING A SOLDER BU MP BY SOLDER-TETTING OR THE LI KE |
| FREESCALE SEMICONDUCTOR, INC. | 5597737 | METHOD FOR TESTING AND BURNING -IN A SEMICONDUCTOR WAFER |
| FREESCALE SEMICONDUCTOR, INC. | 5597768 | METHOD OF FORMING A GA203 DIEL ECTRIC LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 5598362 | APPARATUS AND METHOD FOR PERFO RMING BOTH 24 BIT AND 16 BIT A RITHMETIC |
| FREESCALE SEMICONDUCTOR, INC. | 5598550 | CACHE CONTROLLER FOR PROCESSIN G SIMULTANEOUS CACHE |

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| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 5598569 | DATA PROCESSOR HAVING OPERATIN G MODES SELECTED BY AT LEAST O NE MASK OPTION BIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5600071 | VERTICALLY INTEGRATED SENSOR S TRUCTURE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5602491 | INTEGRATED CIRCUIT TESTING BOA RD HAVING CONSTRAINED THERMAL EXPANSION CHARACTERISTICS |
| FREESCALE SEMICONDUCTOR, INC. | 5604160 | METHOD FOR PACKAGING SEMICONDU CTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 5605615 | METHOD AND APPARATUS FOR PLATI NG METALS |
| FREESCALE SEMICONDUCTOR, INC. | 5605865 | METHOD FOR FORMING SELF-ALIGNE D SILICIDE IN A SEMICONDUCTOR DEVICE USING VAPOR PHASE REACT ION |
| FREESCALE SEMICONDUCTOR, INC. | 5606275 | BUFFER CIRCUIT HAVING VARIABLE OUTPUT IMPEDANCE |
| FREESCALE SEMICONDUCTOR, INC. | 5606319 | METHOD AND APPARATUS FOR INTER POLATION AND NOISE SHAPING IN A SIGNAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 5606682 | DATA PROCESSOR WITH BRANCH TAR GET ADDRESS CACHE AND SUBROUTI NE RETURN ADDRESS CACHE AND ME THOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 5608345 | PROGRAMMABLE SWITCHED CAPACITO R CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5608795 | TELEPHONE LINE INTERFACE CIRCU IT |
| FREESCALE SEMICONDUCTOR, INC. | 5610543 | DELAY LOCKED LOOP FOR DETECTIN G THE PHASE DIFFERENCE OF TWO SIGNALS HAVING DIFFERENT FREQU ENCIES |
| FREESCALE SEMICONDUCTOR, INC. | 5612232 | A METHOD OF FABRICATING SEMICO NDUCTOR DEVICES AND THE DEVICE S |
| FREESCALE SEMICONDUCTOR, INC. | 5612576 | SELF-OPENING VENT HOLE IN AN O VERMOLDED SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5612861 | METHOD AND APPARATUS FOR LOW V OLTAGE CMOS START CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5613119 | DATA PROCESSOR INITIALIZATION PROGRAM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5614131 | METHOD OF MAKING AN OPTO-ELECT RONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5614816 | LOW VOLTAGE REFERENCE CIRCUIT AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 5616886 | WIREBONDLESS MODULE PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 5617054 | SWITCHED CAPACITOR VOLTAGE ERR OR COMPENSATING CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5617348 | LOW POWER DATA TRANSLATION CIR CUIT AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 5617531 | DATA PROCESSOR HAVING A BUILT- IN INTERNAL SELF TEST CONTROLL ER FOR TESTING A PLURALITY OF MEMORIES INTERNAL TO THE DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 5619064 | III-V SEMICONDUCTOR GATE STRUC TURE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 5619156 | LOW VOLTAGE INHIBIT CIRCUIT AN D INTEGRATED CIRCUIT USING SAM E |
| FREESCALE SEMICONDUCTOR, INC. | 5619687 | QUEUE SYSTEM HAVING A TIME-OUT FEATURE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5623159 | INTEGRATED CIRCUIT ISOLATION S TRUCTURE FOR SUPPRESSING HIGH-FREQUENCY CROSS-TALK |
| FREESCALE SEMICONDUCTOR, INC. | 5623234 | CLOCK SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5623664 | AN INTERACTIVE MEMORY ORGANIZA TION SYSTEM AND METHOD THEREFO R |
| FREESCALE SEMICONDUCTOR, INC. | 5624854 | SEMICONDUCTOR DEVICE AND METHO D OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 5625224 | METHOD AND APPARATUS FOR AN IN TEGRATED CIRCUIT CHIP CARRIER HAVING IMPROVED MOUNTING PAD D ENSITY |
| EDEEGGALE GELUGONDUGEOD ING | E CO E 100 | CURCUIT AND ACTIVOD FOR MODAL ATLANCE CURCUIT BY OCCUR FOR DEDIVING |

POWER DISSIPATION

CIRCUIT AND METHOD FOR ISOLATI NG CIRCUIT BLOCKS FOR REDUCING

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| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 5627890 | TELEPHONE LINE INTERFACE CIRCU IT |
| FREESCALE SEMICONDUCTOR, INC. | 5628026 | MULTI-DIMENSIONAL DATA TRANSFE R IN A DATA PROCESSING SYSTEM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5628862 | POLISHING PAD FOR CHEMICAL-MEC HANICAL POLISHING OF A SEMICON DUCTOR SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 5628922 | ELECTRICAL FLAME-OFF WAND |
| FREESCALE SEMICONDUCTOR, INC. | 5629630 | SEMICONDUCTOR WAFER CONTACT SY STEM AND METHOD FOR CONTACTING A SEMICONDUCTOR WAFER |
| FREESCALE SEMICONDUCTOR, INC. | 5629643 | FEEDBACK LATCH AND METHOD THER EFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5630228 | DOUBLE BALANCE MIXER CIRCUIT W ITH ACTIVE FILTER LOAD FOR A P ORTABLE COMMUNICATION RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 5631178 | METHOD FOR MANUFACTURING A STA BLE ARSENIC DOPED SEMICONDUCTO R DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5631192 | SEMICONDUCTOR DEVICE ON AN OPP OSED LEADFRAME AND METHOD FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 5631492 | A STANDARD CELL HAVING A GROUN D CAPACITOR AND A POWER SUPPLY CAPACITOR FOR REDUCING NOISE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 5631548 | POWER OFF-LOADING CIRCUIT AND METHOD FOR DISSIPATING POWER |
| FREESCALE SEMICONDUCTOR, INC. | 5633186 | PROCESS FOR FABRICATING A NON- VOLATILE MEMORY CELL IN A SEMI CONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5633640 | METHOD AND APPARATUS FOR A DAT A CONVERTER WITH A SINGLE OPER ATIONAL AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 5635767 | SEMICONDUCTOR DEVICE HAVING BU ILT-IN HIGH FREQUENCY BYPASS C APACITOR AND METHOD FOR ITS FA BRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 5636228 | SCAN REGISTER WITH DECOUPLED S CAN ROUTING |
| FREESCALE SEMICONDUCTOR, INC. | 5637834 | MULTILAYER CIRCUIT SUBSTRATE AND METOD FOR FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5638020 | SWITCHED CAPACITOR DIFFERENTIA L CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 5639683 | STRUCTURE AND METHOD FOR INTER GRATING MICROWAVE COMPONENTS O N A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 5639687 | METHOD AND STRUCTURE FOR FORMING AN INTEGRATED CIRCUIT PATTE RN ON A SEMICONDUCTOR SUBSTRAT E |
| FREESCALE SEMICONDUCTOR, INC. | 5639695 | LOW-PROFILE BALL-GRID ARRAY SE MICONDUCTOR PACKAGE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5639989 | SHIELDED ELECTRONIC COMPONENT ASSEMBLY AND METHOD FOR MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5640460 | AMPLITUDE ADJUST CIRCUIT AND M ETHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 5640681 | BOOT-STRAPPED CASCODE CURRENT MIRROR |
| FREESCALE SEMICONDUCTOR, INC. | 5641695 | METHOD OF FORMING A SILICON CA RBIDE JFET |
| FREESCALE SEMICONDUCTOR, INC. | 5641712 | METHOD AND STRUCTURE FOR REDUC ING CAPACITANCE BETWEEN INTERC ONNECT LINES |
| FREESCALE SEMICONDUCTOR, INC. | 5642305 | LOGARITHM/INVERSE-LOGARITHM CO NVERTER AND METHOD OFUSING SAM E |
| FREESCALE SEMICONDUCTOR, INC. | 5642480 | METHOD AND APPARATUS FOR ENHAN CED SECURITY OF A DATA PROCESS OR |
| FREESCALE SEMICONDUCTOR, INC. | 5643405 | METHOD FOR POLISHING A SEMICON DUCTOR SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 5644519 | METHOD AND APPARATUS FOR A MUL TIPLY AND ACCUMULATE CIRCUIT H AVING A DYNAMIC SATURATION RAN GE |
| FREESCALE SEMICONDUCTOR, INC. | 5644528 | NON-VOLATILE MEMORY HAVING A CELL APPLYING TO MULTI-BIT DATA BY MULTI-LAYERED FLOATING GATE ARCHITECTURE AND PROGRAM MING METHOD FOR THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5644756 | INTEGRATED CIRCUIT DATA PROCES SOR WITH SELECTABLE ROUTING OF DATA ACCESSES |
| FREESCALE SEMICONDUCTOR, INC. | 5646055 | METHOD FOR MAKING BIPOLAR TRAN SISTOR |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 5646060 | METHOD FOR MAKING AN EEPROM CE LL WITH ISOLATION TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 5646550 | HIGH RELIABILITY OUTPUT BUFFER FOR MULTIPLE VOLTAGE SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5646946 | APPARATUS AND METHOD FOR SELEC TIVELY COMPANDING DATA ON A SL OT-BY-SLOT BASIS |
| FREESCALE SEMICONDUCTOR, INC. | 5646949 | METHOD AND APPARATUS FOR GENER ATING INSTRUCTIONS FOR USE IN TESTING A MICROPROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 5647123 | IMPROVED METHOD FOR UNDERFILLI NG EUTECTIC BUMPED FLIP CHIP D IE |
| FREESCALE SEMICONDUCTOR, INC. | 5649125 | METHOD AND APPARATUS FOR PROVI DING VALID ADDRESSES ACROSS A MULTIPLEXED COMMUNICATIONS BUS |
| FREESCALE SEMICONDUCTOR, INC. | 5650749 | FM DEMODULATOR USING INJECTION LOCKED OSCILLATOR HAVING TUNING FEEDBACK AND LINEARIZING FE EDBACK |
| FREESCALE SEMICONDUCTOR, INC. | 5652844 | FLEXIBLE PIN CONFIGURATION FOR USE IN A DATA PROCESSING SYST EMDURING A RESET OPERATION AN D METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5654588 | APPARATUS FOR PERFORMING WAFER LEVEL TESTING OF INTEGRATED COROUTS WHERE THE WAFER USES A SEGMENTED CONDUCTIVE TOPLAYER BUS STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 5655042 | MOLDED SLOTTED OPTICAL SWITCH STRUCTURE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5656549 | METHOD OF PACKAGING A SEMICOND UCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5656844 | SEMICONDUCTOR-ON-INSULATOR TRA NSISTOR HAVING A DOPING PROFIL E FOR FULLY-DEPLETED OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 5656943 | APPARATUS FOR FORMING A TEST S TACK FOR SEMICONDUCTOR WAFER ROBING AND METHOD FOR USING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5656951 | INPUT CIRCUIT AND METHOD FOR H OLDING DATA IN MIXED POWER SU PPLY MODE |
| FREESCALE SEMICONDUCTOR, INC. | 5657324 | BIDIRECTIONAL COMMUNICATION SY STEM |
| FREESCALE SEMICONDUCTOR, INC. | 5658810 | METHOD FOR MAKING A SENSOR FOR DETERMINING A RATIO OF MATERI ALS IN A MIXTURE |
| FREESCALE SEMICONDUCTOR, INC. | 5659648 | POLYIMIDE OPTICAL WAVEGUIDE HA VING ELECTRICAL CONDUCTIVITY |
| FREESCALE SEMICONDUCTOR, INC. | 5659698 | METHOD AND APPARATUS FOR GENER ATING A CIRCULAR BUFFER ADDRES S IN INTEGRATED CIRCUIT THAT P ERFORMS MULTIPLE COMMUNICATION TASKS |
| FREESCALE SEMICONDUCTOR, INC. | 5659950 | ELECTRONIC DIE PACKAGE ASSEMBL Y HAVING A SUPPORT AND METHOL |
| FREESCALE SEMICONDUCTOR, INC. | 5661042 | PROCESS FOR ELECTRICALLY CONNE CTING ELECTRICAL DEVICES USING A CONDUCTIVE ANISDTROPIC MATE RIAL |
| FREESCALE SEMICONDUCTOR, INC. | 5661082 | SEMICONDUCTOR DEVICE HAVING A BOND PAD AND A PROCESS FOR FOR MING THE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5661088 | ELECTRONIC COMPONENT AND METHO D OF PACKAGING |
| FREESCALE SEMICONDUCTOR, INC. | 5661312 | SILICON CARBIDE MOSFET |
| FREESCALE SEMICONDUCTOR, INC. | 5663690 | CONSTANT HIGH Q VOLTAGE CONTRO LLED OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | 5664168 | METHOD AND APPARATUS IN A DATA PROCESSING SYSTEM FOR SELECTI VELY INSERTING BUS CYCLE IDLE TIME |
| FREESCALE SEMICONDUCTOR, INC. | 5665202 | MULTI-STEP PLANARIZATION PROCE SS |
| FREESCALE SEMICONDUCTOR, INC. | 5665633 | SEMICONDUCTOR DEVICE HAVING FI ELD ISOLATION AND A PROCESS FO R FORMING THE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5665658 | METHOD OF FORMING A DIELECTRIC LAYER STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 5666509 | A DATA PROCESSING SYSTEM FOR P ERFORMING EITHER A PRECISE MEM ORY ACCESS OR AN IMPRECISE MEM ORY ACCESS BASED UPON A LOGICAL L ADDRESS VALUE AND METHOD THE REOF |
| EDEECCALE CEMICONDUCTOR INC | ECCE100 | MODIZETATION FOR PROCECCING A FIFTURE MEMBRANCE |

WORKSTATION FOR PROCESSING A F LEXIBLE MEMBRANCE

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| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 5667632 | METHOD OF DEFINING A LINE WIDT H |
| FREESCALE SEMICONDUCTOR, INC. | 5668021 | PROCESS FOR FABRICATING A SEMI CONDUCTOR DEVICE HAVING A SEGM ENTED CHANNEL REGION |
| FREESCALE SEMICONDUCTOR, INC. | 5670389 | SEMICONDUCTOR-ON-INSULATOR DEV ICE HAVING A LATERALLY-GRADED CHANNEL REGION AND METHOD OF M AKING |
| FREESCALE SEMICONDUCTOR, INC. | 5670829 | PRECISION CURRENT LIMIT CIRCUI T |
| FREESCALE SEMICONDUCTOR, INC. | 5673001 | METHOD AND APPARATUS FOR AMPLI FYING A SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 5673396 | ADJUSTABLE DEPTH/WIDTH FIFO BU FFER FOR VARIABLE WIDTH DATA T RANSFERS |
| FREESCALE SEMICONDUCTOR, INC. | 5674762 | METHOD OF FABRICATING AN EPROM WITH HIGH VOLTAGE TRANSISTORS |
| FREESCALE SEMICONDUCTOR, INC. | 5674780 | METHOD OF FORMING AN ELECTRICA LLY CONDUCTIVE POLYMER BUMP OV ER AN ALUMINUM ELECTRODE |
| FREESCALE SEMICONDUCTOR, INC. | 5675166 | FET WITH STABLE THRESHOLD VOLT AGE AND METHOD OF MANUFACTURIN G THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5675243 | VOLTAGE SOURCE DEVICE FOR LOW- VOLTAGE OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 5675469 | INTEGRATED CIRCUIT WITH ELECTR OSTATIC DISCHARGE (ESD) PROTEC TION AND ESD PROTECTION CIRCUI T |
| FREESCALE SEMICONDUCTOR, INC. | 5675822 | METHOD AND APPARATUS FOR A DIG ITAL SIGNAL PROCESSOR HAVING A MULTIPLIERLESS COMPUTATION BLO CK |
| FREESCALE SEMICONDUCTOR, INC. | 5677917 | INTEGRATED CIRCUIT MEMORY USIN G FUSIBLE LINKS IN A SCAN CHAI N |
| FREESCALE SEMICONDUCTOR, INC. | 5679275 | CIRCUIT AND METHOD OF MODIFYIN G CHARACTERISTICS OF A UTILIZA TION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5680626 | METHOD AND APPARATUS FOR PROVI DING ONLY THAT NUMBER OF CLOCK PULSES NECESSARY TO COMPLETE A TASK |
| FREESCALE SEMICONDUCTOR, INC. | 5682340 | LOW POWER CONSUMPTION CIRCUIT AND METHOD OF OPERATION FOR IM PLEMENTING SHIFTS AND BIT REVE RSALS |
| FREESCALE SEMICONDUCTOR, INC. | 5683569 | METHOD OF SENSING A CHEMICAL A ND SENSOR THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5683934 | ENHANCED MOBILITY MOSFET DEVIC E AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5683944 | METHOD OF FABRICATING A THERMA LLY ENHANCED LEAD FRAME |
| FREESCALE SEMICONDUCTOR, INC. | 5684928 | CIRCUIT AND METHOD FOR EVALUAT ING FUZZY LOGIC RULES |
| FREESCALE SEMICONDUCTOR, INC. | 5686698 | PACKAGE FOR ELECTRICAL COMPONE NTS AND METHOD FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 5686860 | AMPLIFIER AND CONTROLLING APPA RATUS OPERATING FROM A UNIPOLA R POWER SUPPLY |
| FREESCALE SEMICONDUCTOR, INC. | 5687104 | METHOD AND APPARATUS FOR GENER ATING DECOUPLED FILTER PARAMET ERS AND IMPLEMENTING A BAND DE COUPLED FILTER |
| FREESCALE SEMICONDUCTOR, INC. | 5689714 | METHOD AND APPARATUS FOR PROVI DING LOW POWER CONTROL OF PERI PHERAL DEVICES USING THE REGIS TER FILE OF A MICROPROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 5691242 | METHOD FOR MAKING AN ELECTRONI C COMPONENT HAVING AN ORGANIC SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 5691253 | PROCESS FOR POLISHING AND ANAL YZING AN EXPOSED SURFACE OF A PATTERNED SEMICONDUCTOR SUBSTR ATE |
| FREESCALE SEMICONDUCTOR, INC. | 5691554 | PROTECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5693545 | METHOD FOR FORMING A SEMICONDU CTOR SENSOR FET DEVICE AND SEM ICONDUCTOR SENSOR FET DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5693955 | TUNNEL TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 5693966 | POWER MOS TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 5694308 | METHOD AND APPARATUS FOR A REG ULATED LOW VOLTAGE CHARGE PUMP |
| FREESCALE SEMICONDUCTOR, INC. | 5694344 | A METHOD FOR ELECTRICALLY MODE LING A SEMICONDUCTOR |

PACKAGE

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 5695877 | METHOD OF DEPOSITING FERRITE FILM (AS AMEMDED) |
| FREESCALE SEMICONDUCTOR, INC. | 5696666 | LOW PROFILE EXPOSED DIE CHIP CARRIER PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 5697088 | BALUN TRANSFORMER |
| FREESCALE SEMICONDUCTOR, INC. | 5699309 | METHOD AND APPARATUS FOR PROVI DING USER SELECTABLE LOW POWER AND HIGH PERFORMANCE MEMORY A CCESS MODES |
| FREESCALE SEMICONDUCTOR, INC. | 5699422 | TELECOMMUNICATIONS DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5702981 | METHOD FOR FORMING A VIA IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5703405 | INTEGRATED CIRCUIT CHIP FORMED FROM PROCESSING TWO OPPOSING SURFACES OF A WAFER |
| FREESCALE SEMICONDUCTOR, INC. | 5703478 | CURRENT MIRROR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5703808 | NON-VOLATILE MEMORY CELL AND M ETHOD OF PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | 5704034 | METHOD AND CIRCUIT FOR INITIAL IZING A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5706036 | METHOD AND APPARATUS FOR PROVI DING A VIDEO SYNCHRONISING SIG NAL OF A PREDETERMINED POLARIT Y |
| FREESCALE SEMICONDUCTOR, INC. | 5706228 | METHOD FOR OPERATING A MEMORY ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | 5707881 | A TEST STRUCTURE AND METHOD FO R PERFORMING BURN-IN TESTING O F A SEMICONDUCTOR PRODUCT WAFE R |
| FREESCALE SEMICONDUCTOR, INC. | 5708288 | THIN FILM SILICON ON INSULATOR SEMICONDUCTOR INTEGRATED CIRC UIT WITH ELECTROSTATIC DAMAGE PROTECTION AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5708839 | METHOD AND APPARATUS FOR PROVI DING BUS PROTOCOL SIMULATION |
| FREESCALE SEMICONDUCTOR, INC. | 5710071 | PROCESS FOR UNDERFILLING A FLI P-CHIP SEMICONDUCTOR DEVICE AN D A DEVICE MADE THEREBY |
| FREESCALE SEMICONDUCTOR, INC. | 5712208 | METHODS OF FORMATION OF SEMICO NDUCTOR COMPOSITE GATE DIELECT RIC HAVING MULTIPLE INCORPORAT ED ATOMIC DOPANTS |
| FREESCALE SEMICONDUCTOR, INC. | 5712589 | APPARATUS AND METHOD FOR PERFO RMING ADAPTIVE POWER REGULATIO N FOR AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5712794 | AUTOMATED METHOD FOR ADDING AT TRIBUTES IDENTIFIED ON A SCHEM ATIC DIAGRAM TO AN INTEGRATED CIRCUIT LAYOUT |
| FREESCALE SEMICONDUCTOR, INC. | 5714792 | SEMICONDUCTOR DEVICE HAVING A REDUCED DIE SUPPORT AREA AND M ETHOD FOR MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5714800 | INTEGRATED CIRCUIT ASSEMBLY HA VING A STEPPED INTERPOSER AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5715014 | CIRCUIT AND METHOD OF PROVIDIN G PARENTAL DISCRETIONARY CONTR OL ON A PIP IC |
| FREESCALE SEMICONDUCTOR, INC. | 5715184 | METHOD OF PARALLEL SIMULATION OF STANDARD CELLS ON A DISTRIB UTED COMPUTER |
| FREESCALE SEMICONDUCTOR, INC. | 5716866 | METHOD OF FORMING A SEMICONDUC TOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5716875 | METHOD FOR MAKING A FERROELECT RIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5717700 | METHOD OF CONSTRUCTION OF A SC ANNABLE INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5717772 | METHOD AND APPARATUS FOR SUPPR ESSING ACOUSTIC FEEDBACK IN AN AUDIO SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5717931 | METHOD AND APPARATUS FOR COMMU NICATING BETWEEN MASTER AND SL AVE ELECTRONIC DEVICES WHERE T HE SLAVE DEVICE MAY BE HAZARDO US |
| FREESCALE SEMICONDUCTOR, INC. | 5719519 | CIRCUIT AND METHOD FOR RECONST RUCTING A PHASE CURRENT |
| FREESCALE SEMICONDUCTOR, INC. | 5719856 | TRANSMITTER/RECEIVER INTERFACE APPARATUS AND METHOD FOR A BI -DIRECTIONAL TRANSMISSION PATH |
| FREESCALE SEMICONDUCTOR, INC. | 5719878 | SCANNABLE STORAGE CELL AND MET HOD OF OPERATION |

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 5720100 | ASSEMBLY HAVING A FRAME EMBEDD ED IN A POLYMERIC ENCAPSULANT AND METHOD FOR FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5721438 | HETEROJUNCTION SEMICONDUCTOR D EVICE AND METHOD OF MANUFACTUR E |
| FREESCALE SEMICONDUCTOR, INC. | 5721450 | MOISTURE RELIEF FOR CHIP CARRIERS |
| FREESCALE SEMICONDUCTOR, INC. | 5721451 | INTEGRATED CIRCUIT ASSEMBLY AD HESIVE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 5721509 | CHARGE PUMP HAVING REDUCED THR ESHOLD VOLTAGE LOSSES |
| FREESCALE SEMICONDUCTOR, INC. | 5721704 | CONTROL GATE DRIVER CIRCUIT FO R A NON-VOLATILE MEMORY AND ME MORY USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5721889 | DATA TRANSFER BETWEEN INTEGRAT ED CIRCUIT TIMER CHANNELS |
| FREESCALE SEMICONDUCTOR, INC. | 5724283 | DATA STORAGE ELEMENT AND METHO D FOR RESTORING DATA |
| FREESCALE SEMICONDUCTOR, INC. | 5724604 | DATA PROCESSING SYSTEM FOR ACC ESSING AN EXTERNAL DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5725788 | APPARATUS AND METHOD FOR PATTE RNING A SURFACE |
| FREESCALE SEMICONDUCTOR, INC. | 5726087 | METHOD OF FORMATION OF SEMICON DUCTOR GATE DIELECTRIC |
| FREESCALE SEMICONDUCTOR, INC. | 5726502 | BUMPED SEMICONDUCTOR DEVICE WI TH ALIGNMENT FEATURES AND METH OD FOR MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5726944 | VOLTAGE REGULATOR FOR REGULATI NG AN OUTPUT VOLTAGE FROM A CH ARGE PUMP AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5727038 | PHASE LOCKED LOOP USING DIGITA L LOOP FILTER AND DIGITALLY CONTROLLED OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | 5727172 | METHOD AND APPARATUS FOR PERFO RMING ATOMIC ACCESSES IN A DATA A PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5729151 | SYSTEM AND METHOD FOR TESTING A PHASE LOCKED LOOP IN AN INTE GRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5729176 | LINEAR DIFFERENTIAL GAIN STAGE |
| FREESCALE SEMICONDUCTOR, INC. | 5729223 | METHOD AND APPARATUS FOR DATA COMPRESSION AND RESTORATION |
| FREESCALE SEMICONDUCTOR, INC. | 5729225 | METHOD AND APPARATUS FOR ASYNC HRONOUS DIGITAL MIXING |
| FREESCALE SEMICONDUCTOR, INC. | 5729438 | DISCRETE COMPNENT PAD ARRAY CARRIER |
| FREESCALE SEMICONDUCTOR, INC. | 5729493 | MEMORY SUITABLE FOR OPERATION AT LOW POWER SUPPLY VOLTAGES AND SENSE AMPLIFIER THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5729577 | SIGNAL PROCESSOR WITH IMPROVED EFFICIENCY |
| FREESCALE SEMICONDUCTOR, INC. | 5729721 | TIMEBASE SYNCHRONIZATION IN SE PARATE INTEGRATED CIRCUITS OR SEPARATE MODULES |
| FREESCALE SEMICONDUCTOR, INC. | 5731709 | METHOD FOR TESTING A BALL GRID ARRAY SEMICONDUCTOR DEVICE AN D A DEVICE FOR SUCH TESTING |
| FREESCALE SEMICONDUCTOR, INC. | 5731769 | MULTI-RATE DIGITAL FILTER APPA RATUS AND METHOD FOR SIGMA-DEL TA CONVERSION PROCESSES |
| FREESCALE SEMICONDUCTOR, INC. | 5732225 | INTEGRATED CIRCUIT TIMER SYSTE M HAVING A GLOBAL BUS FOR TRAN SFERRING INFORMATION BETWEEN L OCAL BUSES |
| FREESCALE SEMICONDUCTOR, INC. | 5732405 | METHOD AND APPARATUS FOR PERFO RMING A CACHE OPERATION IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5733794 | PROCESS FOR FORMING A SEMICOND UCTOR DEVICE WITH ESD PROTECTS ON |
| FREESCALE SEMICONDUCTOR, INC. | 5733806 | METHOD FOR FORMING A SELF-ALIG NED SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5734201 | LOW PROFILE SEMICONDUCTOR DEVI CE AND METHOD FOR MAKING THE S AME |
| FREESCALE SEMICONDUCTOR, INC. | 5734317 | CURRENT LIMIT CONTROLLER FOR A N AIR BAG DEPLOYMENT SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5737254 | SYMMETRICAL FILTERING APPARATU S AND METHOD THEREFOR |

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| FREESCALE SEMICONDUCTOR, INC. | 5737516 | DATA PROCESSING SYSTEM FOR PER FORMING A DEBUG FUNCTION AND M ETHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5737584 | DATA PROCESSING SYSTEM HAVING PROGRAMMABLE EXTERNAL TERMINAL S SUCH THAT THE EXTERNAL TERMI NALS ARE SELECTIVELY SUBJECTED TO BUS ARBITRATION |
| FREESCALE SEMICONDUCTOR, INC. | 5737760 | MICROCONTROLLER WITH SECURITY LOGIC CIRCUIT WHICH PREVENTS F EADING OF INTERNAL MEMORY BY E XTERNAL PROGRAM |
| FREESCALE SEMICONDUCTOR, INC. | 5737768 | METHOD AND SYSTEM FOR STORING DATA BLOCKS IN A MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5739557 | REFRACTORY GATE HETEROSTRUCTUR E FIELD EFFECT TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 5740109 | NON-LINEAR CHARGE PUMP |
| FREESCALE SEMICONDUCTOR, INC. | 5740325 | COMPUTER UTILIZING NEURAL NETW ORK AND METHOD OF USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5740382 | METHOD AND APPARATUS FOR ACCES SING A CHIP-SELECTABLE DEVICE IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5740417 | PIPELINED PROCESSOR OPERATING IN DIFFERENT POWER MODE BASED ON BRANCH PREDICTION STATE OF BRANCH HISTORY BIT ENCODED AS TAKEN WEAKLY NOT TAKEN AND STR ONGLY NOT TAKEN STATES |
| FREESCALE SEMICONDUCTOR, INC. | 5742007 | ELECTRONIC DEVICE PACKAGE AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5742100 | STRUCTURE HAVING FLIP-CHIP CON NECTED |
| FREESCALE SEMICONDUCTOR, INC. | 5742210 | NARROW-BAAND OVERCOPPLED DIREC TIONAL COUPLER IN MULTILAYER P ACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 5742799 | METHOD AND APPARATUS FOR SYNCHRONIZING MULTIPLE CLOCKS |
| FREESCALE SEMICONDUCTOR, INC. | 5744396 | A SEMICONDUCTOR DEVICE FORMED ON A HIGHLY DOPED N+ SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 5744841 | SEMICONDUCTOR DEVICE WITH ESD PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 5745411 | SEMICONDUCTOR MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5747839 | CHEMICAL SENSING TRENCH FIELD EFFECT TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 5747858 | ELECTRONIC COMPONENT HAVING AN INTERCONNECT SUBSTRATE ADJACE NT TO A SIDE SURFACE OF A DEVI CE SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 5748161 | INTEGRATED ELECTRO-OPTICAL PAC KAGE WITH INDEPENDENT MENU BAR |
| FREESCALE SEMICONDUCTOR, INC. | 5748475 | APPARATUS AND METHOD OF ORIENT ING ASYMMETRICAL SEMICONDUCTOR DEVICES IN A CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5748645 | SINGLE CLOCK SCAN DESIGN CIRCU IT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5748949 | COUNTER HAVING PROGRAMMABLE PE RIODS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5749090 | CACHE TAG RAM HAVING SEPARATE VALID BIT ARRAY WITH MULTIPLE STEP INVALIDATION AND METHOD T HEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5749614 | VACUUM PICKUP TOOL FOR PLACING BALLS IN A CUSTOMIZED PATTERN |
| FREESCALE SEMICONDUCTOR, INC. | 5750419 | PROCESS FOR FORMING A SEMICOND UCTOR DEVICE HAVING A FERROELE CTRIC CAPACITOR |
| FREESCALE SEMICONDUCTOR, INC. | 5750440 | APPARATUS AND METHOD FOR DYNAM ICALLY MIXING SLURRY FOR CHEMI CAL MECHANICAL POLISHING |
| FREESCALE SEMICONDUCTOR, INC. | 5751166 | INPUT BUFFER CIRCUIT AND METHO D . |
| FREESCALE SEMICONDUCTOR, INC. | 5751555 | ELECTRONIC COMPONENT HAVING RE DUCED CAPACITANCE |
| FREESCALE SEMICONDUCTOR, INC. | 5751938 | PERIPHERAL MODULE AND MICROPRO CESSOR SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5752077 | DATA PROCESSING SYSTEM HAVING A MULTI-FUNCTION INPUT/OUTPUT PORT WITH INDIVIDUAL PULL-UP A ND PULL-DOWN CONTROL |

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| FREESCALE SEMICONDUCTOR, INC. | 5753904 | TOOL FOR DETECTING MISSING BAL LS USING A PHOTODETECTOR |
| FREESCALE SEMICONDUCTOR, INC. | 5753929 | MULTI-DIRECTIONAL OPTOCOUPLER AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 5754010 | MEMORY CIRCUIT AND METHOD FOR SENSING DATA |
| FREESCALE SEMICONDUCTOR, INC. | 5754482 | MEMORY USING UNDECODED PRECHAR GE FOR HIGH SPEED DATA SENSING |
| FREESCALE SEMICONDUCTOR, INC. | 5754861 | DYNAMIC PROGRAM INPUT/OUTPUT D ETERMINATION |
| FREESCALE SEMICONDUCTOR, INC. | 5754879 | INTEGRATED CIRCUIT FOR EXTERNA L BUS INTERFACE HAVING PROGRAM MABLE MODE SELECT BY SELECTIVE LY BONDING ONE OF THE BOND PAD S TO A RESET TERMINAL VIA A CO NDUCTIVE WIRE |
| FREESCALE SEMICONDUCTOR, INC. | 5756380 | METHOD FOR MAKING A MOISTURE R ESISTANT SEMICONDUCTOR DEVICE HAVING AN ORGANIC SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 5757303 | MULTI-BIT A/D CONVERTER HAVING REDUCED CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | 5758107 | SYSTEM FOR OFFLOADING EXTERNAL BUS BY COUPLING PERIPHERAL DE VICE TO DATA PROCESSOR THROUGH INTERFACE LOGIC THAT EMULATE THE CHARACTERISTICS OF THE EXT ERNAL BUS |
| FREESCALE SEMICONDUCTOR, INC. | 5759910 | PROCESS FOR FABRICATING A SOLD ER BUMP FOR A FLIP CHIP INTEGR ATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5760459 | HIGH PERFORMANCE HIGH VOLTAGE NON-EPI BIPOLAR TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 5760489 | METHOD FOR TRANSMITTING SIGNAL S BETWEEN A MICROPORCESSOR AND AN INTERFACE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5760728 | INPUT STATE FOR AN ANALOG-TO-D ITIGAL CONVERTER AND METHOD OF OPERATION THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 5761215 | SCAN BASED PATH DELAY TESTING OF INTEGRATED CIRCUITS CONTAIN ING EMBEDDED MEMORY ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | 5761489 | METHOD AND APPARATUS FOR SCAN TESTING WITH EXTENDED TEST VEC TOR STORAGE IN A MULTI-PURPOSE MEMORY SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5761491 | DATA PROCESSING SYSTEM AND MET HOD FOR STORING AND RESTORING A STACK POINTER |
| FREESCALE SEMICONDUCTOR, INC. | 5761700 | ROM MAPPING AND INVERSION APPA RATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5763862 | DUAL CARD SMART CARD READER WI TH VISUAL IMAGE DISPLAY |
| FREESCALE SEMICONDUCTOR, INC. | 5764024 | PULSE WIDTH MODULATOR (PWM) SY STEM WITH LOW COST DEAD TIME D ISTORTION CORRECTION |
| FREESCALE SEMICONDUCTOR, INC. | 5765208 | METHOD OF SPECULATIVELY EXECUT ING STORE INSTRUCTIONS PRIOR T O PERFORMING SNOOP OPERATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 5765216 | DATA PROCESSOR WITH AN EFFICIE NT BIT MOVE CAPABILITY AND MET HOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5770849 | SMART CARD DEVICE WITH PAGER A ND VISUAL IMAGE DISPLAY |
| FREESCALE SEMICONDUCTOR, INC. | 5770965 | CIRCUIT AND METHOD OF COMPENSA TING FOR NON-LINEARITIES IN A SENSOR SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 5773083 | METHOD FOR COATING A SUBSTRATE WITH A COATING SOLUTION |
| FREESCALE SEMICONDUCTOR, INC. | 5773314 | PLUG PROTECTION PROCESS FOR US E IN THE MANUFACTURE OF EMBEDD ED DYNAMIC RANDOM ACCESS MEMOR Y (DRAM) CELLS |
| FREESCALE SEMICONDUCTOR, INC. | 5773326 | METHOD OF MAKING AN SOI INTEGR ATED CIRCUIT WITH ESD PROTECTI ON |
| FREESCALE SEMICONDUCTOR, INC. | 5773359 | INTERCONNECT SYSTEM AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 5773364 | METHOD FOR USING AMMONIUM SALT SLURRIES FOR CHEMICAL MECHANI CAL POLISHING (CMP) |
| FREESCALE SEMICONDUCTOR, INC. | 5773887 | HIGH FREQUENCY SEMICONDUCTOR C OMPONENT |
| FREESCALE SEMICONDUCTOR, INC. | 5773987 | METHOD FOR PROBING A SEMICONDU CTOR WAFER USING A MOTOR CONTR OLLED SCRUB PROCESS |

SEMICONDUCTOR PACKAGE AND METH OD THEREFOR

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| FREESCALE SEMICONDUCTOR, INC. | 5777361 | SINGLE GATE NONVOLATILE MEMORY CELL AND METHOD FOR ACCESSING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5777522 | ELECTRONIC DEVICE FOR CONTROLL ING A REACTANCE VALUE FOR A REACTIVE ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 5777935 | MEMORY DEVICE WITH FAST WRITE RECOVERY AND RELATED WRITE REC OVERY METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5780352 | METHOD OF FORMING AN ISOLATION OXIDE FOR SILICON-ON-INSULATO ITECHNOLOGY |
| FREESCALE SEMICONDUCTOR, INC. | 5780878 | LATERAL GATE VERTICAL DRIFT RE GION TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 5781480 | PIPELINED DUAL PORT INTEGRATED CIRCUIT MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 5781566 | CYCLIC REDUNDANCY CODER |
| FREESCALE SEMICONDUCTOR, INC. | 5781765 | SYSTEM FOR DATA SYNCHRONIZATIO N BETWEEN TWO DEVICES USING FO UR TIME DOMAINS |
| FREESCALE SEMICONDUCTOR, INC. | 5784427 | FEEDBACK AND SHIFT UNIT |
| FREESCALE SEMICONDUCTOR, INC. | 5786230 | METHOD OF FABRICATING MULTI-CH IP PACKAGES |
| FREESCALE SEMICONDUCTOR, INC. | 5786263 | METHOD FOR FORMING A TRENCH IS OLATION STRUCTURE IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5786608 | A SEMICONDUCTOR CHEMICAL SENSO R WITH SPECIFIC HEATER STRUCTU RE |
| FREESCALE SEMICONDUCTOR, INC. | 5787125 | METHOD AND APPARATUS FOR DERIV ING IN-PHASE AND QUADRATURE-PH ASE BASEBAND SIGNALS FROM A CO MMUNICATION SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 5789733 | SMART CARD WITH CONTACTLESS OP TICAL INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | 5789766 | LED ARRAY WITH STACKED DRIVER CIRCUITS AND METHODS OF MANUFA CTURE |
| FREESCALE SEMICONDUCTOR, INC. | 5789815 | THREE DIMENSIONAL SEMICONDUCTO R PACKAGE HAVING FLEXIBLE APPE NDAGES AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5789973 | RESISTORLESS OPERATIONAL TRANS CONDUCTANCE AMPLIFIER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5790728 | OPTICAL COUPLING COMPONENT AND METHOD OF MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5792594 | METALLIZATION AND TERMINATION PROCESS FOR AN INTEGRATED CIRC UIT CHIP |
| FREESCALE SEMICONDUCTOR, INC. | 5796391 | SCALEABLE REFRESH DISPLAY CONT ROLLER |
| FREESCALE SEMICONDUCTOR, INC. | 5796682 | METHOD FOR MEASURING TIME AND STRUCTURE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5796993 | METHOD AND APPARATAUS FOR SEMI CONDUCTOR DEVICE OPTIMIZATION USING ON-CHIP VERIFICATION |
| FREESCALE SEMICONDUCTOR, INC. | 5798556 | SENSOR AND METHOD OF FABRICATI ON |
| FREESCALE SEMICONDUCTOR, INC. | 5798937 | METHOD AND APPARATUS FOR FORMI NG REDUNDANT VIAS BETWEEN COND UCTIVE LAYERS OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5799049 | PHASE-INDEPENDENT CLOCK CIRCUI T AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5799160 | CIRCUIT AND METHOD FOR CONTROL LING BUS ARBITRATION |
| FREESCALE SEMICONDUCTOR, INC. | 5800747 | METHOD FOR MOLDING USING AN IO N IMPLANTED MOLD |
| FREESCALE SEMICONDUCTOR, INC. | 5801108 | LOW TEMPERATURE COFIREABLE DIELECTRIC PASTE AND METHOD OF FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5801523 | CIRCUIT AND METHOD OF PROVIDIN G A CONSTANT CURRENT |
| FREESCALE SEMICONDUCTOR, INC. | 5801552 | VOLTAGE DETECTOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5801798 | FAST SPEED LIQUID CRYSTAL PHAS E SPATIAL LIGHT MODULATOR FOR ENHANCED DISPLAY RESOLUTION |

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| FREESCALE SEMICONDUCTOR, INC. | 5801799 | MULTI-DIRECTIONAL LIQUID CRYST AL PHASE SPATIAL LIGHT MODULAT OR FOR ENHANCED DISPLAY RESOLU TION |
| FREESCALE SEMICONDUCTOR, INC. | 5801987 | AUTOMATIC TRANSITION CHARGE PU MP FOR NON-VOLATILE MEMORIES |
| FREESCALE SEMICONDUCTOR, INC. | 5802317 | ELECTRONIC CIRCUIT HAVING CASC ADED LOGIC BUSSES |
| FREESCALE SEMICONDUCTOR, INC. | 5802541 | METHOD AND APPARATUS IN A DATA PROCESSING SYSTEM FOR USING C HIP SELECTS TO PERFORM A MEMOR Y MANAGEMENT FUNCTION |
| FREESCALE SEMICONDUCTOR, INC. | 5804881 | METHOD AND ASSEMBLY FOR PROVID ING INPROVED UNDERCHIP ENCAPSU LATION |
| FREESCALE SEMICONDUCTOR, INC. | 5804958 | SELF-REFERENCED CONTROL CIRCUI T |
| FREESCALE SEMICONDUCTOR, INC. | 5804985 | PROGRAMMABLE OUTPUT BUFFER AND METHOD FOR PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | 5806365 | ACCELERATION SENSING DEVICE ON A SUPPORT SUBSTRATE AND METHO D OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 5808362 | INTERCONNECT STRUCTURE AND MET HOD OF FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 5808873 | ELECTRONIC COMPONENT ASSEMBLY HAVING AN ENCAPSULATION MATERI AL AND METHOD OF FORMING THE S AME |
| FREESCALE SEMICONDUCTOR, INC. | 5809530 | METHOD AND APPARATUS FOR EFFIC IENTLY PROCESSING MULTIPLE CAC HE MISSES |
| FREESCALE SEMICONDUCTOR, INC. | 5809532 | DATA PROCESSOR WITH CACHE AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 5812561 | SCAN BASED TESTING OF AN INTEG RATED CIRCUIT FOR COMPLIANCE W ITH TIMING SPECIFICATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 5812595 | WAVEFORM SHAPING CIRCUIT FOR A MULTIPLEXED INFOMRATION BUS T RANSMITTER |
| FREESCALE SEMICONDUCTOR, INC. | 5812831 | METHOD AND AAPRATUS FOR PULSE WIDTH MODULATION |
| FREESCALE SEMICONDUCTOR, INC. | 5812833 | TIMER BUS STRUCTURE FOR AN INT EGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5812868 | METHOD AND APPARATUS FOR SELEC TING A REGISTER FILE IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5813041 | METHOD FOR ACCESSING MEMORY BY ACTIVATING A PROGRAMMABLE CHI F SELECT SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 5814401 | SELECTIVELY FILLED ADHESIVE FILM CONTAINING A FLUXING AGENT |
| FREESCALE SEMICONDUCTOR, INC. | 5814545 | METHOD OF MANUFACTURE A SEMICO NDUCTOR DEVICE HAVING A PHOSPH ORUS DOPED PECVD FILM |
| FREESCALE SEMICONDUCTOR, INC. | 5814727 | SEMICONDUCTOR ACCELEROMETER HA VING REDUCED SENSOR PLATE FLEX URE |
| FREESCALE SEMICONDUCTOR, INC. | 5814733 | METHOD OF CHARACTERIZING DYNAM ICS OF A WORKPIECE HANDLING SY STEM |
| FREESCALE SEMICONDUCTOR, INC. | 5814893 | SEMICONDUCTOR DEVICE HAVING A BOND PAD |
| FREESCALE SEMICONDUCTOR, INC. | 5815017 | FORCED OSCILLATOR CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5816478 | FLUXLESS FLIP-CHIP BOND AND A METHOD FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 5818276 | NON-OVERLAPPING CLOCK GENERATO R CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5819305 | METHOD AND APPARATUS FOR CONFI GURING OPERATING MODES IN A ME MORY |
| FREESCALE SEMICONDUCTOR, INC. | 5821160 | METHOD FOR FORMING A LASER REP AIRABLE FUSE AREA OF A MEMORY CELL USING AN ETCH STOP LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 5821168 | PROCESS FOR FORMING A SEMICOND UCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5821170 | METHOD OF REMOVING ETCHING AN INSULATING MATERIAL |
| FREESCALE SEMICONDUCTOR, INC. | 5821456 | MICROELECTRONIC ASSEMBLY INCLU DING A DECOMPOSABLE ENCAPSULAN T, AND METHOD FOR FORMING AND REWORKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5822764 | METHOD AND CIRCUIT FOR EFFICIE NTLY REPLACING INVALID LOCKED PORTIONS OF A CACHE WITH VALID DATA |

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| FREESCALE SEMICONDUCTOR, INC. | 5824584 | METHOD OF MAKING AND ACCESSING SPLIT GATE MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5824601 | CARBOXYLIC ACID ETCHING SOLUTI ON AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5825091 | SENSOR ASSEMBLY MOUNTED TO A L EADFRAME WITH ADHESIVE DEPOSIT S AT SEPARATE LOCATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 5825093 | ATTACHMENT SYSTEM AND METHOD T HEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5825640 | CHARGE PUMP CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5825819 | ASYMMETRICAL DIGITAL SUBSCRIBE R LINE (ADSL) LINE DRIVER CIRC UIT |
| FREESCALE SEMICONDUCTOR, INC. | 5826047 | METHOD AND APPARATUS FOR EXTER NAL VIEWING OF AN INTERNAL BUS |
| FREESCALE SEMICONDUCTOR, INC. | 5826058 | METHOD AND APPARATUS FOR PROVI DING AN EXTERNAL INDICATION OF INTERNAL CYCLES IN A DATA PROC ESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5827625 | METHODS OF DESIGNING AND FORMI NG A RETICLE AND FORMING A SEM ICONDUCTOR DEVICE THEREWITH |
| FREESCALE SEMICONDUCTOR, INC. | 5828264 | TWO-STAGE OPERATIONAL AMPLIFIE R CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5828607 | MEMORY PROGRAMMING CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5828612 | METHOD AND CIRCUIT FOR CONTROL LING A PRECHARGE CYCLE OF A ME MORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5828827 | DATA PROCESSING SYSTEM FOR PER FORMING A TEST FUNCTION AND ME THOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5829879 | TEMPERATURE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | 5831699 | DISPLAY WITH INACTIVE PORTIONS AND ACTIVE PORTIONS AND HAVIN G DRIVERS IN THE INACTIVE PORT IONS |
| FREESCALE SEMICONDUCTOR, INC. | 5831832 | MOLDED PLASTIC BALL GRID ARRAY PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 5832370 | CURRENT MODE TRANSCEIVER CIRCU IT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5838416 | DEVICE AND METHOD FOR ENHANCIN G THE VIEWING ANGLE OF A DISPL AY |
| FREESCALE SEMICONDUCTOR, INC. | 5844315 | LOW-PROFILE MICROELECTRIC PACK AGE, AND METHOD FOR FORMING SA ME |
| FREESCALE SEMICONDUCTOR, INC. | 5844319 | MICROELECTRONIC ASSEMBLY WITH COLLAR SURROUNDING INTEGRATED CIRCUIT COMPONENT ON A SUBSTRA TE |
| FREESCALE SEMICONDUCTOR, INC. | 5845098 | ADDRESS LINES LOAD REDUCTION |
| FREESCALE SEMICONDUCTOR, INC. | 5848289 | EXTENSIBLE CENTRAL PROCESSING UNIT |
| FREESCALE SEMICONDUCTOR, INC. | 5848466 | METHOD FOR FORMING A MICROELEC TRONIC ASSEMBLY AND ASSEMBLY FORMED THEREBY |
| FREESCALE SEMICONDUCTOR, INC. | 5849440 | PROCESS FOR PRODUCING AND INSP ECTING A LITHOGRAPHIC RETICLE AND FABRICATING SEMICONDUCTOR DEVICES USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5851927 | METHOD OF FORMING A SEMICONDUC TOR DEVICE BY DUV RESIST PATTE RNING |
| FREESCALE SEMICONDUCTOR, INC. | 5852316 | COMPLEMENTARY HETEROJUNCTION A MPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 5854944 | METHOD AND APPARATUS FOR DETER MINING WAIT STATES ON A PER CY CLE BASIS IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5856068 | METHOD FOR FABRICATING A PRINT ED CIRCUIT BOARD UNDER SUPERAT MOSPHERIC PRESSURE |
| FREESCALE SEMICONDUCTOR, INC. | 5856684 | HIGH POWER HFET WITH IMPROVED CHANNEL INTERFACES |
| FREESCALE SEMICONDUCTOR, INC. | 5859541 | DATA PROCESSOR HAVING AN OUTPU T TERMINAL WITH SELECTABLE OUT PUT IMPEDANCES |
| FREESCALE SEMICONDUCTOR, INC. | 5861347 | METHOD FOR FORMING A HIGH VOLT AGE GATE DIELECTRIC FOR USE IN INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 5863838 | SLURRY FOR CHEMICALLY-MECHANIC ALLY POLISHING A LAYER AND MET |

HOD OF USE

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 5867032 | PROCESS FOR TESTING A SEMICOND UCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5870670 | INTEGRATED IMAGE REJECT MIXER |
| FREESCALE SEMICONDUCTOR, INC. | 5872374 | VERTICAL SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5872385 | CONDUCTIVE INTERCONNECT STRUCT URE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 5872458 | METHOD FOR ELECTRICALLY CONTAC TING SEMICONDUCTOR DEVICES IN TRAYS AND TEST CONTACTOR USEFU L THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5875143 | DYNAMIC MEMORY DEVICE WITH REF RESH CIRCUIT AND REFRESH METHO D |
| FREESCALE SEMICONDUCTOR, INC. | 5875482 | METHOD AND APPARATUS FOR PROGR AMMABLE CHIP SELECT NEGATION I N A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5875897 | PACKAGING APPARATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5877047 | LATERAL GATE, VERTICAL DRIFT R EGION TRANSLATION |
| FREESCALE SEMICONDUCTOR, INC. | 5877654 | CLASS A AMPLIFIER WITH A DIGIT ALLY PROGRAMMABLE MILLER COMPENSATION NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 5879630 | SEMICONDUCTOR CHEMICAL SENSOR DEVICE AND ETHOD OF FORMING A THERMOCOUPLE FOR A SEMICONDUCT OR CHEMICAL SENSOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5880018 | A METHOD FOR MANUFACTURING A L OW DIELECTRIC CONSTANT INTERLE VEL INTEGRATED CIRCUIT STRUCTU RE |
| FREESCALE SEMICONDUCTOR, INC. | 5880687 | CASCADED INTEGRATOR-COMB INTER POLATION FILTER |
| FREESCALE SEMICONDUCTOR, INC. | 5882034 | AUTOMOBILE AIRBAG SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5883012 | METHOD OF ETCHING A TRENCH INT O A SEMICONDUCTOR SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 5883305 | TIRE PRESSURE MONITORING SYSTE M |
| FREESCALE SEMICONDUCTOR, INC. | 5883404 | COMPLEMENTARY HETEROJUNCTION S EMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5885856 | INTEGRATED CIRCUIT HAVING A DU MMY STRUCTURE AND METHOD OF MA KING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5885860 | SILICON CARBIDE TRANSISTOR AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5885870 | METHOD FOR FORMING A SEMICONDU CTOR DEVICE HAVING A NITRIDED OXIDE DIELECTRIC LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 5886396 | LEADFRAME ASSEMBLY FOR CONDUCT ING THERMAL ENERGY FROM A SEMI CONDCUTOR DIE DISPOSED IN A PA CKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 5886556 | LOW POWER SCHMITT TRIGGER |
| FREESCALE SEMICONDUCTOR, INC. | 5886562 | METHOD AND APPARATUS FOR SYNCH RONIZING A PLURALITY OF OUTPUT CLOCK SIGNALS GENERATED FROM A CLOCK INPUT SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 5886928 | NON-VOLATILE MEMORY CELL AND M ETHOD OF PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | 5888412 | METHOD FOR MAKING A SCULPTURED DIAPHRAHM |
| FREESCALE SEMICONDUCTOR, INC. | 5889211 | MEDIA COMPATIBLE MICROSENSOR S TRUCTURE AND METHODS OF MANUFA CTURING AND USING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5889788 | WRAPPER CELL ARCHITECTURE FOR PATH DELAY TESTING OF EMBEDDED CORE MICROPROCESSORS AND METH OD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 5889973 | METHOD AND APPPARATUS FOR SELE CTIVELY CONTROLLING INTERRUPT LATENCY IN A DATA PROCESSING S YSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5890191 | METHOD AND APPARATUS FOR PROVI DING ERASING AND PROGRAMMING P ROTECTION FOR ELECTRICALLY ERA SABLE PROGRAMMABLE READ ONLY M EMORY |

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| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 5890799 | METHOD FOR REDUCING POWER CONS UMPTION IN A PORTABLE ELECTRON IC DEVICE WITH A LIQUID CRYSTA L DISPLAY SCREEN |
| FREESCALE SEMICONDUCTOR, INC. | 5891606 | HIGH-DENSITY CIRCUIT STRUCTURE WITH INTERLAYER ELECTRICAL CO NNECTIONS AND PROCESS THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5892252 | CHEMICAL SENSING TRENCH FIELD EFFECT TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 5892379 | TRANSISTOR PROTECTION CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5892661 | SMARTCARD AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 5892682 | METHOD AND APPARATUS FOR GENER ATING A HIERARCHICAL INTERCONN ECTION DESCRIPTION OF AN INTEG RATED CIRCUIT DESIGN AND USING THE DESCRIPTION TO EDIT THE IN TEGRATED CIRCUIT DESIGN |
| FREESCALE SEMICONDUCTOR, INC. | 5892777 | APPARATUS AND METHOD FOR OBSER VING THE MODE OF A MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5893137 | APPARATUS AND METHOD FOR IMPLE MENTING A CONTENT ADDRESSABLE MEMORY CIRCUIT WITH TWO STAGE MATCHING |
| FREESCALE SEMICONDUCTOR, INC. | 5893752 | SEMICONDUCTOR DEVICE AND A PRO CESS FOR FORMING THE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5895229 | MICROELECTRONIC PACKAGE INCLUD ING A POLYMER ENCAPSULATED DIE , AND METHOD FOR FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5895247 | METHOD OF FORMING A HIGH PERFO RMANCE, HIGH VOLTAGE NON-EPI B IPOLAR TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 5895260 | METHOD OF FABRICATING SEMICOND UCTOR DEVICES AND THE DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 5895929 | LOW SUBTHRESHOLD LEAKAGE CURRE NT HFET |
| FREESCALE SEMICONDUCTOR, INC. | 5895976 | MICROELECTRONIC ASSEMBLLY INCL UDING POLYMERIC REMINFORCEMENE T DIE AND METHOD FOR FORMING S AME |
| FREESCALE SEMICONDUCTOR, INC. | 5896045 | A STATIC PULSED CROSS-COUPLED LEVEL SHIFTER AND METHOD THERE FOR |
| FREESCALE SEMICONDUCTOR, INC. | 5896335 | METHOD AND APPARATUS FOR REDUC ING POWER DISSIPATION IN A PRE CHARGE/DISCHARGE MEMORY SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5897375 | CHEMICAL MECHANICAL POLISHING (CMP) SLURRY FOR COPPER AND METHOD OF USE IN INTEGRATED CIRCUIT MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 5898213 | SEMICONDUCTOR PACKAGE BOND POS T CONFIGURATION |
| FREESCALE SEMICONDUCTOR, INC. | 5898217 | SEMICONDUCTOR DEVICE INCLUDING A SUBSTRATE HAVING CLUSTERED INTERCONNECTS |
| FREESCALE SEMICONDUCTOR, INC. | 5898617 | SENSING CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5898619 | MEMORY CELL HAVING A PLURAL TR ANSISTOR TRANSMISSION GATE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 5898633 | CIRCUIT AND METHOD OF LIMITING LEAKAGE CURRENT IN A MEMORY C IRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5900340 | ONE-DIMENSIONAL LITHOGRAPHIC P ROXIMITY CORRECTION USING DRC SHAPE FUNCTIONS |
| FREESCALE SEMICONDUCTOR, INC. | 5900530 | METHOD FOR TESTING PRESSURE SE NSORS |
| FREESCALE SEMICONDUCTOR, INC. | 5900776 | CURRENT SENSE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5901103 | INTEGRATED CIRCUIT HAVING STAN DBY CONTROL FOR MEMORY AND MET HOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 5902130 | THERMAL PROCESSING OF OXIDE CO MPOUND SEMICONDUCTOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 5903038 | SEMICONDUCTOR SENSING DEVICE A ND METHOD FOR FABRICATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5903419 | CIRCUIT FOR ELECTROSTATIC DISC HARGE (ESD) PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 5903748 | METHOD AND APPARATUR FOR MANAG ING FAILURE OF A SYSTEM CLOCK IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5903919 | METHOD AND APPARATUS FOR SELEC TING A REGISTER BANK |
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| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 5904547 | APPARATUS FOR DICING A SEMICON DUCTOR DEVICE SUBSTRATE AND A PROCESSOR THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5904553 | FABRICATION METHOD FOR A GATE QUALITY OXIDE-COMPOUND SEMICON DUCTOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 5905393 | UNBUFFERED LATCH RESISTANT TO BACKWRITING AND METHOD OF OPER ATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5905397 | A MOS SWITCHING CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5907765 | SEMICONDUCTOR SENSOR DEVICE AN D METHOD FOR FORMING A SEMICON DUCTOR SENSOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5907792 | METHOD OF FORMING A SILICON NI TRIDE LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 5910994 | METHOD AND APPARATUS FOR SUPPR ESSING ACOUSTIC FEEDBACK IN AN AUDIO SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5911151 | OPTIMIZING BLOCK-SIZED OPERAND MOVEMENT UTILIZING STANDARD I NSTRUCTIONS |
| FREESCALE SEMICONDUCTOR, INC. | 5912510 | BONDING STRUCTURE FOR AN ELECT RONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5912562 | QUIESCENT CURRENT MONITOR CIRC UIT FOR WAFER LEVEL INTEGRATED CIRCUIT TESTING |
| FREESCALE SEMICONDUCTOR, INC. | 5912819 | METHOD FOR DESIGNING AN ARCHIT ECTURAL SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5914521 | SEMICONDUCTOR DEVICE AND METHO D FOR MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5915463 | HEAT DISSIPATION APPARATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5916011 | PROCESS FOR POLISHING A SEMICO NDUCTOR DEVICE SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 5917336 | CIRCUIT FOR ELECTROSTATIC DISC HARGE (ESD) PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 5917358 | METHOD AND OUTPUT BUFFER WITH PROGRAMMABLE BIAS TO ACCOMODAT E MULTIPLE SUPPLY VOLTAGES |
| FREESCALE SEMICONDUCTOR, INC. | 5917363 | MULTIPLEXED DRIVER SYSTEM REQU IRING A REDUCED NUMBER OF AMPL IFIER CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 5918112 | SEMICONDUCTOR COMPONENT AND ME THOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 5918247 | METHOD FOR CANCELING PARTIAL L INE FETCH FOR CACHE WHEN NEW D ATA IS REQUESTED DURING CURREN T FETCH AND INVALIDATING PORTI ON OF PREVIOUSLY FETCHED DATA |
| FREESCALE SEMICONDUCTOR, INC. | 5920093 | SOI FET HAVING GATE SUB-REGION S CONFORMING TO T-SHAPE |
| FREESCALE SEMICONDUCTOR, INC. | 5920113 | LEADFRAME STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 5920487 | TWO DIMENSIONAL LITHOGRAPHIC PROXIMITY CORRECTION USING DRC SHAPE FUNCTIONS |
| FREESCALE SEMICONDUCTOR, INC. | 5920690 | METHOD AND APPARATUS FOR PROVI DING ACCESS PROTECTION IN AN I NTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5920810 | MULTIPLIER AND METHOD FOR MIXI NG SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 5923217 | AMPLIFIER CIRCUIT AND METHOD F OR GENERATING A BIAS VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | 5923222 | LOW POWER AMPLIFIER AND AN OSC ILLATING CIRCUIT INCORPORATING THE AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 5923615 | SYNCHRONOUS PIPELINED BURST ME MORY AND METHOD FOR OPERATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5924005 | PROCESS FOR FORMING A SEMICOND UCTOR DEVICE WITH A LOW K DIEL ECTRIC LAYER AND DEVICE MADE T HEREBY |
| FREESCALE SEMICONDUCTOR, INC. | 5925908 | SEMICONDUCTOR DEVICE AND METHO D OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 5928001 | SURFACE MOUNTABLE FLEXIBLE INTERCONNECT |
| FREESCALE SEMICONDUCTOR, INC. | 5929478 | SINGLE LEVEL GATE NONVOLATILE MEMORY DEVICE AND METHOD FOR A CCESSING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5929494 | A READ ONLY MEMORY ARRAY AND A METHOD OF MANUFACTURING THE A |

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| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 5929659 | CIRCUIT AND PROCESS FOR SENSIN G DATA |
| FREESCALE SEMICONDUCTOR, INC. | 5929662 | ANALOG COMPARATOR AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5932924 | LEADFRAME HAVING CONTINUOUSLY REDUCING WIDTH AND SEMICONDUCT OR DEVICE INCLUDING SUCH A LEA D FRAME |
| FREESCALE SEMICONDUCTOR, INC. | 5933750 | METHOD OF FABRICATING A SEMICO NDUCTOR DEVICE WITH A THINNED SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 5935871 | PROCESS FOR FORMING A SEMICOND UCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5936454 | LATERAL BIPOLAR TRANSISTOR OPE RATING WITH INDEPENDENT BASE A ND GATE BIASING |
| FREESCALE SEMICONDUCTOR, INC. | 5936469 | AMPLIFIER WITH INPUT REFERRED COMMON-MODE ADJUSTMENT |
| FREESCALE SEMICONDUCTOR, INC. | 5936837 | SEMICONDUCTOR COMPONENT HAVING LEADFRAME WITH OFFSET GROUND PLANE |
| FREESCALE SEMICONDUCTOR, INC. | 5937285 | METHOD OF FABRICATING SUBMICRO N FETS AND DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5939753 | MONOLITHIC INTEGRATED CIRCUIT AND PROCESS FOR FABRICATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5939906 | CIRCUIT COMPENSATING NONLINEARITIES |
| FREESCALE SEMICONDUCTOR, INC. | 5940683 | LED DISPLAY PACKAGING WITH SUB STRATE REMOVAL AND METHOD OF F ABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 5941974 | SERIAL INTERFACE WITH REGISTER SELECTION WHICH USES CLOCK COUNTING, CHIP SELECT PULSING, AND NO ADDRESS BITS |
| FREESCALE SEMICONDUCTOR, INC. | 5943274 | METHOD AND APPARATUS FOR AMPLI FYING A SIGNAL TO PRODUCE A LA TCHED DIGITAL SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 5945346 | CHEMICAL MECHANICAL PLANARIZAT ION SYSTEM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5945694 | METHOD OF FORMING A COMPOUND S EMICONDUCTOR DEVICE HAVING RED UCED TERMPERATURE VIABILITY |
| FREESCALE SEMICONDUCTOR, INC. | 5945718 | SELF-ALIGNED METAL-OXIDE-COMPO UND SEMICONDUCTOR DEVICE AND M ETHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 5946177 | CIRCUIT FOR ELECTROSTATIC DISC HARGE PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 5949125 | SEMICONDUCTOR DEVICE HAVING FI ELD ISOLATION WITH A MESA |
| FREESCALE SEMICONDUCTOR, INC. | 5952870 | CIRCUIT WITH HYSTERESIS AND ME THOD USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5953251 | PROGRAMMING METHOD FOR NONVOLA TILE MEMORIES |
| FREESCALE SEMICONDUCTOR, INC. | 5954813 | DATA PROCESSOR WITH TRANSPARENT OPERATION DURING A BACKGROUND MODE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 5955980 | CIRCUIT AND METHOD FOR CALIBRA TING A DIGITAL TO ANALOG CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 5956336 | APPARATUS AND METHOD FOR CONCURRENT SEARCH CONTENT ADDRESSABLE MEMORY CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5958029 | METHOD AND SYSTEM FOR EFFICIENT MESSAGE VALIDATION |
| FREESCALE SEMICONDUCTOR, INC. | 5958508 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5958635 | LITHOGRAPHIC PROXIMITY CORRECTION THROUGH SUBSET FEATURE MODIFICATION |
| FREESCALE SEMICONDUCTOR, INC. | 5959462 | A TEST STRUCTURE FOR ENABLING BURN-IN TESTING ON AN ENTIRE SEMICONDUCTOR WAFER |
| FREESCALE SEMICONDUCTOR, INC. | 5959522 | INTEGRATED ELECTROMAGNETIC DEV ICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5960270 | METHOD OF FORMING AN MOS TRANSISTOR HAVING A METALLIC GATE ELECTRODE THAT IS FORMED AFTER THE FORMATION OF SELF-ALIGNED SOURCE AND DRAIN REGIONS |
| FREESCALE SEMICONDUCTOR, INC. | 5960289 | A METHOD FOR MAKING A DUAL-THICKNESS GATE OXIDE LAYER USING A NITRIDE/OXIDE COMPOSITE REGION |
| FREESCALE SEMICONDUCTOR, INC. | 5960306 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 5961373 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5961622 | SYSTEM AND METHOD FOR RECOVERING A MICROPROCESSOR FROM A LOCKED BUS STATE |
| FREESCALE SEMICONDUCTOR, INC. | 5961791 | PROCESS FOR FABRICATING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5962926 | SEMICONDUCTOR DEVICE HAVING MULTIPLE OVERLAPPING ROWS OF BOND PADS WITH CONDUCTIVE INTERCONNECTS AND METHOD OF PAD PLACE |
| FREESCALE SEMICONDUCTOR, INC. | 5963068 | FAST START-UP PROCESSOR CLOCK GENERATION METHOD AND SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 5963315 | METHOD AND APPARATUS FOR PROCESSING A SEMICONDUCTOR WAFER ON A ROBOTIC TRACK HAVING ACCESS TO IN SITU WAFER BACKSIDE PARTICLE DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | 5963782 | SEMICONDUCTOR COMPONENT AND ME THOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 5965912 | VARIABLE CAPACITOR AND METHOD FOR FABRICATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5966029 | MULTI-BIT EXCLUSIVE OR |
| FREESCALE SEMICONDUCTOR, INC. | 5966038 | CIRCUIT WITH OVERVOLTAGE PROTE CTION AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5966047 | PROGRAMMABLE ANALOG ARRAY AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5966054 | METHOD AND APPARATUS FOR PROVIDING A CLOCKING SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 5966635 | METHOD FOR REDUCING PARTICLES ON A SUBSTRATE USING CHUCK CLE ANING |
| FREESCALE SEMICONDUCTOR, INC. | 5969383 | SPLIT GATE MEMORY DEVICE AND METHOD FOR ACCESSING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 5972804 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 5973379 | FERROELECTRIC SEMICONDUCTOR DE VICE |
| FREESCALE SEMICONDUCTOR, INC. | 5973388 | LEADFRAME, METHOD OF MANUFACTU RING A LEADFRAME AND METHOD OF PACKAGING AN ELECTRONIC COMPO NENT UTILIZING THE LEADFRAME |
| FREESCALE SEMICONDUCTOR, INC. | 5973568 | POWER AMPLIFIER OUTPUT MODULE FOR DUAL-MODE DIGITAL SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 5973955 | COMPARISON CIRCUIT UTILIZING A DIFFERENTIAL AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 5975757 | PROVE FOR PROVIDING SURFACE IM AGES AND METHOD FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 5977632 | FLIP CHIP BUMP STRUCTURE AND M ETHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 5977892 | OFFSET CANCELLATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5978249 | HIGH IMPEDANCE SIGNAL CONVERSI ON CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 5978286 | TIMING CONTROL OF AMPLIFIERS I N A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 5980106 | TEMPERATURE DETECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 5981340 | METHOD OF BUILDING AN EPROM CELL WITHOUT DRAIN DISTURB AND REDUCED SELECT GATE RESISTANCE |
| FREESCALE SEMICONDUCTOR, INC. | 5982166 | METHOD FOR MEASURING A CHARACT ERISTIC OF A SEMICONDUCTOR WAF ER USING CYLINDRICAL CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 5985045 | PROCESS FOR POLISHING A SEMICONDUCTOR SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 5985731 | METHOD FOR FORMING A SEMICONDU CTOR DEVICE HAVING A CAPACITOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 5986598 | SIGMA DELTA DATA CONVERTER WIT H FEED-FORWARD PATH TO STABILI ZE INTEGRATOR SIGNAL SWING |
| FREESCALE SEMICONDUCTOR, INC. | 5990547 | SEMICONDUCTOR DEVICE HAVING PLATED CONTACTS AND METHOD |

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| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 5995731 | MULTIPLE BIST CONTROLLERS FOR TESTING MULTIPLE EMBEDDED MEMO RY ARRAYS |
| FREESCALE SEMICONDUCTOR, INC. | 5998258 | METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING A STACKED CAPACITOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6000029 | METHOD AND APPARATUS FOR AFFECTING SUBSEQUENT INSTRUCTION PROCESSING IN A DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 6001730 | A CHEMICAL MECHANICAL POLISHING (CMP) SLURRY FOR POLISHING COPPER INTERCONNECTS WHICH USE TANTALUM-BASED BARRIER LAYERS |
| FREESCALE SEMICONDUCTOR, INC. | 6002273 | LINEAR LOW NOISE PHASE-FREQUEN CY DETECTOR |
| FREESCALE SEMICONDUCTOR, INC. | 6003133 | DATA PROCESSOR WITH A PRIVILEGED STATE FIREWALL AND METHOD THEREFORE |
| FREESCALE SEMICONDUCTOR, INC. | 6004850 | A TANTALUM OXIDE ANTI-REFLECTI VE COATING (ARC) INTEGRATED WITH A METALLIC TRANSISTOR GATE ELECTRODE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 6005634 | METHOD AND APPARATUS FOR CONTR OLLING THE DISPLAY OF A VIDEO IMAGE |
| FREESCALE SEMICONDUCTOR, INC. | 6008677 | VOLTAGE RECOVERY CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6009012 | MICROCONTROLLER HAVING A NON-VOLATILE MEMORY AND A METHOD FOR SELECTING AN OPERATIONAL MODE |
| FREESCALE SEMICONDUCTOR, INC. | 6010927 | A METHOD FOR MAKING A FERROELECTRIC DEVICE HAVING A TANTALUM NITRIDE BARRIER LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 6011734 | A FUSELESS MEMORY REPAIR SYSTEM AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 6011749 | INTEGRATED CIRCUIT HAVING OUTPUT TIMING CONTROL CIRCUIT AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6012076 | ARITHMETIC LOGIC UNIT HAVING P RESHIFT AND PREROUND CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 6013571 | MICROELECTRONIC ASSEMBLLY INCL UDING COLUMNAR INTERCONNECTION S AND METHOD FOR FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6013933 | SEMICONDUCTOR STRUCTURE HAVING A MONOCRYSTALLINE MEMBER OVER LYING A CAVITY IN A SEMICONDUC TOR SUBSTRATE AND PROCESS THER EFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6014722 | DATA COMMUNICATION SYSTEM FOR CONTROLLING PRIORITIZATION AND TRANSFER OF DATA AND METHOD TH EREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6016269 | QUANTUM RANDOM ADDRESS MEMORY WITH MAGNETIC READOUT AND/OR N ANO-MEMORY ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | 6017798 | FET WITH STABLE THRESHOLD VOLT AGE AND METHOD OF MANUFACTURIN G THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6018998 | ACCELERATION SENSING DEVICE AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 6019508 | INTEGRATED TEMPERATURE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | 6020024 | METHOD FOR FORMING HIGH DIELECTRIC CONSTANT METAL OXIDES |
| FREESCALE SEMICONDUCTOR, INC. | 6020611 | SEMICONDUCTOR COMPONENT AND ME THOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6020787 | METHOD AND APPARATUS FOR AMPLIFYING A SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 6021072 | METHOD AND APPARATUS FOR PRECHARGING BITLINES IN A NONVOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 6022754 | ELECTRONIC DEVICE AND METHOD F OR FORMING A MEMBRANE FOR AN ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6022761 | METHOD FOR COUPLING SUBSTRATES AND STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6023091 | SEMICONDUCTOR HEATER AND METHO D FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 6023133 | PARABOLIC SIGNAL GENERATOR |
| FREESCALE SEMICONDUCTOR, INC. | 6023136 | ADAPTIVE MOTOR CONTROL CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6023141 | METHOD AND APPARATUS FOR ELECT RONICALLY COMMUTATING AN ELECT |

RIC MOTOR

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6026003 | CHARGE PUMP CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6026013 | QUANTUM RANDOM ADDRESS MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 6026501 | DATA PROCESSING SYSTEM FOR CON TROLLING EXECUTION OF A DEBUG FUNCTION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6027961 | CMOS SEMICONDUCTOR DEVICES AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 6027997 | METHOD FOR CHEMICAL MECHANICAL POLISHING A SEMICONDUCTOR DEVICE USING SLURRY |
| FREESCALE SEMICONDUCTOR, INC. | 6031775 | DYNAMIC SENSE AMPLIFIER IN A MEMORY CAPABLE OF LIMITING THE VOLTAGE SWING ON HIGH-CAPACITANCE GLOBAL DATA LINES |
| FREESCALE SEMICONDUCTOR, INC. | 6034333 | ASSEMBLY HAVING A FRAME EMBEDD ED IN A POLYMERIC ENCAPSULANT AND METHOD FOR FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6034562 | MIXED SIGNAL PROCESSING SYSTEM AND METHOD FOR POWERING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6034735 | CLOCK GENERATOR FOR DIGITAL VI DEO SIGNAL PROCESSING APPARATU S |
| FREESCALE SEMICONDUCTOR, INC. | 6034736 | DIGITAL HORIZONTAL FLYBACK CON TROL CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6035372 | MICROPROCESSOR AND SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6035422 | DATA PROCESSING SYSTEM FOR CON TROLLING EXECUTION OF A DEBUG FUNCTION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6037668 | INTEGRATED CIRCUIT HAVING A SUPPORT STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6039765 | COMPUTER INSTRUCTION WHICH GENERATES MULTIPLE RESULTS OF DIFFERENT DATA TYPES TO IMPROVE SOFTWARE EMULATION |
| FREESCALE SEMICONDUCTOR, INC. | 6040604 | SEMICONDUCTOR COMPONENT COMPRISING AN ELECTROSTATIC-DISCHARGE PROTECTION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6040624 | SEMICONDUCTOR DEVICE PACKAGE A ND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6040729 | DIGITAL OUTPUT BUFFER FOR MULTIPLE VOLTAGE SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6043146 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6043524 | TRANSDUCER AND INTERFACE CIRCU IT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6044036 | BUFFER CIRCUIT MEMORY DEVICE, AND INTEGRATED CIRCUIT FOR RECEIVING DIGITAL SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 6044392 | METHOD AND APPARATUS FOR PERFO RMING ROUNDING IN A DATA PROCE SSOR |
| FREESCALE SEMICONDUCTOR, INC. | 6045435 | LOW SELECTIVITY CHEMICAL MECHA NICAL POLISHING (CMP) PROCESS FOR USE ON INTEGRATED CIRCUIT METAL INTERCONNECTS |
| FREESCALE SEMICONDUCTOR, INC. | 6046642 | AMPLIFIER WITH ACTIVE BIAS COM PENSATION AND METHOD FOR ADJUS TING QUIESCENT CURRENT |
| FREESCALE SEMICONDUCTOR, INC. | 6046897 | SEGMENTED BUS ARCHITECTURE (SB A) FOR ELECTROSTATIC DISCHARGE (ESD) PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 6046901 | SUPPORT STRUCTURE ELECTRONIC A SSEMBLY AND METHOD OF MANUFACT URE |
| FREESCALE SEMICONDUCTOR, INC. | 6046910 | MICROELECTRONIC ASSEMBLY HAVIN G SLIDABLE |
| FREESCALE SEMICONDUCTOR, INC. | 6047025 | METHOD AND APPARATUS FOR EQUAL IZATION IN AN ASYMMETRIC DIGIT AL SUBSCRIBER LINE (ADSL) |
| FREESCALE SEMICONDUCTOR, INC. | 6047390 | MULTIPLE CONTEXT SOFTWARE ANAL YSIS |
| FREESCALE SEMICONDUCTOR, INC. | 6049114 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE AND A SEMICONDUCTOR DEVICE FORMED THEREBY |
| FREESCALE SEMICONDUCTOR, INC. | 6049119 | PROTECTION CIRCUIT FOR A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6049501 | MEMORY DATA BUS ARCHITECTURE AND METHOD OF CONFIGURING MULTIWIDE WORD MEMORIES |
| FREESCALE SEMICONDUCTOR, INC. | 6049865 | METHOD AND APPARATUS FOR IMPLEMENTING FLOATING POINT PROJECTION INSTRUCTIONS |

INSTRUCTIONS

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6049876 | DATA PROCESSING SYSTEM AND METHOD WHICH DETECT UNAUTHORIZED MEMORY ACCESSES |
| FREESCALE SEMICONDUCTOR, INC. | 6051997 | CIRCUIT FOR TRACKING RAPID CHA NGES IN MID-POINT VOLTAGE OF A DATA SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 6052302 | BIT-WISE CONDITIONAL WRITE METHOD AND SYSTEM FOR AN MRAM |
| FREESCALE SEMICONDUCTOR, INC. | 6052746 | INTEGRATED CIRCUIT HAVING SINGLE PROGRAMMABLE PULL DEVICE CONFIGURED TO ENABLE/DISABLE FIRST FUNCTION IN FAVOR OF SECOND FUNCTION ACCORDING TO PREDETERMINED SCHEME BEFORE/AFTER RESET |
| FREESCALE SEMICONDUCTOR, INC. | 6053049 | ELECTRICAL DEVICE HAVING ATMOS PHERIC ISOLATION |
| FREESCALE SEMICONDUCTOR, INC. | 6054825 | METHOD AND APPARATUS FOR HIGH VOLTAGE GENERATION |
| FREESCALE SEMICONDUCTOR, INC. | 6054901 | LOW-NOISE PREAMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 6056888 | ELECTRONIC COMPONENT AND METHO D OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6057219 | METHD OF FORMING AN OHMIC CONT ACT TO A III-A SEMICONDUCTOR M ATERIAL |
| FREESCALE SEMICONDUCTOR, INC. | 6057566 | SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6057713 | METHOD AND APPARATUS FOR PERFORMING VOLTAGE SAMPLING |
| FREESCALE SEMICONDUCTOR, INC. | 6058405 | SIMD COMPUTATION OF RANK BASED FILTERS FOR M X N GRIDS |
| FREESCALE SEMICONDUCTOR, INC. | 6058449 | FAULT TOLERANT SERIAL ARBITRATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6061218 | OVERVOLTAGE PROTECTION DEVICE AND METHOD FOR INCREASING SHUN T CURRENT |
| FREESCALE SEMICONDUCTOR, INC. | 6063698 | A METHOD FOR MANUFACTURING A HIGH DIELECTRIC CONSTANT GATE OXIDE FOR USE IN SEMICONDUCTOR INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 6064114 | SEMICONDUCTOR DEVICE HAVING A SUB-CHIP-SCALE PACKAGE STRUCTURE AND METHOD FOR FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6066971 | INTEGRATED CIRCUIT HAVING BUFFERING CIRCUITRY WITH SLEW RATE CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 6068668 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6069493 | INPUT CIRCUIT AND METHOD FOR P ROTECTING THE INPUT CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6069593 | DISPLAY CARRIER AND ELECTRONIC DISPLAY CONTROL FOR MULTIPLE DISPLAYS IN A PORTABLE ELECTRO NIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6070263 | CIRCUIT FOR USE IN A VITERBI D ECODER |
| FREESCALE SEMICONDUCTOR, INC. | 6070464 | SENSING STRUCTURE COMPRISING A MOVABLE MASS AND A SELF-TEST STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6071816 | METHOD OF CHEMICAL MECHANICAL PLANARIZATION USING A WATER RINSE TO PREVENT PARTICLE CONTAMINATION |
| FREESCALE SEMICONDUCTOR, INC. | 6072211 | SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 6072238 | SEMICONDUCTOR COMPONENT |
| FREESCALE SEMICONDUCTOR, INC. | 6073252 | DATA PROCESSING SYSTEM WITH MEMORY PATCHING AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6075271 | SEMICONDUCTOR DEVICE INHIBITING PARASITIC EFFECTS DURING ELECTROSTATIC DISCHARGE |
| FREESCALE SEMICONDUCTOR, INC. | 6075409 | DEMODULATION METHOD AND ARRANG MENT |
| FREESCALE SEMICONDUCTOR, INC. | 6075727 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6076096 | BINARY RATE MULTIPLIER |
| FREESCALE SEMICONDUCTOR, INC. | 6076149 | DATA PROCESSING CIRCUIT |
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| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6076177 | METHOD AND APPARATUS FOR TESTING A CIRCUIT MODULE CONCURRENTLY WITH A NON-VOLATILE MEMORY OPERATION IN A MULT-MODULE DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6077726 | METHOD AND APPARATUS FOR STRESS RELIEF IN SOLDER BUMP FORMATION ON A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6078277 | ARRANGEMENT AND METHOD FOR PRO DUCING A PLURALITY OF PULSE WI DTH MODULATED SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 6078527 | PIPELINED DUAL PORT INTEGRATED CIRCUIT MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 6079015 | DATA PROCESSING SYSTEM HAVING SELECTABLE EXCEPTIONAL TABLE RELOCATION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6081037 | SEMICONDUCTOR DEVICE AND METHO D FOR PACKAGING A SEMICONDUCTO R CHIP |
| FREESCALE SEMICONDUCTOR, INC. | 6081091 | MOTOR CONTROLLER, INTEGRATED CIRCUIT, AND METHOD OF CONTROLLING A MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | 6081216 | LOW-POWER DECIMATOR FOR AN OVERSAMPLED ANALOG-TO-DIGITAL CONVERTER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6083806 | METHOD OF FORMING AN ALIGNMENT MARK |
| FREESCALE SEMICONDUCTOR, INC. | 6083819 | METHOD AND ASSEMBLY FOR PROVID ING INPROVED UNDERCHIP ENCAPSU LATION |
| FREESCALE SEMICONDUCTOR, INC. | 6084241 | METHOD OF MANUFACTURING SEMICO NDUCTOR DEVICES AND APPARATUS THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6084279 | SEMICONDUCTOR DEVICE AND A PROCESS FOR FORMING THE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6087701 | SEMICONDUCTOR DEVICE HAVING A CAVITY AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 6087873 | PRECISION HYSTERESIS CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6088215 | CAPACITOR AND METHOD OF MANUFA CTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6088782 | METHOD AND APPARATUS FOR MOVING DATA IN A PARALLEL PROCESSOR USING SOURCE AND DESTINATION VECTOR REGISTERS |
| FREESCALE SEMICONDUCTOR, INC. | 6091287 | VOLTAGE REGULATOR WITH AUTOMATIC ACCELERATED AGING CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6093966 | A SEMICONDUCTOR DEVICE WITH A COPPER BARRIER LAYER AND FORMATION THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6093972 | MICROELECTRONIC PACKAGE INCLUD ING A POLYMER ENCAPSULATED DIE , AND METHOD FOR FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6094295 | ULTRAVIOLET TRANSMITTING OXIDE WITH METALLIC OXIDE PHASE AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 6096575 | OPTIMUM CONDITION DETECTING METHOD FOR FLIP-CHIP |
| FREESCALE SEMICONDUCTOR, INC. | 6096606 | SEMICONDUCTOR DEVICE AND METHO D OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 6096652 | METHOD OF CHEMICAL MECHANICAL PLANARIZATION USING COPPER COORDINATING LIGANDS |
| FREESCALE SEMICONDUCTOR, INC. | 6097075 | SEMICONDUCTOR STRUCTURE FOR DRIVER CIRCUITS WITH LEVEL SHIFTING |
| FREESCALE SEMICONDUCTOR, INC. | 6097627 | QUANTUM RANDOM ADDRESS MEMORY WITH NANO-DIODE MIXER |
| FREESCALE SEMICONDUCTOR, INC. | 6100549 | HIGH BREAKDOWN VOLTAGE RESURF HFET |
| FREESCALE SEMICONDUCTOR, INC. | 6100763 | CIRCUIT FOR RF BUFFER AND METH OD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 6100787 | MULTILAYER CERAMIC PACKAGE WIT H LOW-VARIANCE EMBEDDED RESIST ORS AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6101125 | ELECTRICALLY PROGRAMMABLE MEMO RY AND METHOD OF PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | 6101145 | SENSING CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6103548 | SEMICONDUCTOR DEVICE AND METHO D OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6104227 | RF MIXER CIRCUIT AND METHOD OF OPERATION |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6107136 | METHOD FOR FORMING A CAPACITOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6107180 | METHOD FOR FORMING INTERCONNEC T BUMPS ON A SEMICONDUCTOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | 6107203 | A CHEMICAL MECHANICAL POLISHIN G SYSTEM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6108181 | ELECTROSTATIC DISCHARGE (ESD) CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6108263 | MEMORY SYSTEM, METHOD FOR VERIFYING DATA STORED IN A MEMORY SYSTEM AFTER A WRITE CYCLE AND METHOD FOR WRITING TO A MEMORY SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6108266 | MEMORY UTILIZING A PROGRAMMABLE DELAY TO CONTROL ADDRESS BUFFERS |
| FREESCALE SEMICONDUCTOR, INC. | 6110840 | METHOD OF PASSIVATING THE SURF ACE OF A SI SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 6111316 | ELECTRONIC COMPONENT AND METHO D FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 6111761 | AN ELECTRONIC ASSEMBLY |
| FREESCALE SEMICONDUCTOR, INC. | 6111796 | PROGRAMMABLE DELAY CONTROL IN A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 6113721 | METHOD OF BONDING A SEMICONDUCTOR WAFER |
| FREESCALE SEMICONDUCTOR, INC. | 6121784 | PROBE TIP, A PROBE CARD, AND A PROCESS FOR TESTING A SEMICON DUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6121845 | PHASED-LOCKED LOOP SYSTEM AND METHOD FOR MODIFYING AN OUTPUT TRANSITION TIME |
| FREESCALE SEMICONDUCTOR, INC. | 6121849 | OSCILLATOR AMPLIFIER WITH FREQUENCY BASED DIGITAL MULTI-DISCRETE-LEVEL GAIN CONTROL AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 6122963 | ELECTRONIC COMPONENT |
| FREESCALE SEMICONDUCTOR, INC. | 6125404 | COMMUNICATIONS SYSTEM HAVING A PROTOCOL TIMER |
| FREESCALE SEMICONDUCTOR, INC. | 6125413 | COMPUTER SYSTEM WITH TRIGGER CONTROLLED INTERFACE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6127230 | VERTICAL SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6127258 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6127831 | METHOD OF TESTING A SEMICONDUCTOR DEVICE BY AUTOMATICALLY MEASURING PROBE TIP PARAMETERS |
| FREESCALE SEMICONDUCTOR, INC. | 6127875 | COMPLIMENTARY DOUBLE PUMPING V OLTAGE BOOST CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 6128224 | METHOD AND APPARATUS FOR WRITING AN ERASABLE NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 6128672 | DATA TRANSFER USING SOFTWARE INTERRUPT SERVICE ROUTINE BETWEEN HOST PROCESSOR AND EXTERNAL DEVICE WITH QUEUE ON HOST PROCESSOR AND HARDWARE QUEUE POINTERS ON EXTERNAL DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6130102 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE INCLUDING A DUAL INLAID STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6130548 | SIGNAL CONVERTING RECEIVER HAVING CONSTANT HYSTERESIS, AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6130821 | MULTI-CHIP ASSEMBLY HAVING A HEAT SINK AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6130920 | METHOD AND APPARATUS FOR ACCURATE SYNCHRONIZATION USING SYMBOL DECISION FEEDBACK |
| FREESCALE SEMICONDUCTOR, INC. | 6131017 | DUAL SYSTEM PORTABLE ELECTRONI C COMMUNICATOR |
| FREESCALE SEMICONDUCTOR, INC. | 6133093 | METHOD FOR FORMING AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6133100 | METHOD FOR MANUFACTURING A REA D ONLY MEMORY ARRAY |
| EDEECCALE CELAGONDIJOTOD 1310 | 6433564 | COMPARATION CIRCULATION METHOD |

6133764 COMPARATOR CIRCUIT AND METHOD

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6133797 | SELF CALIBRATING VCO CORRECTION CIRCUIT AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 6134675 | METHOD OF TESTING MULTI-CORE PROCESSORS AND MULTI-CORE PROCESSOR TESTING DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6136682 | METHOD FOR FORMING A CONDUCTIVE STRUCTURE HAVING A COMOSITE OR AMORPHOUS BARRIER LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 6137062 | BALL GRID ARRAY WITH RECESSED SOLDER BALLS |
| FREESCALE SEMICONDUCTOR, INC. | 6137154 | BIPOLAR TRANSISTOR WITH INCREA SED EARLY VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | 6137347 | MID SUPPLY REFERENCE GENERATOR |
| FREESCALE SEMICONDUCTOR, INC. | 6137429 | CIRCUIT AND METHOD FOR ATTENUA TING NOISE IN A DATA CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 6137852 | PHASE DETECTOR CIRCUIT AND MET HOD OF PHASE DETECTING |
| FREESCALE SEMICONDUCTOR, INC. | 6137995 | CIRCUIT AND METHOD OF GENERATI NG A PHASE LOCKED LOOP SIGNAL HAVING AN OFFSET REFERENCE |
| FREESCALE SEMICONDUCTOR, INC. | 6137999 | IMAGE REJECTION TRANSCEIVER AN D METHOD OF REJECTING AN IMAGE |
| FREESCALE SEMICONDUCTOR, INC. | 6140184 | FIELD EFFECT TRANSISTOR AND ME THOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 6140212 | SEMICONDUCTOR DEVICE AND METHO D THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6140703 | METHOD OF FORMING A SEMICONDUC TOR METALLIZATION SYSTEM AND S TRUCTURE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6143648 | METHOD FOR FORMING AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6144569 | SYSTEM AND METHOD FOR RECOVERING FROM A POWER SUPPLY INTERRUPTION |
| FREESCALE SEMICONDUCTOR, INC. | 6144845 | METHOD AND CIRCUIT FOR IMAGE R EJECTION |
| FREESCALE SEMICONDUCTOR, INC. | 6144846 | FREQUENCY TRANSLATION CIRCUIT AND METHOD OF TRANSLATING |
| FREESCALE SEMICONDUCTOR, INC. | 6145097 | METHOD AND APPARATUS FOR PROVIDING OPERAND FEED FORWARD SUPPORT IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6145104 | DATA PROCESSING SYSTEM EXTERNAL PIN CONNECTIVITY TO COMPLEX FUNCTIONS |
| FREESCALE SEMICONDUCTOR, INC. | 6145122 | DEVELOPMENT INTERFACE FOR A DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 6146948 | METHOD FOR MANUFACUTRING A THIN OXIDE FOR USE IN SEMICONDUCTOR INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 6146970 | CAPPED SHALLOW TRENCH ISOLATION AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 6147410 | ELECTRONIC COMPONENT AND METHO D OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6147551 | SWITCHED CAPACITOR CIRCUIT AND METHOD FOR REDUCING SAMPLING NOISE |
| FREESCALE SEMICONDUCTOR, INC. | 6148673 | DIFFERENTIAL PRESSURE SENSOR A ND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6149508 | CHEMICAL MECHANICAL PLANARIZAT ION SYSTEM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6150190 | METHOD OF FORMATION OF BURIED MIRROR SEMICONDUCTIVE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6150200 | SEMICONDUCTOR DEVICE AND METHO D OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 6150724 | MULTI-CHIP SEMICONDUCTOR DEVIC E AND METHOD FOR MAKING THE DEVICE BY USING MULTIPLE FLIP CHIP INTERFACES |
| FREESCALE SEMICONDUCTOR, INC. | 6150881 | AMPLIFIER CIRCUIT WITH AMPLTUD E AND PHASE CORRECTION AND MET HOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 6150889 | CIRCUIT AND METHOD FOR MINIMIZ ING RECOVERY TIME |
| FREESCALE SEMICONDUCTOR, INC. | 6150917 | PIEZORESISTIVE SENSOR AND METHOD |
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| Owner EDEESCALE SEMICONDUCTOR INC | Patent # | Description ARTIFICIAL NEURON AND METHOD O F USING SAME |
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| FREESCALE SEMICONDUCTOR, INC. | 6153519 | METHOD FOR DEPOSITING A DIFFUSION BARRIER |
| FREESCALE SEMICONDUCTOR, INC. FREESCALE SEMICONDUCTOR, INC. | 6153519 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6154369 | ELECTRONIC ASSEMBLY AND METHOD OF MANUFACTURE |
| , and the second | | |
| FREESCALE SEMICONDUCTOR, INC. | 6157583 | INTEGRATED CIRCUIT MEMORY HAVING A FUSE DETECT CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6157989 | DYNAMIC BUS ARBITRATION PRIORITY AND TASK SWITCHING BASED ON SHARED MEMORY FULLNESS IN A MULTI-PROCESSOR SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6157998 | METHOD FOR PERFORMING BRANCH PREDICTION AND RESOLUTION OF TWO OR MORE BRANCH INSTRUCTIONS WITHIN TWO OR MORE BRANCH PREDICTION BUFFERS |
| FREESCALE SEMICONDUCTOR, INC. | 6157999 | DATA PROCESSING SYSTEM HAVING A SYNCHRONIZING LINK STACK AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6159834 | METHOD OF FORMING A GATE QUALI TY OXIDE COMPOUND SEMICONDUCTOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6160280 | DOWN CONVERTER AND METHOD FOR GENERATING AN INTERMEDIATE FRE QUENCY SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 6160305 | BETA DEPENDENT TEMPERATURE SENSOR FOR AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6160490 | APPARATUS FOR IMPROVING THE BA TTERY LIFE OF A SELECTIVE CALL RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 6160842 | DEVICE AND METHOD FOR SERIALLY COMMUNICATING |
| FREESCALE SEMICONDUCTOR, INC. | 6160861 | METHOD AND APPARATUS FOR A FREQUENCY MODULATION PHASE LOCKED LOOP |
| FREESCALE SEMICONDUCTOR, INC. | 6161200 | METHOD AND APPARATUS FOR ANALYZING SOFTWARE EXECUTED IN EMBEDDED SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 6163063 | SEMICONDUCTOR DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6163835 | METHOD AND APPARATUS FOR TRANSFERRING DATA OVER A PROCESSOR INTERFACE BUS |
| FREESCALE SEMICONDUCTOR, INC. | 6166451 | RECTIFIER CIRCUIT HAVING FIRST AND SECOND INPUTS INTERCHANGE ABLY CONNECTED TO FIRST AND SE COND CONDUCTORS |
| FREESCALE SEMICONDUCTOR, INC. | 6166578 | CIRCUIT ARRANGEMENT TO COMPENSATE NON-LINEARITIES IN A RESISTOR, AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6166653 | SYSTEM FOR ADDRESS INITIALIZAT ION OF GENERIC NODES IN A DISTRIBUTED COMMAND AND CONTROL SYSTEM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6167081 | DUAL MODE RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 6167484 | METHOD AND APPARATUS FOR LEVERAGING HISTORY BITS TO OPTIMIZE MEMORY REFRESH PERFORMANCE |
| FREESCALE SEMICONDUCTOR, INC. | 6169408 | METHOD AND APPARATUS FOR TESTI NG AN INTEGRATED CIRCUIT WITH A PULSED RADIATION BEAM |
| FREESCALE SEMICONDUCTOR, INC. | 6169420 | OUTPUT BUFFER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6169800 | INTEGRATED CIRCUIT AMPLIFIER A ND METHOD FOR ADAPTIVE OFFSET |
| FREESCALE SEMICONDUCTOR, INC. | 6171910 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6171959 | METHOD FOR MAKING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6174425 | PROCESS FOR DEPOSITING A LAYER OF MATERIAL ON A SUBSTRATE AN D A PLATING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6177354 | METHOD OF ETCHING A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 6177832 | HIGH FREQUENCY DIFFERENTIAL TO SINGLE-ENDED CONVERTER |
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| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6178491 | METHOD FOR STORING DATA STRUCTURES IN MEMORY USING ADDRESS POINTERS, AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 6181168 | HIGH SPEED PHASE DETECTOR AND A METHOD FOR DETECTING PHASE DIFFERENCE |
| FREESCALE SEMICONDUCTOR, INC. | 6182104 | CIRCUIT AND METHOD OF MODULO M ULTIPLICATION |
| FREESCALE SEMICONDUCTOR, INC. | 6184072 | PROCESS FOR FORMING A HIGH-K GATE DIELECTRIC |
| FREESCALE SEMICONDUCTOR, INC. | 6184073 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE HAVING AN INTERCONECT OR CONDUCTIVE FILM ELECTRICALLY INSULATED FROM A CONDUCTIVE MEMBER OR REGION |
| FREESCALE SEMICONDUCTOR, INC. | 6185139 | CIRCUIT AND METHOD FOR ENABLING SEMICONDUCTOR DEVICE BURN-IN |
| FREESCALE SEMICONDUCTOR, INC. | 6185657 | MULTI-WAY CACHE APPARATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6187216 | METHOD FOR ETCHING A DIELECTRIC LAYER OVER A SEMICONDUCTOR SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 6189061 | MULTI-MASTER BUS SYSTEM PERFORMING ATOMIC TRANSACTIONS AND METHOD OF OPERATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6194246 | PROCESS FOR FABRICATING ELECTRONIC DEVICES HAVING A THERMALLY CONDUCTIVE SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 6194250 | LOW-PROFILE MICROELECTRIC PACK AGE, AND METHOD FOR FORMING SA ME |
| FREESCALE SEMICONDUCTOR, INC. | 6195536 | IMPEDANCE MATCHING FOR A DUAL BAND POWER AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 6198314 | SAMPLE AND HOLD CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6200829 | MICROELECTRONIC ASSEMBLY WITH CONNECTION TO A BURIED ELECTRI CAL ELEMENT, AND METHOD FOR FO RMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6201186 | ELECTRONIC COMPONENT ASSEMBLY AND METHOD OF MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6201192 | METHOD AND ASSEMBLY FOR PROVID ING INPROVED UNDERCHIP ENCAPSU LATION |
| FREESCALE SEMICONDUCTOR, INC. | 6204783 | DIGITAL TO ANALOG CONVERTER HAVING A DC OFFSET CANCELLING DEVICE AND A METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6208205 | AMPLIFIER CIRCUIT AND METHOD FOR REDUCING NOISE THEREIN |
| FREESCALE SEMICONDUCTOR, INC. | 6208211 | LOW JITTER PHASE LOCKED LOOP HAVING A SIGMA DELTA MODULATOR AND A METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6215359 | IMPEDANCE MATCHING FOR A DUAL BAND POWER AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 6215423 | METHOD AND SYSTEM FOR A SYNCHRONOUS SAMPLE RATE CONVERSION USING A NOISE-SHAPED NUMERICALLY CONTROL OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | 6215834 | DUAL BANDWIDTH PHASE LOCKED LO OP FREQUENCY LOCK DETECTION SY STEM AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6217660 | METHOD OF CLEANING A THROTTLE VALVE AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 6218200 | MULTI-LAYER REGISTRATION CONTROL FOR PHOTOLITHOGRAPHY PROCESSES |
| FREESCALE SEMICONDUCTOR, INC. | 6218302 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6222236 | PROTECTION CIRCUIT AND METHOD FOR PROTECTING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6222420 | MINIMIZING RECOVERY TIME |
| FREESCALE SEMICONDUCTOR, INC. | 6224669 | METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE HAVING A CRYSTALLINE ALKALINE EARTH METAL OXIDE INTERFACE WITH SILICON |
| FREESCALE SEMICONDUCTOR, INC. | 6225144 | A METHOD AND MACHINE FOR UNDER FILLING AN ASSEMPLY TO FORM A SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 6225674 | SEMICONDUCTOR STRUCTURE AND ME THOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6226556 | APPARATUS WITH FAILURE RECOVERY AND METHOD THEREFORE |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6226724 | MEMORY CONTROLLER AND METHOD FOR GENERATING COMMANDS TO A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 6228275 | METHOD OF MANUFACTURING A SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | 6228743 | SEMICONDUCTOR DEVICE AND ALIGNMENT METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6229097 | SUBSTRATE HAVING TRIM WINDOW IN A C5 ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | 6229400 | METHOD AND APPARATUS FOR A CALIBRATED FREQUENCY MODULATION PHASE LOCKED LOOP |
| FREESCALE SEMICONDUCTOR, INC. | 6230238 | METHOD AND APPARATUS FOR ACCESSING MISALIGNED DATA FROM MEMORY IN AN EFFICIENT MANNER |
| FREESCALE SEMICONDUCTOR, INC. | 6231743 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6232634 | NONVOLATILE MEMORY CELL AND ME THOD FOR MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6235603 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE USING AN ETCH STOP LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 6236611 | PEAK PROGRAM CURRENT APPARATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6237089 | METHOD AND APPARATUS FOR AFFECTING SUBSEQUENT INSTRUCTION PROCESSING IN A DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 6238967 | METHOD OF FORMING EMBEDDED DRAM STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6239636 | DIGITAL WAVEFORM GENERATOR APPARATUS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6240024 | METHOD AND APPARATUS FOR GENERATING AN ECHO CLOCK IN A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 6240479 | METHOD AND APPARATUS FOR TRANSFERRING DATA ON A SPLIT BUS IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6240493 | METHOD AND APPARATUS FOR PERFORMING ACCESS CENSORSHIP IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6241821 | METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE HAVING A CR YSTALLINE ALKALINE EARTH METAL OXIDE INTERFACE WITH SILICON |
| FREESCALE SEMICONDUCTOR, INC. | 6242802 | MOISURE ENHANCED BALL GRID ARRAY PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 6242892 | PORTABLE ELECTRONIC DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6242956 | PHASE LOCKED LOOP |
| FREESCALE SEMICONDUCTOR, INC. | 6243566 | IMPEDANCE MATCHING FOR A DUAL BAND POWER AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 6243802 | APPARATUS AND METHOD FOR ENCRY PTED INSTRUCTIONS |
| FREESCALE SEMICONDUCTOR, INC. | 6245686 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE AND A PROCESS FOR OPERATING AN APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 6249170 | LOGARITHMIC GAIN CONTROL CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6249857 | APPARATUS USING A MULTIPLE INS TRUCTION REGISTER LOGARITHM BA SEI PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 6251734 | METHOD FOR FABRICATING TRENCH ISOLATION AND TRENCH SUBSTRATE CONTACT |
| FREESCALE SEMICONDUCTOR, INC. | 6254815 | MOLDED PACKAGING METHOD FOR A SENSING DIE HAVING A PRESSURE SENSING DIAPHRAGM |
| FREESCALE SEMICONDUCTOR, INC. | 6255204 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6255710 | 3-D SMART POWER IC |
| FREESCALE SEMICONDUCTOR, INC. | 6257756 | APPARATUS AND METHOD FOR IMPLEMENTING VITERBI BUTTERFLIES |
| FREESCALE SEMICONDUCTOR, INC. | 6259904 | EAST SQUELCH CIRCUIT AND METHOD |
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WORDS

6260086 CONTROLLER CIRCUIT FOR TRANSFERRING A SET OF PERIPHERAL DATA

| Owner | Patent # | Description |
|-------------------------------|----------|---|
| FREESCALE SEMICONDUCTOR, INC. | 6261868 | SEMICONDUCTOR COMPONENT AND ME THOD FOR MANUFACTURING THE SEM ICONDUCTOR COMPONENT |
| FREESCALE SEMICONDUCTOR, INC. | 6261978 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE WITH THICK AND THIN FILMS |
| FREESCALE SEMICONDUCTOR, INC. | 6262451 | ELECTRODE STRUCTURE FOR TRANSI STORS NON-VOLATILE MEMORIES AN D THE LIKE |
| FREESCALE SEMICONDUCTOR, INC. | 6262461 | METHOD AND APPARATUS FOR CREAT ING A VOLTAGE THRESHOLD IN A F ET |
| FREESCALE SEMICONDUCTOR, INC. | 6265329 | QUANTUM DEPOSITION DISTRIBUTIO N CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 6265917 | CIRCUIT AND METHOD FOR ALTERING THE FREQUENCY OF A SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 6267641 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND CHEMICAL-MECHANICAL POLISHING SYSTEM THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6268289 | METHOD FOR PROTECTING THE EDGE EXCULUSION OF A SEMICONDUCTOR WAFER FROM COPPER PLATING THROUGH USE OF AN EDGE EXCLUSION MASKING LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 6271106 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT |
| FREESCALE SEMICONDUCTOR, INC. | 6271143 | METHOD FOR PREVENTING TRENCH FILL EROSION |
| FREESCALE SEMICONDUCTOR, INC. | 6271699 | DRIVER CIRCUIT AND METHOD FOR CONTROLLING TRANSITION TIME OF A SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 6272588 | METHOD AND APPARATUS FOR VERIF YING AND CHARACTERIZING DATA R ETENTION TIME IN A DRAM USING BUILT-IN TEST CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | 6274424 | SEMICONDUCTOR DEVICE INCLUDING A DUAL INLAID STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6274478 | A METHOD FOR FORMING A COPPER INTERCONNECT USING A MULTI-PLATEN CHEMICAL MECHANICAL POLISHING (CMP) PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 6274515 | SPIN-ON DIELECTRIC FOR USE IN MANUFACTURING SEMICONDUCTORS |
| FREESCALE SEMICONDUCTOR, INC. | 6274899 | SEMICONDUCTOR DEVICE CAPACITOR ELECTRODE |
| FREESCALE SEMICONDUCTOR, INC. | 6275178 | VARIABLE CAPACITANCE VOLTAGE SHIFTER AND AMPLIFIER AND A METHOD FOR AMPLIFYING AND SHIFTING VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | 6275835 | FINITE IMPULSE RESPONSE FILTER AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6278158 | VOLTAGE VARIABLE CAPACITOR WITH IMPROVED C-V LINEARITY |
| FREESCALE SEMICONDUCTOR, INC. | 6278394 | A SIGNAL PROCESSING CIRCUIT AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 6284616 | CIRCUIT AND METHOD FOR REDUCING PARASITIC BIPOLAR EFFECTS DURING ELECTROSTATIC DISCHARGES |
| FREESCALE SEMICONDUCTOR, INC. | 6284633 | METHOD FOR FORMING A TENSILE PLASMA ENHANCED NITRIDE CAPPING LAYER OVER A GATE ELECTRODE |
| FREESCALE SEMICONDUCTOR, INC. | 6285066 | SEMICONDUCTOR DEVICE HAVING FIELD ISOLATION |
| FREESCALE SEMICONDUCTOR, INC. | 6285073 | CONTACT STRUCTURE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 6285214 | OUTPUT BUFFER STAGE FOR USE WITH A CURRENT CONTROLLED OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | 6287951 | PROCESS FOR FORMING A COMBINATION HARDMASK AND ANTIREFLECTIVE LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 6287960 | SELF ALIGNED INLAID PATTERNING AND ETCHING |
| FREESCALE SEMICONDUCTOR, INC. | 6288599 | DATA PROCESSING SYSTEM HAVING AN INPUT BUFFER WHICH INTERFACES UNDER ADDRESS CONTROL WITH CIRCUITRY OPERATING WITH A DIFFERENT SUPPLY VOLTAGE VALUE |
| FREESCALE SEMICONDUCTOR, INC. | 6289204 | INTEGRATION OF A RECEIVER FRON T-END IN MULTILAYER CERAMIC IN TEGRATED CIRCUIT TECHNOLOGY |
| FREESCALE SEMICONDUCTOR, INC. | 6291319 | METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE HAVING A STABLE CRYSTALLINE INTERFACE WITH SILICON |
| FREESCALE SEMICONDUCTOR, INC. | 6292034 | LOW NOISE TRANSCONDUCTANCE DEVICE |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6294405 | METHOD OF FORMING SEMICONDUCTOR DEVICE HAVING A SUB-CHIP-SCALE PACKAGE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6294820 | A METAL OXIDE GATE ELECTRODE STACK HAVING A METALLIC GATE DIELECTRIC, METALLIC GATE ELECTRODE AND A METALLIC ARC LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 6294933 | METHOD AND APPARATUS FOR LOW POWER DIFFERENTIAL SIGNALING TO REDUCE POWER |
| FREESCALE SEMICONDUCTOR, INC. | 6294938 | SYSTEM WITH DLL |
| FREESCALE SEMICONDUCTOR, INC. | 6295229 | SEMICONDUCTOR DEVICE AND METHODS OF FORMING AND OPERATING IT |
| FREESCALE SEMICONDUCTOR, INC. | 6297095 | MEMORY DEVICE THAT INCLUDES PASSIVATED NANOCLUSTERS AND METHOD FOR MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6297155 | METHOD OF FORMING A COPPER LAYER OVER A SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 6297173 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6297757 | METHOD AND CIRCUIT FOR TESTING AN ANALOG-TO-DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 6298464 | METHOD AND APPARATUS FOR MAXIM UM LIKELIHOOD SEQUENCE DETECTI ON |
| FREESCALE SEMICONDUCTOR, INC. | 6300202 | SELECTIVE REMOVAL OF A METAL OXIDE DIELECTRIC |
| FREESCALE SEMICONDUCTOR, INC. | 6300234 | PROCESS FOR FORMING AN ELECTRICAL DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6300884 | METHOD FOR DECODING A QUADRATURE ENCODED SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 6304843 | METHOD AND APPARATUS FOR RECONSTRUCTING A LINEAR PREDICTION |
| FREESCALE SEMICONDUCTOR, INC. | 6305708 | AIRBAG DEPLOYMENT SYSTEM AND M ETHOD FOR MONITORING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6307169 | MICRO-ELECTROMECHANICAL SWITCH |
| FREESCALE SEMICONDUCTOR, INC. | 6307298 | ACTUATOR AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6307452 | FOLDED SPRING BASED MICRO ELECTROMECHANICAL RF SWITCH |
| FREESCALE SEMICONDUCTOR, INC. | 6307782 | PROCESS FOR OPERATING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6307904 | CLOCK RECOVERY CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6308308 | SEMICONDUCTOR DEVICE USING DIODE PLACE-HOLDERS AND METHOD OF MANUFACTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6309908 | A PACKAGE FOR AN ELECTRONIC COMPONENT AND METHOD OF MAKING IT |
| FREESCALE SEMICONDUCTOR, INC. | 6309912 | METHOD OF INTERCONNECTING AN EMBEDDED INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6310403 | METHOD OF MANUFACTURING COMPONENTS AND COMPONENT THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6311327 | METHOD AND APPARATUS FOR ANALYZING SOFTWARE IN A LANGUAGE-INDEPENDENT MANNER |
| FREESCALE SEMICONDUCTOR, INC. | 6313024 | METHOD FOR FORMING AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6313567 | LITHOGRAPHY CHUCK HAVING PIEZOELECTRIC ELEMENTS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6313664 | LOAD CAPACITANCE COMPENSATED BUFFER AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6313774 | DELTA-SIGMA ANALOG-TO-DIGITAL CONVERTER, AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6314023 | NON-VOLATILE PROGRAMMING ELEMENTS FOR REDUNDANCY AND IDENTIFICATION IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6316164 | PROXIMITY EFFECT CORRECTION METHOD THROUGH UNIFORM REMOVAL OF FRACTION OF INTERIOR PIXELS |
| FREESCALE SEMICONDUCTOR, INC. | 6316359 | INTERCONNECT STRUCTURE IN A SEMICONDUCTOR DEVICE AND METHOD OF |

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| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6316968 | SENSE AMPLIFIER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6317474 | METHOD AND APPARATUS FOR ESTIMATING TIME-OF-ARRIVAL OF A SYNCHRONIZATION SIGNAL SENT SIMULTANEOUSLY FROM AT LEAST TWO NON-COLLOCATED TRANSMITTERS |
| FREESCALE SEMICONDUCTOR, INC. | 6318174 | SENSOR AND METHOD OF USE |
| FREESCALE SEMICONDUCTOR, INC. | 6319730 | METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE INCLUDING A METAL OXIDE INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | 6320425 | DUAL FET DIFFERENTIAL VOLTAGE CONTROLLED ATTENUATOR |
| FREESCALE SEMICONDUCTOR, INC. | 6320784 | MEMORY CELL AND METHOD FOR PROGRAMMING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6323704 | MULTIPLE VOLTAGE COMPATIBLE I/O BUFFER |
| FREESCALE SEMICONDUCTOR, INC. | 6326228 | SENSOR AND METHOD OF FABRICATI ON |
| FREESCALE SEMICONDUCTOR, INC. | 6326554 | SURFACE MOUNT FLEXIBLE INTERCONNECT AND COMPONENT CARRIER |
| FREESCALE SEMICONDUCTOR, INC. | 6326811 | OUTPUT BUFFER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6327126 | ELECTROSTATIC DISCHARGE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6327182 | SEMICONDUCTOR DEVICE AND A METHOD OF OPERATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6327647 | METHOD AND APPARATUS FOR INTERFACING A PROCESSOR TO A COPROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 6329692 | CIRCUIT AND METHOD FOR REDUCING PARASITIC BIPOLAR EFFECTS DURING ELECTROSTATIC DISCHARGES |
| FREESCALE SEMICONDUCTOR, INC. | 6330184 | METHOD OF OPERATING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6330234 | METHOD AND APPARATUS FOR REDUCING CURRENT CONSUMPTION |
| FREESCALE SEMICONDUCTOR, INC. | 6342411 | ELECTRONIC COMPONENT AND METHOD FOR MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6344403 | MEMORY DEVICE AND METHOD FOR MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6344413 | METHOD OF FORMING A SEMICONDUC TOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6346469 | SEMICONDUCTOR DEVICE AND A PROCESS FOR FORMING THE SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6346829 | HIGH VOLTAGE INPUT BUFFER MADE BY A LOW VOLTAGE PROCESS AND HAVING A SELF-ADJUSTING TRIGGER POINT |
| FREESCALE SEMICONDUCTOR, INC. | 6346832 | MULTI-CHANNEL SIGNALING |
| FREESCALE SEMICONDUCTOR, INC. | 6346880 | CIRCUIT AND METHOD FOR CONTROLLING AN ALARM |
| FREESCALE SEMICONDUCTOR, INC. | 6346908 | APPARATUS FOR CONVERTING AN ANALOG SIGNAL UTILIZING RESISTOR D/A CONVERTER PRECHARGING |
| FREESCALE SEMICONDUCTOR, INC. | 6347056 | RECORDING OF RESULT INFORMATION IN A BUILT-IN SELF-TEST CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6348386 | METHOD FOR MAKING A HAFNIUM-BASED INSULATING FILM |
| FREESCALE SEMICONDUCTOR, INC. | 6348820 | HIGH-SIDE, LOW-SIDE CONFIGURABLE DRIVER |
| FREESCALE SEMICONDUCTOR, INC. | 6350954 | ELECTRONIC DEVICE PACKAGE, AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6351020 | LINEAR CAPACITOR STRUCTURE IN A CMOS PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 6351246 | PLANAR ULTRA WIDE BAND ANTENNA WITH INTEGRATED ELECTRONICS |
| FREESCALE SEMICONDUCTOR, INC. | 6352192 | SYSTEM AND METHOD TO CONTROL SOLDER REFLOW FURNACE WITH WAFER SURFACE CHARACTERIZATION |

6352874 METHOD OF MANUFACTURING A SENSOR

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6353296 | ELECTRONIC DRIVER CIRCUIT WITH MULTIPLEXER FOR ALTERNATIVELY DRIVING A LOAD FOR A BUSLINE, AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6355550 | ULTRA-LATE PROGRAMMING ROM AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6356142 | DIGITAL FILTER TUNE LOOP |
| FREESCALE SEMICONDUCTOR, INC. | 6356594 | DATA CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 6356636 | CIRCUIT AND METHOD FOR FAST MODULAR MULTIPLICATION |
| FREESCALE SEMICONDUCTOR, INC. | 6358816 | METHOD FOR UNIFORM POLISH IN MICROELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6359294 | INSULATOR COMPOUND SEMICONDUCT OR INTERFACE STRUCTURE AND MET HODS OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 6359458 | APPARATUS FOR DETECTING A DIAPHRAGM FAILURE |
| FREESCALE SEMICONDUCTOR, INC. | 6360243 | METHOD, DEVICE AND ARTICLE OF MANUFACTURE FOR IMPLEMENTING A REAL-TIME TASK SCHEDULING ACC ELERATOR |
| FREESCALE SEMICONDUCTOR, INC. | 6362018 | MEMS VARIABLE CAPACITOR WITH STABILIZED ELECTROSTATIC DRIVE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6362071 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE WITH AN OPENING IN A DIELECTRIC LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 6362089 | METHOD FOR PROCESSING A SEMICONDUCTOR SUBSTRATE HAVING A COPPER SURFACE DISPOSED THEREON AND STRUCTURE FORMED |
| FREESCALE SEMICONDUCTOR, INC. | 6365474 | SEMICONDUCTOR DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6366157 | METHODS AND CIRCUITS FOR SYNAM ICALLY ADJUSTING A SUPPLY VOLT AGE AND/OR A FREQUENCY OF A CL OCK SIGNAL IN A DIGITAL CIRCUI |
| FREESCALE SEMICONDUCTOR, INC. | 6366768 | CIRCUIT AND METHOD OF FREQUENC Y SYNTHESIZER CONTROL WITH A S ERIAL PERIPHERAL INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | 6366786 | RADIO WITH SYNCHRONIZATION APP ARATUS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6366865 | APPARATUS AND METHOD FOR ESTIMATING THE COIL RESISTANCE AND ELECTRIC MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | 6368924 | AMORPHOUS CARBON LAYER FOR IMPROVED ADHESION OF PHOTORESIST AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 6368929 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND SEMICONDUCTOR COMPONENT THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6369647 | DEMODULATOR CIRCUIT AND METHOD OF TUNING |
| FREESCALE SEMICONDUCTOR, INC. | 6369742 | SELECTIVE OVER-RANGING IN FOLDING AND AVERAGING INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 6372622 | FINE PITCH BUMPING WITH IMPROVED DEVICE STANDOFF AND BUMP VOLUME |
| FREESCALE SEMICONDUCTOR, INC. | 6372638 | A METHOD FOR FORMING A CONDUCTIVE PLUG BETWEEN CONDUCTIVE LAYERS OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6372665 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6373104 | CIRCUIT AND METHOD FOR REDUCIN G PARASITIC BIPOLAR EFFECTS DURING ELECTROSTATIC DISCHARGES |
| FREESCALE SEMICONDUCTOR, INC. | 6373139 | LAYOUT FOR A BALL GRID ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | 6373271 | SEMICONDUCTOR FRONT SIDE PRESSURE TESTING SYSTEM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6376349 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE AND A CONDUCTIVE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6376371 | METHOD OF FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6377125 | DISTRIBUTED AMPLIFIER HAVING SEPARATELY BIASED SECTIONS |
| FREESCALE SEMICONDUCTOR, INC. | 6378022 | METHOD AND APPARATUS FOR PROCESING INTERRUPTIBLE MULTI-CYCLE INSTRUCTIONS |
| FREESCALE SEMICONDUCTOR, INC. | 6379744 | METHOD FOR COATING AN INTEGRAT ED CIRCUIT SUBSTRATE |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6380760 | INTEGRATED CIRCUIT FOR HANDLING BUFFER CONTENTION AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6380811 | SIGNAL GENERATOR AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6381224 | METHOD AND APPARATUS FOR CONTROLLING A FULL-DUPLEX COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6381656 | METHOD AND APPARATUS FOR MONITORING INPUT/OUTPUT ("I/O") PERFORMANCE IN I/O PROCESSORS |
| FREESCALE SEMICONDUCTOR, INC. | 6383873 | PROCESS FOR FORMING A STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6383885 | BIPOLAR TRANSISTOR WITH IMPROVED REVERSE BREAKDOWN CHARACTERISTICS |
| FREESCALE SEMICONDUCTOR, INC. | 6384353 | MICRO-ELECTROMECHANICAL SYSTEM DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6385021 | ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6385101 | PROGRAMMABLE DELAY CONTROL FOR SENSE AMPLIFIERS IN A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 6387787 | LITHOGRAPHIC TEMPLATE AND METHOD OF FORMATION AND USE |
| FREESCALE SEMICONDUCTOR, INC. | 6389489 | DATA PROCESSING SYSTEM HAVING A FIFO BUFFER WITH VARIABLE THRESHOLD VALUE BASED ON INPUT AND OUTPUT DATA RATES AND DATA BLOCK SIZE |
| FREESCALE SEMICONDUCTOR, INC. | 6389706 | WAFER CONTAINER HAVING ELECTRICALLY CONDUCTIVE KINEMATIC COUPLING GROOVE, SUPPORT SURFACE WITH ELECTRICALLY CONDUCTIVE KINEMATIC COUPLING PIN, TRANSPORTATION SYSTEM, AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6391762 | METHOD OF FORMING A MICROELECTRIC ASSEMBLY WITH A PARTICULATE FREE UNDERFILL MATERIAL AND A MICROELECTRONIC ASSEMBLY INCORPORATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6392257 | SEMICONDUCTOR STRUCTURE, SEMICONDUCTOR DEVICE, COMMUNICATING DEVICE, INTEGRATED CIRCUIT, AND PROCESS FOR FABRICATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6392558 | SYSTEM FOR ADDRESS INITIALIZATION OF GENERIC NODES IN A DISTRIBUTED COMMAND AND CONTROL SYSTEM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6395053 | METHOD OF FORMING METAL COLLOIDS, METAL COLLOIDS AND METHOD OF FORMING A METAL OXIDE SENSITIVE LAYER FOR A CHEMICAL SENSOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6396158 | SEMICONDUCTOR DEVICE AND A PROCESS FOR DESIGNING A MASK |
| FREESCALE SEMICONDUCTOR, INC. | 6400610 | MEMORY DEVICE INCLUDING ISOLATED STORAGE ELEMENTS THAT UTILIZE HOLE CONDUCTION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6401196 | DATA PROCESSING SYSTEM HAVING BRANCH CONTROL AND METHOD THER EOF |
| FREESCALE SEMICONDUCTOR, INC. | 6401536 | ACCELERATION SENSOR AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6401545 | MICRO ELECTRO-MECHANICAL SYSTEM SENSOR WITH SELECTIVE ENCAPSULATION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6404283 | METHOD AND APPARATUS FOR AMPLIFYING A RADIO FREQUENCY SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 6404912 | METHOD AND APPARATUS FOR VISUALLY INSPECTING AN OBJECT |
| FREESCALE SEMICONDUCTOR, INC. | 6406555 | POINT OF USE DILUTION TOOL AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6406791 | MULTIPHASE DIALECTRIC COMPOSITION AND MULTILAYERED DEVICE INCORPORATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6406976 | SEMICONDUCTOR DEVICE AND PROCESS FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6407634 | LINEAR ENVELOPE TRACKING RF POWER AMPLIFIER WITH ADAPTIVE ANALOG SIGNAL PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 6408023 | METHOD AND APPARATUS FOR PERFO RMING EQUALISATION IN A RADIO RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 6410861 | LOW PROFILE INTERCONNECT STRUCTURE |

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| FREESCALE SEMICONDUCTOR, INC. | 6410941 | RECONFIGURABLE SYSTEMS USING HYBRID INTEGRATED CIRCUITS WITH OPTICAL PORTS |
| FREESCALE SEMICONDUCTOR, INC. | 6411116 | A METHOD FOR TESTING A PRODUCT INTEGRATED CIRCUIT WAFER USIN G A STIMULUS INTEGRATED CIRCUI T WAFER |
| FREESCALE SEMICONDUCTOR, INC. | 6411226 | HUFFMAN DECODER WITH REDUCED MEMORY SIZE |
| FREESCALE SEMICONDUCTOR, INC. | 6411232 | METHOD AND SYSTEM FOR DETERMINING AN ELEMENT CONVERSION CHARACTERISTIC CONTEMPORANEOUS WITH CONVERTING AN INPUT SIGNAL IN A SIGNAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 6411758 | METHOD AND APPARATUS FOR ALIGNING A WAVEGUIDE TO A DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6413806 | SEMICONDUCTOR DEVICE AND METHOD FOR PROTECTING SUCH DEVICE FROM A REVERSED DRAIN VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | 6413819 | MEMORY DEVICE AND METHOD FOR USING PREFABRICATED ISOLATED STORAGE ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | 6413878 | METHOD OF MANUFACTURING ELECTRONIC COMPONENTS |
| FREESCALE SEMICONDUCTOR, INC. | 6414562 | CIRCUIT AND METHOD FOR IMPEDAN CE MATCHING |
| FREESCALE SEMICONDUCTOR, INC. | 6414613 | APPARATUS FOR NOISESHAPING A PULSE WIDTH MODULATION (PWM) SIGNAL AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6418029 | INTERCONNECT SYSTEM HAVING VERTICALLY MOUNTED PASSIVE COMPONENTS ON AN UNDERSIDE OF A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 6418489 | DIRECT MEMORY ACCESS CONTROLLER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6418527 | DATA PROCESSOR INSTRUCTION SYSTEM FOR GROUPING INSTRUCTION WITH OR WITHOUT A COMMON PREFIX AND DATA PROCESSING SYSTEM THAT USES TWO OR MORE INSTRUCTION GROUPING METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 6420098 | METHOD AND SYSTEM FOR MANUFACTURING SEMICONDUCTOR DEVICES ON A WAFER |
| FREESCALE SEMICONDUCTOR, INC. | 6420208 | AN ALTERNATIVE GROUND CONTACT FOR A SEMICONDUCTOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | 6420923 | LOW SUPPLY CURRENT CONTROLLED FET P1 ATTENUATOR |
| FREESCALE SEMICONDUCTOR, INC. | 6421744 | DIRECT MEMORY ACCESS CONTROLLER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6423619 | TRANSISTOR METAL GATE STRUCTURE THAT MINIMIZES NON-PLANARITY EFFECTS AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 6423638 | FILTER APPARATUS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6423991 | FIELD EFFECT TRANSISTOR AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 6426239 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6426683 | INTEGRATED FILTER WITH IMPROVED I/O MATCHING AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 6426698 | LOT SIGNALLING DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6427066 | APPARATUS AND METHOD FOR EFFECTING COMMUNICATIONS AMONG A PLURALITY OF REMOTE STATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 6429030 | METHOD AND APPARATUS FOR TESTI NG A SEMICONDUCTOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | 6429046 | FLIP CHIP DEVICE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6429103 | MOCVD-GROWN EMODE HIGFET BUFFER |
| FREESCALE SEMICONDUCTOR, INC. | 6429531 | METHOD AND APPARATUS FOR MANUFACTURING AN INTERCONNECT STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6430666 | LINKED LIST MEMORY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6432779 | SELECTIVE REMOVAL OF A METAL OXIDE DIELECTRIC |
| FREESCALE SEMICONDUCTOR, INC. | 6433382 | SPLIT-GATE VERTICALLY ORIENTATED EEPROM DEVICE AND PROCESS |

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| FREESCALE SEMICONDUCTOR, INC. | 6433568 | MASSIVE PARALLEL SEMICONDUCTOR MANUFACTURING TEST PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 6433571 | PROCESS FOR TESTING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6433626 | CURRENT MODE FILTER WITH COMPLEX ZEROS |
| FREESCALE SEMICONDUCTOR, INC. | 6434698 | MICROPROCESSOR MODULE AND METH OD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6434707 | LOW JITTER CLOCK GENERATION WI THOUT SINE LOOK-UP TABLES |
| FREESCALE SEMICONDUCTOR, INC. | 6434721 | METHOD AND APPARATUS FOR CONSTRAINT GRAPH BASED LAYOUT COMPACTION FOR INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 6436300 | METHOD OF MANUFACTURING ELECTRONIC COMPONENTS |
| FREESCALE SEMICONDUCTOR, INC. | 6436730 | MICROELECTRONIC PACKAGE COMPRISING TIN-COPPER BUMP INTERCONNECTIONS, AND METHOD FOR FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6440805 | METHOD OF FORMING A SEMICONDUCTOR DEVICE WITH ISOLATION AND WELL REGIONS |
| FREESCALE SEMICONDUCTOR, INC. | 6441449 | MEMS VARIABLE CAPACITOR WITH STABILIZED ELECTROSTATIC DRIVE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6441594 | LOW POWER VOLTAGE REGULATOR WITH IMPROVED ON-CHIP NOISE ISOLATION |
| FREESCALE SEMICONDUCTOR, INC. | 6441688 | SINGLE-TO-DIFFERENTIAL BUFFER AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 6444512 | DUAL METAL GATE TRANSISTORS FOR CMOS PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 6444545 | DEVICE STRUCTURE FOR STORING CHARGE AND METHOD THEREFORE |
| FREESCALE SEMICONDUCTOR, INC. | 6444563 | METHOD AND APPARATUS FOR EXTENDING FATIGUE LIFE OF SOLDER JOINTS IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6444569 | A METHOD FOR FORMING A COPPER INTERCONNECT USING A MULTI-PLATEN CHEMICAL MECHANICAL POLISHING (CMP) PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 6448192 | METHOD FOR FORMING A HIGH DIELECTRIC CONSTANT MATERIAL |
| FREESCALE SEMICONDUCTOR, INC. | 6448736 | METHOD FOR CONTROLLING SWITCHED RELUCTANCE MOTOR, AND CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | 6449195 | METHOD AND APPARATUS FOR COUPLING NOISE REDUCTION IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6449675 | MULTIFIELD REGISTER HAVING A SELECTION FIELD FOR SELECTING A SOURCE OF AN INFORMATION FIELD |
| FREESCALE SEMICONDUCTOR, INC. | 6451127 | CONDUCTIVE PASTE AND SEMICONDU CTOR COMPONENT HAVING CONDUCTIVE BUMMPS MADE FROM THE CONDUC TIVE PASTE |
| FREESCALE SEMICONDUCTOR, INC. | 6451181 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE BARRIER LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 6451627 | SEMICONDUCTOR DEVICE AND PROCESS FOR MANUFACTURING AND PACAKAGING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6451681 | METHOD OF FORMING COPPER INTERCONNECTION UTILIZING ALUMINUM CAPPING FILM |
| FREESCALE SEMICONDUCTOR, INC. | 6452284 | SEMICONDUCTOR DEVICE SUBSTRATE AND A PROCESS FOR ALTERING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6452445 | VOLTAGE CONTROLLED VARIABLE GAIN ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 6453749 | PHYSICAL SENSOR COMPONENT |
| FREESCALE SEMICONDUCTOR, INC. | 6458622 | STRESS COMPENSATION COMPOSITION AND SEMICONDUCTOR COMPONENT FORMED USING THE STRESS COMPENSATION COMPOSITION |
| FREESCALE SEMICONDUCTOR, INC. | 6459156 | SEMICONDUCTOR DEVICE, A PROCESS FOR A SEMICONDUCTOR DEVICE, AND A PROCESS FOR MAKING A MASKING DATABASE |
| FREESCALE SEMICONDUCTOR, INC. | 6459325 | OUTPUT BUFFER HAVING A PRE-DRIVER TRANSITION CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | 6461898 | TWO STEP WIRE BOND PROCESS |

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| FREESCALE SEMICONDUCTOR, INC. | 6461914 | PROCESS FOR MAKING A MIM CAPACITOR |
| FREESCALE SEMICONDUCTOR, INC. | 6461925 | METHOD OF MANUFACTURING A HETEROJUNCTION BICMOS INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6462360 | INTEGRATED GALLIUM ARSENIDE COMMUNICATION SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 6462789 | CIRCUIT AND METHOD FOR GENERAT ING CHROMINANCE LOCK |
| FREESCALE SEMICONDUCTOR, INC. | 6463549 | A DEVICE AND METHOD FOR PATCHING CODE RESIDING ON A READ ONLY MEMORY MODULE |
| FREESCALE SEMICONDUCTOR, INC. | 6465281 | METHOD OF MANUFACTURING A SEMICONDUCTOR WAFER LEVEL PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 6465297 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND SEMICONDUCTOR COMPONENT THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6465743 | MULTI-STRAND SUBSTRATE FOR BALL-GRID ARRAY ASSEMBLIES AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6465853 | METHOD FOR MAKING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6469536 | A METHOD AND DEVICE FOR TESTING AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6472243 | METHOD OF FORMING AN INTEGRATED CMOS CAPACITIVE PRESSURE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | 6472276 | USING SILICATE LAYERS FOR COMPOSITE SEMICONDUCTOR STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | 6472694 | MICROPROCESSOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6473605 | NOISE REDUCTION AND RANGE CONTROL FOR AN AM/FM DUAL RADIO SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6473606 | COMMON INTERMEDIATE FREQUENCY BROADCAST RADIO FRONT END |
| FREESCALE SEMICONDUCTOR, INC. | 6475930 | UV CURE PROCESS AND TOOL FOR LOW K FILM FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 6476506 | PACKAGED SEMICONDUCTOR WITH MULTIPLE ROWS OF BOND PADS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6477285 | INTEGRATED CIRCUITS WITH OPTICAL SIGNAL PROPAGATION |
| FREESCALE SEMICONDUCTOR, INC. | 6477477 | EXTENDED BASE BAND MULTICARRIER SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6477608 | INTERFACE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6477640 | APPARATUS FOR PERFORMING BRANCH PREDICTION AND RESOLUTION OF TWO OR MORE BRANCH INSTRUCTIONS WITHIN TWO OR MORE BRANCH PREDICTION BUFFERS |
| FREESCALE SEMICONDUCTOR, INC. | 6477679 | METHODS FOR DECODING DATA IN DIGITAL COMMUNICATION SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 6477681 | METHODS FOR DECODING DATA IN DIGITAL COMMUNICATION SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 6479310 | METHOD AND APPARATUS FOR TESTING A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6479843 | SINGLE SUPPLY HFET WITH TEMPERATURE COMPENSATION |
| FREESCALE SEMICONDUCTOR, INC. | 6482073 | TRANSLATION MECHANISM FOR A CHEMICAL MECHANICAL PLANARIZATION SYSTEM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6483885 | FRAME SYNCHRONIZER |
| FREESCALE SEMICONDUCTOR, INC. | 6487240 | APPARATUS FOR RECEIVING AND RECOVERING FREQUENCY SHIFT KEYED SYMBOLS |
| FREESCALE SEMICONDUCTOR, INC. | 6487670 | METHOD FOR DETECTING AND FOR RESPONDING TO DETECTION OF A BATTERY TO A LOGIC DEVICE AND SYSTEMS RELATING THERETO |
| FREESCALE SEMICONDUCTOR, INC. | 6489083 | SELECTIVE SIZING OF FEATURES TO COMPENSATE FOR RESIST THICKNESS VARITATIONS IN SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 6489211 | SEIMCONDUCTOR COMPONENT AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6489229 | METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING CONDUCTIVE |

BUMPS WITHOUT USING GOLD

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6489914 | |
| FREESCALE SEMICONDUCTOR, INC. | 6491451 | WAFER PROCESSING EQUIPMENT AND METHOD FOR PROCESSING WAFERS |
| FREESCALE SEMICONDUCTOR, INC. | 6492202 | METHOD OF ASSEMBLING COMPONENTS ONTO A CIRCUIT BOARD AND ELECTRONIC COMPONENT THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6492232 | VERTICAL SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6492686 | INTEGRATED CIRCUIT HAVING BUFFERING CIRCUITRY WITH SLEW RATE CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 6492874 | ACTIVE BIAS CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6493497 | ELECTRO-OPTIC STRUCTURE AND PROCESS FOR FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6496556 | STEP-DOWN CLOCK CONTROL AND METHOD FOR IMPROVING CONVERGENCE FOR A DIGITALLY CONTROLLED SELF-CALIBRATING VCO |
| FREESCALE SEMICONDUCTOR, INC. | 6496946 | ELECTRONIC CONTROL APPARATUS WITH MEMORY VALIDATION AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6498066 | ULTRA-LATE PROGRAMMING ROM AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6498550 | FILTERING DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6499092 | METHOD AND APPARATUS FOR PERFORMING ACCESS CENSORSHIP IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6500324 | PROCESS FOR DEPOSITING A LAYER OF MATERIAL ON A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 6500723 | METHOD FOR FORMING A WELL UNDER ISOLATION AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6500724 | METHOD OF MAKING SEMICONDUCTOR DEVICE HAVING PASSIVE ELEMENTS INCLUDING FORMING CAPACITOR ELECTRODE AND RESISTOR FROM SAME LAYER OF MATERIA |
| FREESCALE SEMICONDUCTOR, INC. | 6500750 | SEMICONDUCTOR DEVICE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 6501121 | SEMICONDUCTOR STRUCTURE AND PROCESS FOR FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6501973 | APPARATUS AND METHOD FOR MEASURING SELECTED PHYSICAL CONDITION OF AN ANIMATE SUBJECT |
| FREESCALE SEMICONDUCTOR, INC. | 6504246 | INTEGRATED CIRCUIT HVING A BALANCED TWIST FOR DIFFERENTIAL SIGNAL LINES |
| FREESCALE SEMICONDUCTOR, INC. | 6504427 | SWITCHING AMPLIFIER HAVING DIGITAL CORRECTION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6505032 | CARRIERLESS ULTRA WIDEBAND WIRELESS SIGNALS FOR CONVEYING APPLICATION DATA |
| FREESCALE SEMICONDUCTOR, INC. | 6505331 | A METHOD FOR ROUTING OF NETS IN AN ELECTRONIC DEVICE USING GRAPH REPRESENTATION |
| FREESCALE SEMICONDUCTOR, INC. | 6507475 | CAPACITIVE DEVICE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6509247 | SEMICONDUCTOR DEVICE AND ALIGNMENT METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6514789 | COMPONENT AND METHOD FOR MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6516420 | DATA SYNCHRONIZER USING A PARALLEL HANDSHAKE PIPELINE WHEREIN VALIDITY INDICATORS GENERATE AND SEND ACKNOWLEDGEMENT SIGNALS TO A DIFFERENT CLOCK DOMAIN |
| FREESCALE SEMICONDUCTOR, INC. | 6516666 | YAW RATE MOTION SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | 6517698 | SYSTEM AND METHOD FOR PROVIDING ROTATION TO PLATING FLOW |
| FREESCALE SEMICONDUCTOR, INC. | 6517977 | LITHOGRAPHIC TEMPLATE AND METHOD OF FORMATION AND USE |
| FREESCALE SEMICONDUCTOR, INC. | 6518106 | SEMICONDUCTOR DEVICE AND A METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6518634 | STRONTIUM NITRIDE OR STRONTIUM OXYNITRIDE GATE DIELECTRIC |

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| FREESCALE SEMICONDUCTOR, INC. | 6519684 | LOW OVERHEAD METHOD FOR SELECTING AND UPDATING AN ENTRY IN A CACHE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 6521961 | SEMICONDUCTOR DEVICE USING A BARRIER LAYER BETWEEN THE GATE ELECTRODE AND SUBSTRATE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6522195 | LOW NOISE AMPLIFIER BYPASS CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | 6524931 | METHOD FOR FORMING A TRENCH ISOLATION STRUCTURE IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6524967 | METHOD FOR INCORPORATING NITROGEN INTO A DIELECTRIC LAYER USING A SPECIAL PRECURSOR |
| FREESCALE SEMICONDUCTOR, INC. | 6525501 | METHOD AND APPARATUS FOR ACCELERATING COMMUNICATION BETWEEN CONTROLLABLE DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 6528377 | SEMICONDUCTOR SUBSTRATE AND METHOD FOR PREPARING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6528849 | DUAL-GATE RESURF SUPERJUNCTION LATERAL DMOSFET |
| FREESCALE SEMICONDUCTOR, INC. | 6531384 | METHOD OF FORMING A BOND PAD AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6531731 | INTEGRATION OF TWO MEMORY TYPES ON THE SAME INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6532559 | METHOD AND APPARATUS FOR TESTING AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6535157 | LOW POWER CYCLIC A/D CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 6540309 | FAULT-TOLERANT ELECTRONIC BRAKING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6541280 | HIGH DIELECTRIC FILM |
| FREESCALE SEMICONDUCTOR, INC. | 6542940 | METHOD AND APPARATUS FOR CONTROLLING TASK EXECUTION IN A DIRECT MEMORY ACCESS CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | 6544810 | CAPACITIVELY SENSED MICROMACHINED COMPONENT AND METHOD OF MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | 6545324 | DUAL METAL GATE TRANSISTORS FOR CMOS PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 6551869 | LATERAL PNP AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6552436 | SEMICONDUCTOR DEVICE HAVING A BALL GRID ARRAY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6553487 | DEVICE AND METHOD FOR PERFORMING HIGH-SPEED LOW OVERHEAD CONTEXT SWITCH |
| FREESCALE SEMICONDUCTOR, INC. | 6556099 | MULTILAYERED TAPERED TRANSMISSION LINE, DEVICE AND METHOD FOR MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6559723 | SINGLE ENDED INPUT, DIFFERENTIAL OUTPUT AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 6562663 | MICROELECTRONIC ASSEMBLY WITH DIE SUPPORT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6563181 | HIGH FREQUENCY SIGNAL ISOLATION IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6563226 | BONDING PAD |
| FREESCALE SEMICONDUCTOR, INC. | 6564366 | METHOD FOR CHANNEL ROUTING AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 6567424 | APPARATUS AND METHOD FOR DETERMINING A SYNCHRONIZATION SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 6569740 | METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING A BUFFER |
| FREESCALE SEMICONDUCTOR, INC. | 6570947 | A PHASE LOCK LOOP HAVING A ROBUST BANDWIDTH AND A CALIBRATION METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6573160 | METHOD AND APPARATUS FOR FORMING A SEMICONDUCTOR DEVICE UTILIZING A LOW TEMPERATURE PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 6573173 | A METHOD FOR FORMING A COPPER INTERCONNECT USING A MULTI-PLATEN CHEMICAL MECHANICAL POLISHING (CMP) PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 6573562 | SEMICONDUCTOR COMPONENT AND METHOD OF OPERATION |
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| FREESCALE SEMICONDUCTOR, INC. 6576520 AMORPHOUS CARBON LAYER FOR IMPROVED ADHESION OF PHOTORESIST AND METHOD OF FABRICATION FREESCALE SEMICONDUCTOR, INC. 6576522 SEMICONDUCTOR DEVICE AND METHOD THEREFOR FREESCALE SEMICONDUCTOR, INC. 6576632 SEMICONDUCTOR STRUCTURE AND METHOD THEREFOR FREESCALE SEMICONDUCTOR, INC. 6576635 BIPOLAR DIFFERENTIAL AMPLIFIER FREESCALE SEMICONDUCTOR, INC. 6577851 IMPULSE NOISE BLANKER FREESCALE SEMICONDUCTOR, INC. 6567852 INFORMATION AND HETHOD OF FORMATION AND USE. FREESCALE SEMICONDUCTOR, INC. 6560238 THREE INPUT SENSE AMPLIFIER AND METHOD OF FORMATION AND USE. FREESCALE SEMICONDUCTOR, INC. 6560301 METHOD AND APPRAATUS FOR IMPROVING ACCESS TIME IN SET. ASSOCIATIVE ACIDE. SYSTEMS. FREESCALE SEMICONDUCTOR, INC. 6560340 METHOD AND APPRAATUS FOR IMPROVING ACCESS TIME IN SET. ASSOCIATIVE ACIDE. SYSTEMS. FREESCALE SEMICONDUCTOR, INC. 6560430 DIELECTRIC BETWEEN METAL STRUCTURES AND METHOD THEREFOR FREESCALE SEMICONDUCTOR, INC. 6560430 METHOD FOR PATTERNING RESIST FREESCALE SEMICONDUCTOR, INC. 6560430 METHOD AND APPRAATUS FOR CONTROLLING ANTI-PHASE DOMAINS IN SEMICONDUCTOR STRUCTURES AND DEVICES FREESCALE SEMICONDUCTOR, INC. 6561030 METHOD FOR PATTERNING RESIST FREESCALE SEMICONDUCTOR, INC. 6561030 DEBUG CONTROLLER IN A DATA PROCESSOR AND METHOD THEREFOR FREESCALE SEMICONDUCTOR, INC. 6561030 DEBUG CONTROLLER IN A DATA PROCESSOR AND METHOD THEREFOR PREESCALE SEMICONDUCTOR, INC. 6561030 FILTER APPRAATUS AND METHOD THEREFOR ASSOCIATIVE ACIDE OF MATERIAL REMOVAL FROM A SEMICONDUCTOR WAFER FREESCALE SEMICONDUCTOR, INC. 6560452 METHOD FOR ADDING FEATURES TO A DESIGN LAYOUT AND PROCESS FOR DESIGNING A MASK FREESCALE SEMICONDUCTOR, INC. 6560452 METHOD FOR ADDING FEATURES TO A DESIGN LAYOUT AND PROCESS FOR DESIGNING A MASK FREESCALE SEMICONDUCTOR, INC. 6560452 METHOD FOR ADDING FEATURES FOR DEMING A PATTERN ON AN INTEGRATED CIRCUIT VIRE AND METHOD THEREFOR FREESCALE SEMICONDUCTOR, INC. 6600388 SECUENTY SYSTEMA AND METHOD THEREFOR FREESCALE SEMICONDUCTOR, INC. 6600395 CIRCUI | Owner | Patent # | Description |
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| THEREFOR FREESCALE SEMICONDUCTOR, INC. 6614197 ODD HARMONICS REDUCTION OF PHASE ANGLE CONTROLLED LOADS FREESCALE SEMICONDUCTOR, INC. 6614307 HYBRID STRUCTURE FOR DISTRIBUTED POWER AMPLIFIERS | FREESCALE SEMICONDUCTOR, INC. | 6614062 | SEMICONDUCTOR TILING STRUCTURE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. 6614307 HYBRID STRUCTURE FOR DISTRIBUTED POWER AMPLIFIERS | FREESCALE SEMICONDUCTOR, INC. | 6614091 | |
| FREESCALE SEMICONDUCTOR, INC. 6614307 HYBRID STRUCTURE FOR DISTRIBUTED POWER AMPLIFIERS | FREESCALE SEMICONDUCTOR, INC. | 6614197 | ODD HARMONICS REDUCTION OF PHASE ANGLE CONTROLLED LOADS |
| FREESCALE SEMICONDUCTOR, INC. 6617214 INTEGRATED CIRCUIT STRUCTURE AND METHOD THEREFORE | | 6614307 | HYBRID STRUCTURE FOR DISTRIBUTED POWER AMPLIFIERS |
| | FREESCALE SEMICONDUCTOR, INC. | 6617214 | INTEGRATED CIRCUIT STRUCTURE AND METHOD THEREFORE |

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6617524 | PACKAGED INTEGRATED CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6617920 | LINEAR ENVELOPE TRACKING RF POWER AMPLIFIER WITH ADAPTIVE ANALOG SIGNAL PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 6620656 | BODY-TIED SILICON ON INSULATOR SEMICONDUCTOR DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6621348 | VARIABLE GAIN AMPLIFIER WITH AUTOBIASING SUPPLY REGULATION |
| FREESCALE SEMICONDUCTOR, INC. | 6621438 | METHOD AND APPARATUS FOR CONVERTING DIGITAL-TO-ANALOG SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 6621729 | SENSE AMPLIFIER INCORPORATING A SYMMETRIC MIDPOINT REFERENCE |
| FREESCALE SEMICONDUCTOR, INC. | 6625232 | SMART DC OFFSET CORRECTION LOOP |
| FREESCALE SEMICONDUCTOR, INC. | 6625727 | APPARATUS AND METHOD FOR CONFIGURING A DATA PROCESSING SYSTEM BY RETRIEVING A CONFIGURATION VALUE FROM STORAGE DEVICE USING RESET VECTOR AND CONFIGURING PARAMETERS AFTER RESET |
| FREESCALE SEMICONDUCTOR, INC. | 6625777 | METHOD OF IDENTIFYING AN IMPROVED CONFIGURATION FOR A COMMUNICATION SYSTEM USING CODING GAIN AND AN APPARATUS THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6629270 | A SYSTEM FOR INITIALIZING A DISTRIBUTED COMPUTER SYSTEM AND A METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6629367 | METHOD FOR FORMING AN ELECTRICALLY ISOLATED VIA IN A MULTILAYER CERAMIC PACKAGE AND AN ELECTRICAL CONNECTION FORMED WITH THE VIA |
| FREESCALE SEMICONDUCTOR, INC. | 6630725 | ELECTRONIC COMPONENT AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6630746 | SEMICONDUCTOR DEVICE AND METHOD OF MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6633716 | OPTICAL DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6636402 | HIGH VOLTAGE PROTECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6638838 | SEMICONDUCTOR STRUCTURE INCLUDING A PARTIALLY ANNEALED LAYER AND METHOD OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6645678 | METHOD AND APPARATUS FOR MAKING AN INTEGRATED CIRCUIT USING POLARIZATION PROPERTIES OF LIGHT |
| FREESCALE SEMICONDUCTOR, INC. | 6646347 | SEMICONDUCTOR POWER DEVICE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 6646844 | APPARATUS FOR POWER-ON DISABLE IN A MULTIPLE POWER SUPPLY SYSTEM AND A METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6646948 | DATA STORAGE SYSTEM UTILIZING A NON-VOLATILE IC BASED MEMORY FOR REDUCTION OF DATA RETRIEVAL TIME |
| FREESCALE SEMICONDUCTOR, INC. | 6647116 | CURRENT SENSING CIRCUIT AND ADSL INTERFACE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6649445 | WAFER COATING AND SINGULATION METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6649452 | METHOD FOR MANUFACTURING A LITHOGRAPHIC RETICLE FOR TRANSFERRING AN INTEGRATED CIRCUIT DESIGN TO A SEMICONDUCTOR WAFER AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6650022 | SEMICONDUCTOR DEVICE EXHIBITING ENHANCED PATTERN RECOGNITION WHEN ILLUMINATED IN A MACHINE VISION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6650092 | SYSTEM AND METHOD FOR REGULATING A POWER SYSTEM WITH FEEDBACK USING CURRENT SENSING |
| FREESCALE SEMICONDUCTOR, INC. | 6650135 | MEASUREMENT CHUCK HAVING PIEZOELECTRIC ELEMENTS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6653053 | METHOD OF FORMING A PATTERN ON A SEMICONDUCTOR WAFER USING AN ATTENUATED PHASE SHIFTING REFLECTIVE MASK |
| FREESCALE SEMICONDUCTOR, INC. | 6653911 | A BROAD BAND IMPEDANCE MATCHING DEVICE WITH REDUCED LINE WIDTH |
| FREESCALE SEMICONDUCTOR, INC. | 6654871 | A DEVICE AND METHOD FOR PERFORMING STACK OPERATIONS IN A PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6656761 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE FOR DETECTING LIGHT |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6657502 | MULTIPHASE VOLTAGE CONTROLLED OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | 6657977 | RADIO WITH BURST EVENT EXECUTION APPARATUS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6658245 | RADIO RECEIVER HAVING A DYNAMIC BANDWIDTH FILTER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6658440 | MULTICHANNEL FILTERING DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6664200 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND POLYIMIDE ETCHANT THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6664606 | MULTILAYER CIRCUIT APPARATUS WITH REDUCED COUPLING |
| FREESCALE SEMICONDUCTOR, INC. | 6664826 | VARIABLE GAIN LOOP FILTER FOR IMPROVED PHASE MARGIN AND DECREASED PHASE NOISE WITH WIDEBAND BOC'S |
| FREESCALE SEMICONDUCTOR, INC. | 6665338 | CIRCUITRY FOR CONVERTING A SAMPLED DIGITAL SIGNAL TO A NATURALLY SAMPLED DIGITAL SIGNAL AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6665527 | DOUBLE BALANCED MIXER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6667196 | METHOD FOR REAL-TIME MONITORING AND CONTROLLING PEROVSKITE OXIDE FILM GROWTH AND SEMICONDUCTOR STRUCTURE FORMED USING THE METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6667500 | SEMICONDUCTOR DEVICE AND METHOD FOR PROTECTING SUCH DEVICE FROM A REVERSED DRAIN VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | 6667701 | VARIABLE LENGTH DECODER |
| FREESCALE SEMICONDUCTOR, INC. | 6669079 | CONDUCTIVE PASTE AND SEMICONDUCTOR COMPONENT HAVING CONDUCTIVE BUMMPS MADE FROM THE CONDUCTIVE PASTE |
| FREESCALE SEMICONDUCTOR, INC. | 6673646 | GROWTH OF COMPOUND SEMICONDUCTOR STRUCTURES ON PATTERNED OXIDE FILMS AND PROCESS FOR FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6673667 | METHOD FOR MANUFACTURING A SUBSTANTIALLY INTEGRAL MONOLITHIC APPARATUS INCLUDING A PLURALITY OF SEMI CONDUCTOR MATERIALS |
| FREESCALE SEMICONDUCTOR, INC. | 6674304 | OUTPUT BUFFER CIRCUIT AND METH OD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 6674333 | BAND SWITCHABLE VOLTAGE CONTROLLED OSCILLATOR WITH SUBSTANTIALLY CONSTANT TUNING RANGE |
| FREESCALE SEMICONDUCTOR, INC. | 6675235 | METHOD FOR AN EXECUTION UNIT INTERFACE PROTOCOL AND APPARATUS THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6677875 | SIGMA-DELTA ANALOG-TO-DIGITAL CONVERTER AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6677876 | DIFFERENTIAL SIGMA-DELTA DAC WITH DYNAMIC SPECTRAL SHAPING |
| FREESCALE SEMICONDUCTOR, INC. | 6678340 | APPARATUS FOR RECEIVING AND PROCESSING A RADIO FREQUENCY SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 6683370 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6683926 | GAIN CONTROLLER WITH COMPARATOR OFFSET COMPENSATION FOR CIRCUIT HAVING IN-PHASE AND QUADRATURE CHANNELS |
| FREESCALE SEMICONDUCTOR, INC. | 6686245 | VERTICAL MOSFET WITH ASYMMETRIC GATE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6686254 | SEMICONDUCTOR STRUCTURE AND METHOD FOR REDUCING CHARGE DAMAGE |
| FREESCALE SEMICONDUCTOR, INC. | 6686282 | PLATED METAL TRANSISTOR GATE AND METHOF OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 6686633 | SEMICONDUCTOR DEVICE, MEMORY CELL AND PROCESSES FOR FORMING THEM |
| FREESCALE SEMICONDUCTOR, INC. | 6686859 | DIGITAL-TO-ANALOG CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 6687813 | DATA PROCESSING SYSTEM AND METHOD FOR IMPLEMENTING ZERO OVERHEAD LOOPS USING A FIRST OR SECOND PREFIX INSTRUCTION FOR INITIATING CONDITIONAL JUMP OPERATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 6689676 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE STRUCTURE IN A SEMICONDUCTOR LAYER |
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FREESCALE SEMICONDUCTOR, INC.

6689680 SEMICONDUCTOR DEVICE AND METHOD OF FORMATION

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6690748 | RECEIVER WITH IMPROVED DIGITAL INTERMEDIATE TO BASE BAND DEMODULATOR |
| FREESCALE SEMICONDUCTOR, INC. | 6690945 | METHOD FOR SUPPRESSING TRANSIENTS USING A PULSE-SHAPING LOOK-UP TABLE |
| FREESCALE SEMICONDUCTOR, INC. | 6693020 | METHOD OF PREPARING COPPER METALLIZATION DIE FOR WIRE BONDING |
| FREESCALE SEMICONDUCTOR, INC. | 6693033 | METHOD OF REMOVING AN AMORPHOUS OXIDE FROM A MONOCRYSTALLINE SURFACE |
| FREESCALE SEMICONDUCTOR, INC. | 6693339 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6693572 | DIGITAL TUNING SCHEME FOR CONTINUOUS-TIME SIGMA DELTA MODULATION |
| FREESCALE SEMICONDUCTOR, INC. | 6697956 | METHOD AND APPARATUS FOR PHRASE SYNCHRONIZING A PLURALITY OF MICROCONTROLLERS OF A DISTRIBUTED MICROCONTROLLER NETWORK IN A BRAKE-BY-WIRE AUTOMOBILE BRAKING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6700451 | CROSS COUPLED CASCODE VOLTAGE CONTROLLED OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | 6700520 | MULTI-BIT CONTINUOUS TMIE SIGMA-DELTA ADC |
| FREESCALE SEMICONDUCTOR, INC. | 6700814 | SENSE AMPLIFIER BIAS CIRCUIT FOR A MEMORY HAVING AT LEAST TWO DISTINCT RESISTANCE STATES |
| FREESCALE SEMICONDUCTOR, INC. | 6700939 | ULTRA WIDE BANDWIDTH SPREAD-SPECTRUM COMMUNICATIONS SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6701476 | TEST ACCESS MECHANISM FOR SUPPORTING A CONFIGURABLE BUILT-IN SELF-TEST CIRCUIT AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6703895 | SEMICONDUCTOR COMPONENT AND METHOD OF OPERATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6706548 | METHOD OF MAKING A MICROMECHANICAL DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6706599 | MULTI-BIT NON-VOLATILE MEMORY DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6707339 | CONTROLLED BIAS CURRENT BUFFER AND METHOD THEREFOF |
| FREESCALE SEMICONDUCTOR, INC. | 6709793 | METHOD OF MANUFACTURING RETICLES USING SUBRESOLUTION TEST PATTERNS |
| FREESCALE SEMICONDUCTOR, INC. | 6710265 | MULTI-STRAND SUBSTRATE FOR BALL-GRID ARRAY ASSEMBLIES AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6713381 | METHOD OF FORMING SEMICONDUCTOR DEVICE INCLUDING INTERCONNECT BARRIER LAYERS |
| FREESCALE SEMICONDUCTOR, INC. | 6713812 | NON-VOLATILE MEMORY DEVICE HAVING AN ANTI-PUNCH THROUGH (APT) REGION |
| FREESCALE SEMICONDUCTOR, INC. | 6714081 | ACTIVE CURRENT BIAS NETWORK FOR COMPENSATING HOT-CARRIER INJECTION INDUCED BIAS DRIFT |
| FREESCALE SEMICONDUCTOR, INC. | 6714436 | WRITE OPERATION FOR CAPACITORLESS RAM |
| FREESCALE SEMICONDUCTOR, INC. | 6717226 | GATE DIELECTRIC AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6717269 | DIELECTRIC BETWEEN METAL STRUCTURES AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6717270 | INTEGRATED CIRCUIT DIE I/O CELLS |
| FREESCALE SEMICONDUCTOR, INC. | 6717533 | METHOD AND APPARATUS FOR COMBINING A WIRELESS RECEIVER AND A NON-WIRELESS RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 6720635 | ELECTRONIC COMPONENT AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6724032 | MULTI-BIT NON-VOLATILE MEMORY CELL AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6724048 | BODY-TIED SILICON ON INSULATOR SEMICONDUCTOR DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6724079 | WIRE BOND-LESS ELECTRONIC COMPONENT FOR USE WITH AN EXTERNAL CIRCUIT AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6724603 | ELECTROSTATIC DISCHARGE PROTECTION CIRCUITRY AND METHOD OF |

OPERATION

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6730623 | COFIREABLE DIELECTRIC COMPOSITION |
| FREESCALE SEMICONDUCTOR, INC. | 6734524 | ELECTRONIC COMPONENT AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6735238 | ULTRA WIDEBAND COMMUNICATION SYSTEM, METHOD, AND DEVICE WITH LOW NOISE PULSE FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 6737202 | METHOD OF FABRICATING A TIERED STRUCTURE USING A MULTI-LAYERED RESIST STACK AND USE |
| FREESCALE SEMICONDUCTOR, INC. | 6737929 | HYBRID N+ AND P+ GATE-DOPED VOLTAGE VARIABLE CAPACITORS TO IMPROVE LINEAR TUNING RANGE IN VOLTAGE CONTROLLED OSCILLATORS |
| FREESCALE SEMICONDUCTOR, INC. | 6738303 | TECHNIQUE FOR SENSING THE STATE OF A MAGNETO-RESISTIVE RANDOM ACCESS MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 6738420 | DIGITAL FILTER HAVING AN UPSAMPLER OPERATIONAL AT A FRACTIONAL CLOCK RATE |
| FREESCALE SEMICONDUCTOR, INC. | 6740544 | SOLDER COMPOSITIONS FOR ATTACHING A DIE TO A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 6741194 | METHODS AND APPARATUS FOR DETECTING OUT-OF-RANGE SIGNALS IN AN ANALOG-TO-DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 6743668 | PROCESS FOR FORMING A METAL OXY-NITRIDE DIELECTRIC LAYER BY VARYING THE FLOW RATE OF NITROGEN INTO THE CHAMBER |
| FREESCALE SEMICONDUCTOR, INC. | 6744117 | HIGH FREQUENCY SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6744264 | TESTING CIRCUIT AND METHOD FOR MEMS SENSOR PACKAGED WITH AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6744494 | CONTINUOUSLY ADJUSTABLE NEUTRAL DENSITY AREA FILTER |
| FREESCALE SEMICONDUCTOR, INC. | 6747332 | SEMICONDUCTOR COMPONENT HAVING HIGH VOLTAGE MOSFET AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6747434 | METHODS AND DEVICES FOR CONTROLLING STEPPER MOTORS |
| FREESCALE SEMICONDUCTOR, INC. | 6748558 | PERFORMANCE MONITOR SYSTEM AND METHOD SUITABLE FOR USE IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6750524 | TRENCH MOS RESURF SUPER-JUNCTION DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 6750664 | APPARATUS AND METHOD FOR MANAGING AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6750704 | OFFSET COMPENSATED DIFFERENTIAL AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 6750721 | HBT LINEARIZER AND POWER BOOSTER |
| FREESCALE SEMICONDUCTOR, INC. | 6750722 | BIAS CONTROL FOR HBT POWER AMPLIFIERS |
| FREESCALE SEMICONDUCTOR, INC. | 6751125 | GATE VOLTAGE REDUCTION IN A MEMORY READ |
| FREESCALE SEMICONDUCTOR, INC. | 6753216 | MULTIPLE GATE TRANSISTOR EMPLOYING MONOCRYSTALLINE SILICON WALLS |
| FREESCALE SEMICONDUCTOR, INC. | 6753242 | INTEGRATED CIRCUIT DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6753719 | SYSTEM AND CIRCUIT FOR CONTROLLING WELL BIASING AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6754752 | MULTIPLE MEMORY COHERENCE GROUPS IN A SINGLE SYSTEM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6756320 | ARTICLE COMPRISING AN OXIDE LAYER ON A GaAs-BASED SEMICONDUCTOR STRUCTURE AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6757701 | APPARATUS AND METHOD FOR IMPLEMENTING A LINEARLY APPROXIMATED LOG MAP ALGORITHM |
| FREESCALE SEMICONDUCTOR, INC. | 6757852 | SELF RESETTING HIGH SPEED REDUNDANCY CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6759675 | OPTICAL DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6759914 | OSCILLATOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6760268 | METHOD AND APPARATUS FOR ESTABLISHING A REFERENCE VOLTAGE IN A MEMORY |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6760864 | DATA PROCESSING SYSTEM WITH ON-CHIP FIFO FOR STORING DEBUG INFORMATION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6762706 | REDUCED POWER ANALOG-TO-DIGITAL CONVERTER AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6764919 | METHOD FOR FORMING A PASSIVATION LAYER FOR AIR GAP FORMATION AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6765778 | INTEGRATED VERTICAL STACK CAPACITOR |
| FREESCALE SEMICONDUCTOR, INC. | 6765816 | STORAGE CIRCUIT HAVING SINGLE-ENDED WRITE CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | 6766431 | DATA PROCESSING SYSTEM AND METHOD FOR A SECTOR CACHE |
| FREESCALE SEMICONDUCTOR, INC. | 6766433 | SYSTEM HAVING USER PROGRAMMABLE ADDRESSING MODES AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6769076 | REAL-TIME PROCESSOR DEBUG SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6769319 | COMPONENT HAVING A FILTER |
| FREESCALE SEMICONDUCTOR, INC. | 6770506 | RELEASE ETCH METHOD FOR MICROMACHINED SENSORS |
| FREESCALE SEMICONDUCTOR, INC. | 6770569 | LOW TEMPERATURE PLASMA SI OR SIGE FOR MEMS APPLICATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 6770923 | HIGH K DIELECTRIC FILM |
| FREESCALE SEMICONDUCTOR, INC. | 6770929 | METHOD FOR UNIFORM POLISH IN MICROELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6771630 | MULTI-CHANNEL CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | 6774497 | FLIP-CHIP ASSEMBLY WITH THIN UNDERFILL AND THICK SOLDER MASK |
| FREESCALE SEMICONDUCTOR, INC. | 6774732 | SYSTEM AND METHOD FOR COARSE TUNING A PHASE LOCKED LOOP (PLL) SYNTHESIZER USING 2-PI SLIP DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | 6775727 | SYSTEM AND METHOD FOR CONTROLLING BUS ARBITRATION DURING CACHE MEMORY BURST CYCLES |
| FREESCALE SEMICONDUCTOR, INC. | 6775765 | DATA PROCESSING SYSTEM HAVING INSTRUCTION FOLDING AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6778457 | VARIABLE REFRESH CONTROL FOR A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 6779055 | FIRST-IN FIRST-OUT MEMORY SYSTEM AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6780751 | METHOD FOR ELIMINATING VOIDING IN PLATED SOLDER |
| FREESCALE SEMICONDUCTOR, INC. | 6781908 | MEMORY HAVING A VARIABLE REFRESH CONTROL AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6783904 | LITHOGRAPHY CORRECTION METHOD AND DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6784103 | METHOD OF FORMATION OF NANOCRYSTALS ON A SEMICONDUCTOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6784725 | SWITCHED CAPACITOR CURRENT REFERENCE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6785177 | METHOD OF ACCESSING MEMORY AND DEVICE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6785326 | METHOD AND APPARATUS FOR DETECTING AND COMPENSATING DIGITAL LOSSES IN A COMMUNICATIONS NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 6785772 | DATA PREFETCHING APPARATUS IN A DATA PROCESSING SYSTEM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6786222 | METHOD FOR REMOVING PARTICLES FROM A SEMICONDUCTOR PROCESSING TOOL |
| FREESCALE SEMICONDUCTOR, INC. | 6787421 | METHOD FOR FORMING A DUAL GATE OXIDE DEVICE USING A METAL OXIDE AND RESULTING DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6787858 | CARRIER INJECTION PROTECTION STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6788117 | METHOD AND APPARATUS FOR GENERATING FREQUENCY-STABLE WAVELETS |
| FREESCALE SEMICONDUCTOR, INC. | 6788134 | LOW VOLTAGE CURRENT SOURCES/CURRENT MIRRORS |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6790719 | PROCESS FOR FORMING DUAL METAL GATE STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | 6790727 | INTEGRATION OF TWO MEMORY TYPES ON THE SAME INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6790759 | SEMICONDUCTOR DEVICE WITH STRAIN RELIEVING BUMP DESIGN |
| FREESCALE SEMICONDUCTOR, INC. | 6791125 | SEMICONDUCTOR DEVICE STRUCTURES WHICH UTILIZE METAL SULFIDES |
| FREESCALE SEMICONDUCTOR, INC. | 6791883 | PROGRAM AND ERASE IN A THIN FILM STORAGE NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 6792481 | DMA CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | 6792502 | A MICROPROCESSOR HAVING A CONTENT ADDRESSABLE MEMORY (CAM) DEVICE AS A FUNCTIONAL UNIT THEREIN AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 6794101 | MICRO-ELECTRO-MECHANICAL DEVICE AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 6794281 | DUAL METAL GATE TRANSISTORS FOR CMOS PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 6794949 | FREQUENCY GENERATING DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6796482 | PHASE SEPARATED SYSTEM FOR FLUXING |
| FREESCALE SEMICONDUCTOR, INC. | 6797440 | METHOD OF FORMING A RIM PHASE SHIFTING MASK AND USING THE RIM PHASE SHIFTING MASK TO FORM A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6798064 | ELECTRONIC COMPONENT AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6798074 | METHOD OF ATTACHING A DIE TO A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 6798152 | CLOSED LOOP CURRENT CONTROL CIRCUIT AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6798289 | SYSTEM, APPARATUS AND METHOD FOR VOLTAGE TO CURRENT CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | 6800946 | SELECTIVE UNDERFILL FOR OPTO-ELECTRONIC FLIP CHIPS AND FLIP-CHIP ASSEMBLIES |
| FREESCALE SEMICONDUCTOR, INC. | 6803248 | A CHEMISTRY FOR ETCHING QUATERNARY INTERFACE LAYERS ON InGaAsP MOSTLY FORMED BETWEEN GaAs AND InxGa(1-x) P LAYERS |
| FREESCALE SEMICONDUCTOR, INC. | 6803302 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING A MECHANICALLY ROBUST PAD INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | 6803323 | METHOD OF FORMING A COMPONENT OVERLYING A SEMICONDUCTOR SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 6803832 | OSCILLATOR CIRCUIT HAVING REDUCED LAYOUT AREA AND LOWER POWER SUPPLY TRANSIENTS |
| FREESCALE SEMICONDUCTOR, INC. | 6808986 | METHOD OF FORMING NANOCRYSTALS IN A MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6809593 | POWER AMPLIFIER DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6810078 | BLIND RATE DETERMINATION |
| FREESCALE SEMICONDUCTOR, INC. | 6811714 | MICROMACHINED COMPONENT AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6811936 | STRUCTURE AND PROCESS FOR A PELLICLE MEMBRANE FOR 157 NANOMETER LITHOGRAPHY |
| FREESCALE SEMICONDUCTOR, INC. | 6812517 | DIELECTRIC STORAGE MEMORY CELL HAVING HIGH PERMITTIVITY TOP DIELECTRIC AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6812580 | SEMICONDUCTOR PACKAGE HAVING OPTIMIZED WIRE BOND POSITIONING |
| FREESCALE SEMICONDUCTOR, INC. | 6812762 | FAST MONO-CYCLE GENERATING CIRCUIT USING FULL RAIL SWING LOGIC CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 6813666 | SCALEABLE ARBITRATION AND PRIORITIZATION OF MULTIPLE INTERRUPTS |
| FREESCALE SEMICONDUCTOR, INC. | 6813762 | METHOD FOR PROCESSING PROGRAM FILES |

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6815254 | SEMICONDUCTOR PACKAGE WITH MULTIPLE SIDES HAVING PACKAGE CONTACTS |
| FREESCALE SEMICONDUCTOR, INC. | 6815780 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6815820 | MULTIPLE THICKNESS SEMICONDUCTOR INTERCONNECT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6816414 | NONVOLATILE MEMORY AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6817602 | ELECTRONIC DEVICE FOR A LITHOGRAPHY MASK CONTAINER, SEMICONDICTOR MANUFACTURING SYSTEM, AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6818362 | PHOTOLITHOGRAPHY RETICLE DESIGN |
| FREESCALE SEMICONDUCTOR, INC. | 6818493 | SELECTIVE METAL OXIDE REMOVAL |
| FREESCALE SEMICONDUCTOR, INC. | 6819200 | BROADBAND BALUN AND IMPEDANCE TRANSFORMER FOR PUSH-PULL AMPLIFIERS |
| FREESCALE SEMICONDUCTOR, INC. | 6819538 | METHOD AND APPARATUS FOR CONTROLLING CURRENT DEMAND IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6819912 | VARIABLE FREQUENCY SWITCHING AMPLIFIER AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6821082 | WAFER MANAGEMENT SYSTEM AND METHODS FOR MANAGING WAFERS |
| FREESCALE SEMICONDUCTOR, INC. | 6821829 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND SEMICONDUCTOR COMPONENT THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6821878 | AREA-ARRAY DEVICE ASSEMBLY WITH PRE-APPLIED UNDERFILL LAYERS ON PRINTED WIRING BOARD |
| FREESCALE SEMICONDUCTOR, INC. | 6823070 | METHOD FOR KEY ESCROW IN A COMMUNICATION SYSTEM AND APPARATUS THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6823224 | DATA PROCESSING SYSTEM HAVING AN ON-CHIP BACKGROUND DEBUG SYSTEM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6825092 | SEMICONDUCTOR DEVICE HAVING PASSIVE ELEMENTS AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6825641 | HIGH EFFICIENCY ELECTRICAL SWITCH AND DC-DC CONVERTER INCORPORATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6825727 | RADIO FREQUENCY POWER TRANSISTOR AVALANCHE BREAKDOWN DETECTION CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6825736 | METHOD AND APPARATUS FOR CONTROLLING A VOLTAGE CONTROLLED OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | 6826103 | AUTO-TUNEABLE REFERENCE CIRCUIT FOR FLASH EEPROM PRODUCTS |
| FREESCALE SEMICONDUCTOR, INC. | 6826691 | ARRANGEMENT FOR ENCRYPTION/DECRYPTION OF DATA AND DATA CARRI ER INCORPORATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6828618 | SPLIT-GATE THIN-FILM STORAGE NVM CELL |
| FREESCALE SEMICONDUCTOR, INC. | 6828650 | BIPOLAR JUNCTION TRANSISTOR STRUCTURE WITH IMPROVED CURRENT GAIN CHARACTERISTICS |
| FREESCALE SEMICONDUCTOR, INC. | 6831310 | INTEGRATED CIRCUIT HAVING MULTIPLE MEMORY TYPES AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 6831350 | SEMICONDUCTOR STRUCTURE WITH DIFFERENT LATTICE CONSTANT MATERIALS AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6832280 | DATA PROCESSING SYSTEM HAVING AN ADAPTIVE PRIORITY CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | 6833761 | AMPLIFIER APPARATUS AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6834073 | SYSTEM AND METHOD FOR BASEBAND REMOVAL OF NARROWBAND INTERFERENCE IN ULTRA WIDEBAND SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 6834086 | PHASE DETECTOR AND METHOD FOR SECOND HARMONIC CANCELLATION |
| FREESCALE SEMICONDUCTOR, INC. | 6834216 | METHOD AND APPARATUS FOR THE AUTOMATIC SYNCHRONIZATION OF DYNAMIC ANGULAR AND TIME DOMAIN CONTROL SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 6835671 | METHOD OF MAKING AN INTEGRATED CIRCUIT USING AN EUV MASK FORMED BY ATOMIC LAYER DEPOSITION |
| FREESCALE SEMICONDUCTOR, INC. | 6838322 | METHOD FOR FORMING A DOUBLE-GATED SEMICONDUCTOR DEVICE |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6838332 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING ELECTRICAL CONTACT FROM OPPOSITE SIDES |
| FREESCALE SEMICONDUCTOR, INC. | 6838354 | METHOD FOR FORMING A PASSIVATION LAYER FOR AIR GAP FORMATION AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6838721 | INTEGRATED CIRCUIT WITH A TRANSISTOR OVER AN INTERCONNECT LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 6838751 | MULTI-ROW LEADFRAME |
| FREESCALE SEMICONDUCTOR, INC. | 6838776 | CIRCUIT DEVICE WITH AT LEAST PARTIAL PACKAGING AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 6838930 | SWITCHED CAPACITOR AMPLIFIER WITH HIGH THROUGHPUT ARCHITECTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6839011 | SYSTEM AND METHOD OF FILTERING |
| FREESCALE SEMICONDUCTOR, INC. | 6839280 | VARIABLE GATE BIAS FOR A REFERENCE TRANSISTOR IN A NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 6840106 | SENSOR USING AN ACTUATOR FOR SELF-TEST AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6841736 | CURRENT-CARRYING ELECTRONIC COMPONENT AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6841869 | ELECTRONIC ASSEMBLY PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 6842822 | SYSTEM AND METHOD FOR CACHE EXTERNAL WRITING |
| FREESCALE SEMICONDUCTOR, INC. | 6844221 | WIRE BOND-LESS ELECTRONIC COMPONENT FOR USE WITH AN EXTERNAL CIRCUIT AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6844224 | SUBSTRATE CONTACT IN SOI AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6844597 | LOW VOLTAGE NMOS-BASED ELECTROSTATIC DISCHARGE CLAMP |
| FREESCALE SEMICONDUCTOR, INC. | 6844631 | SEMICONDUCTOR DEVICE HAVING A BOND PAD AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6844762 | CAPACITIVE CHARGE PUMP |
| FREESCALE SEMICONDUCTOR, INC. | 6845419 | FLEXIBLE INTERRUPT CONTROLLER THAT INCLUDES AN INTERRUPT FORCE REGISTER |
| FREESCALE SEMICONDUCTOR, INC. | 6845670 | SINGLE PROOF MASS, 3 AXIS MEMS TRANSDUCER |
| FREESCALE SEMICONDUCTOR, INC. | 6846716 | INTEGRATED CIRCUIT DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6846717 | SEMICONDUCTOR DEVICE HAVING A WIRE BOND PAD AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6847102 | SEMICONDUCTOR DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6847548 | MEMORY WITH MULTIPLE STATE CELLS AND SENSING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 6848030 | METHOD AND APPARATUS FOR FILLING LINES IN A CACHE |
| FREESCALE SEMICONDUCTOR, INC. | 6849487 | METHOD FOR FORMING AN ELECTRONIC STRUCTURE USING ETCH |
| FREESCALE SEMICONDUCTOR, INC. | 6849515 | SEMICONDUCTOR PROCESS FOR DISPOSABLE SIDEWALL SPACERS AND STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6850733 | CARRIERLESS ULTRA WIDEBAND WIRELESS SIGNALS FOR CONVEYING DATA |
| FREESCALE SEMICONDUCTOR, INC. | 6852454 | MULTI-TIERED LITHOGRAPHIC TEMPLATE AND METHOD OF FORMATION AND USE |
| FREESCALE SEMICONDUCTOR, INC. | 6852588 | METHODS OF FABRICATING SEMICONDUCTOR STRUCTURES COMPRISING EPITAXIAL HF3SI2 LAYERS |
| FREESCALE SEMICONDUCTOR, INC. | 6853586 | NON-VOLATILE MEMORY ARCHITECTURE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6854637 | WIREBONDING INSULATED WIRE |
| FREESCALE SEMICONDUCTOR, INC. | 6855992 | STRUCTURE AND METHOD FOR FABRICATING CONFIGURABLE TRANSISTOR DEVICES UTILIZING THE FORMATION OF A COMPLIANT SUBSTRATE FOR MATERIALS LISED TO FORM THE SAME |

MATERIALS USED TO FORM THE SAME

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6856173 | MULTIPLEXING OF DIGITAL SIGNALS AT MULTIPLE SUPPLY VOLTAGES IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6856266 | MULTI-RATE ANALOG-TO-DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 6858542 | SEMICONDUCTOR FABRICATION METHOD FOR MAKING SMALL FEATURES |
| FREESCALE SEMICONDUCTOR, INC. | 6858932 | PACKAGED SEMICONDUCTOR DEVICE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 6859506 | ULTRA WIDEBAND COMMUNICATION SYSTEM, METHOD, AND DEVICE WITH LOW NOISE RECEPTION |
| FREESCALE SEMICONDUCTOR, INC. | 6859875 | PROCESSOR HAVING SELECTIVE BRANCH PREDICTION |
| FREESCALE SEMICONDUCTOR, INC. | 6861689 | ONE TRANSISTOR DRAM CELL STRUCTURE AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 6861817 | METHOD AND APPARATUS FOR DETECTING A STALL CONDITION IN A STEPPING MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | 6862240 | VARIABLE REFRESH CONTROL FOR A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 6864135 | SEMICONDUCTOR FABRICATION PROCESS USING TRANSISTOR SPACERS OF DIFFERING WIDTHS |
| FREESCALE SEMICONDUCTOR, INC. | 6864758 | APPARATUS AND RESONANT CIRCUIT EMPLOYING A VARACTOR DIODE IN PARALLEL WITH A TRANSMISSION LINE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6864817 | SIGNALING DEPENDENT ADAPTIVE ANALOG-TO-DIGITAL CONVERTER (ADC) SYSTEM AND METHOD OF USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6867072 | FLIPCHIP QFN PACKAGE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6867078 | METHOD FOR FORMING A MICROWAVE FIELD EFFECT TRANSISTOR WITH HIGH OPERATING VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | 6868129 | DEMODULATOR FOR A RADIO RECEIVER AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 6868431 | CIRCUIT AND METHOD FOR PROCESSING DATA |
| FREESCALE SEMICONDUCTOR, INC. | 6870219 | FIELD EFFECT TRANSISTOR AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6870243 | THIN GAAS WITH COPPER BACK-METAL STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6870444 | ELECTROMECHANICAL RESONATOR AND METHOD OF OPERATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6871246 | PREFETCH CONTROL IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6873218 | FREQUENCY MODULATOR USING A WAVEFORM GENERATOR |
| FREESCALE SEMICONDUCTOR, INC. | 6875546 | METHOD OF PATTERNING PHOTORESIST ON A WAFER USING AN ATTENUATED PHASE SHIFT MASK |
| FREESCALE SEMICONDUCTOR, INC. | 6875635 | METHOD OF ATTACHING A DIE TO A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 6877123 | SCAN CLOCK CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6878633 | FLIP-CHIP STRUCTURE AND METHOD FOR HIGH QUALITY INDUCTORS AND TRANSFORMERS |
| FREESCALE SEMICONDUCTOR, INC. | 6879028 | MULTI-DIE SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 6879476 | ELECTROSTATIC DISCHARGE CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6880134 | METHOD FOR IMPROVING CAPACITOR NOISE AND MISMATCH CONSTRAINTS IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6881681 | FILM DEPOSITION ON A SEMICONDUCTOR WAFER |
| FREESCALE SEMICONDUCTOR, INC. | 6882023 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6882582 | EEPROM CIRCUIT VOLTAGE REFERENCE CIRCUIT AND METHOD FOR PROVIDING A LOW TEMPERATURE-COEFFICIENT VOLTAGE REFERENCE |

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6882745 | METHOD AND APPARATUS FOR TRANSLATING DETECTED WAFER DEFECT COORDINATES TO RETICLE COORDINATES USING CAD DATA |
| FREESCALE SEMICONDUCTOR, INC. | 6884685 | RADICAL OXIDATION AND/OR NITRIDATION DURING METAL OXIDE LAYER DEPOSITION PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 6884727 | SEMICONDUCTOR FABRICATION PROCESS FOR MODIFYING THE PROFILES OF PATTERNED FEATURES |
| FREESCALE SEMICONDUCTOR, INC. | 6885065 | A FERROMAGNETIC SEMICONDUCTOR STRUCTURE AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6885093 | STACKED DIE SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6887138 | CHEMICAL MECHANICAL POLISH (CMP) CONDITIONING-DISK HOLDER |
| FREESCALE SEMICONDUCTOR, INC. | 6887758 | NON-VOLATILE MEMORY DEVICE AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 6888246 | SEMICONDUCTOR POWER DEVICE WITH SHEAR STRESS COMPENSATION |
| FREESCALE SEMICONDUCTOR, INC. | 6889427 | PROCESS AND APPARATUS FOR DISENGAGING SEMICONDUCTOR DIE FROM AN ADHESIVE FILM |
| FREESCALE SEMICONDUCTOR, INC. | 6890816 | COMPOUND SEMICONDUCTOR STRUCTURE INCLUDING AN EPITAXIAL PEROVSKITE LAYER AND METHOD FOR FABRICATING SEMICONDUCTOR STRUCTURES AND DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 6891229 | INVERTED ISOLATION FORMED WITH SPACERS |
| FREESCALE SEMICONDUCTOR, INC. | 6891846 | METHOD AND APPARATUS FOR A TRAFFIC SHAPER |
| FREESCALE SEMICONDUCTOR, INC. | 6892260 | INTERRUPT PROCESSING IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6893947 | ADVANCED RF ENHANCEMENT-MODE FETS WITH IMPROVED GATE PROPERTIES |
| FREESCALE SEMICONDUCTOR, INC. | 6894353 | CAPPED DUAL METAL GATE TRANSISTOR FOR CMOS PROCESS AND METHOD FOR MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6894540 | GLITCH REMOVAL CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6895530 | METHOD AND APPARATUS FOR CONTROLLING A DATA PROCESSING SYSTEM DURING DEBUG |
| FREESCALE SEMICONDUCTOR, INC. | 6895596 | CIRCUIT AND METHOD FOR INTERLEAVING A DATA STREAM |
| FREESCALE SEMICONDUCTOR, INC. | 6897095 | SEMICONDUCTOR PROCESS AND INTEGRATED CIRCUIT HAVING DUAL METAL OXIDE GATE DIELECTRIC WITH SINGLE METAL GATE ELECTRODE |
| FREESCALE SEMICONDUCTOR, INC. | 6897562 | ELECTRONIC COMPONENT AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6898129 | ERASE OF A MEMORY HAVING A NON-CONDUCTIVE STORAGE MEDIUM |
| FREESCALE SEMICONDUCTOR, INC. | 6898682 | AUTOMATIC READ LATENCY CALCULATION WITHOUT SOFTWARE INTERVENTION FOR A SOURCE-SYNCHRONOUS INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | 6900105 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6900970 | ELECTROSTATIC DISCHARGE CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6901112 | ULTRA WIDE BANDWIDTH SPREAD-SPECTRUM COMMUNICATIONS SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6902440 | METHOD OF FORMING A LOW K DIELECTRIC IN A SEMICONDUCTOR MANUFACTURING PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 6902969 | PROCESS FOR FORMING DUAL METAL GATE STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | 6902971 | TRANSISTOR SIDEWALL SPACER STRESS MODULATION |
| FREESCALE SEMICONDUCTOR, INC. | 6903004 | METHOD OF MAKING A SEMICONDUCTOR DEVICE HAVING A LOW K DIELECTRIC |
| FREESCALE SEMICONDUCTOR, INC. | 6903967 | MEMORY WITH CHARGE STORAGE LOCATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 6904446 | FLOATING POINT MULTIPLIER/ACCUMULATOR WITH REDUCED LATENCY AND |

METHOD THEREOF

| <u>Owner</u> | Patent # | Description |
|-------------------------------|----------|---|
| FREESCALE SEMICONDUCTOR, INC. | 6905392 | POLISHING SYSTEM HAVING A CARRIER HEAD WITH SUBSTRATE PRESENCE SENSING |
| FREESCALE SEMICONDUCTOR, INC. | 6905891 | METHOD FOR PROCESSING MULTIPLE SEMICONDUCTOR DEVICES FOR TEST |
| FREESCALE SEMICONDUCTOR, INC. | 6906406 | MULTIPLE DICE PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 6906582 | CIRCUIT VOLTAGE REGULATION |
| FREESCALE SEMICONDUCTOR, INC. | 6906900 | STRUCTURE AND METHOD OF THERMALLY PROTECTING POWER DEVICES FOR AIR-BAG DEPLOYMENT |
| FREESCALE SEMICONDUCTOR, INC. | 6908822 | SEMICONDUCTOR DEVICE HAVING AN INSULATING LAYER AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 6908852 | METHOD OF FORMING AN ARC LAYER FOR A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6909320 | METHOD AND APPARATUS FOR DUAL OUTPUT VOLTAGE REGULATION |
| FREESCALE SEMICONDUCTOR, INC. | 6909393 | SPACE EFFICIENT LOW POWER CYCLIC A/D CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 6909638 | NON-VOLATILE MEMORY HAVING A BIAS ON THE SOURCE ELECTRODE FOR HCI PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | 6909877 | CARRIERLESS ULTRA WIDEBAND WIRELESS SIGNALS FOR CONVEYING DATA |
| FREESCALE SEMICONDUCTOR, INC. | 6911360 | FUSE AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 6912372 | ULTRA WIDEBAND SIGNALS FOR CONVEYING DATA |
| FREESCALE SEMICONDUCTOR, INC. | 6913941 | SOI POLYSILICON TRENCH REFILL PERIMETER OXIDE ANCHOR SCHEME |
| FREESCALE SEMICONDUCTOR, INC. | 6914012 | ARTICLE COMPRISING AN OXIDE LAYER ON A GAAS-BASED SEMICONDUCTOR STRUCTURE AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6914573 | ELECTRICALLY SMALL PLANAR UWB ANTENNA APPARATUS AND RELATED SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6916682 | SEMICONDUCTOR PACKAGE DEVICE FOR USE WITH MULTIPLE INTEGRATED CIRCUITS IN A STACKED CONFIGURATION AND METHOD OF FORMATION AND TESTING |
| FREESCALE SEMICONDUCTOR, INC. | 6916717 | METHOD FOR GROWING A MONOCRYSTALLINE OXIDE LAYER AND FOR FABRICATING A SEMICONDUCTOR DEVICE ON A MONOCRYSTALLINE SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 6916728 | SEMICONDUCTOR STRUCTURE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6917097 | DUAL GAUGE LEADFRAME |
| FREESCALE SEMICONDUCTOR, INC. | 6917555 | INTEGRATED CIRCUIT POWER MANAGEMENT FOR REDUCING LEAKAGE CURRENT IN CIRCUIT ARRAYS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6919244 | METHOD OF MAKING A SEMICONDUCTOR DEVICE, AND SEMICONDUCTOR DEVICE MADE THEREBY |
| FREESCALE SEMICONDUCTOR, INC. | 6919258 | SEMICONDUCTOR DEVICE INCORPORATING A DEFECT CONTROLLED STRAINED CHANNEL STRUCTURE AND METHOD OF MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6919590 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6920316 | HIGH PERFORMANCE INTEGRATED CIRCUIT REGULATOR WITH SUBSTRATE TRANSIENT SUPPRESSION |
| FREESCALE SEMICONDUCTOR, INC. | 6921700 | METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE CHANNELS |
| FREESCALE SEMICONDUCTOR, INC. | 6921961 | SEMICONDUCTOR DEVICE HAVING ELECTRICAL CONTACT FROM OPPOSITE SIDES INCLUDING A VIA WITH AN END FORMED AT A BOTTOM SURFACE OF THE DIFFUSION REGION |
| FREESCALE SEMICONDUCTOR, INC. | 6921975 | CIRCUIT DEVICE WITH AT LEAST PARTIAL PACKAGING, EXPOSED ACTIVE SURFACE AND A VOLTAGE REFERENCE PLANE |
| FREESCALE SEMICONDUCTOR, INC. | 6921979 | SEMICONDUCTOR DEVICE HAVING A BOND PAD AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6922100 | METHOD AND APPARATUS FOR SWITCHING AMPLIFICATION HAVING VARIABLE SAMPLE POINT AND VARIABLE ORDER CORRECTION |
| FREESCALE SEMICONDUCTOR, INC. | 6924172 | METHOD OF FORMING A BOND PAD |
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| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6924184 | SEMICONDUCTOR DEVICE AND METHOD FOR FORMING A SEMICONDUCTOR DEVICE USING POST GATE STACK PLANARIZATION |
| FREESCALE SEMICONDUCTOR, INC. | 6924697 | SEMICONDUCTOR DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6925108 | ULTRAWIDE BANDWIDTH SYSTEM AND METHOD FOR FAST SYNCHRONIZATION |
| FREESCALE SEMICONDUCTOR, INC. | 6927429 | INTEGRATED CIRCUIT WELL BIAS CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | 6927613 | CIRCUIT GENERATING CONSTANT NARROW-PULSE-WIDTH BOPOLARITY CYCE MONOCYCLES USING CMOS CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 6927722 | SERIES CAPACITIVE COMPONENT FOR SWITCHED-CAPACITOR CIRCUITS CONSISTING OF SERIES-CONNECTED CAPACITORS |
| FREESCALE SEMICONDUCTOR, INC. | 6928005 | DOMINO COMPARATOR CAPABLE FOR USE IN A MEMORY ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | 6928409 | SPEECH RECOGNITION USING POLYNOMIAL EXPANSION AND HIDDEN MARKOV MODELS |
| FREESCALE SEMICONDUCTOR, INC. | 6930027 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT |
| FREESCALE SEMICONDUCTOR, INC. | 6930032 | UNDER BUMP METALLURGY STRUCTURAL DESIGN FOR HIGH RELIABILITY BUMPED PACKAGES |
| FREESCALE SEMICONDUCTOR, INC. | 6931078 | ULTRA WIDE BANDWIDTH SPREAD-SPECTRUM COMMUNICATIONS SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6931241 | DUAL DIGITAL LOW IF COMPLEX RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 6933227 | SEMICONDUCTOR DEVICE AND METHOD OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6933523 | SEMICONDUCTOR ALIGNMENT AID |
| FREESCALE SEMICONDUCTOR, INC. | 6933546 | SEMICONDUCTOR COMPONENT AND METHOD FOR MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6933772 | VOLTAGE REGULATOR WITH IMPROVED LOAD REGULATION USING ADAPTIVE BIASING |
| FREESCALE SEMICONDUCTOR, INC. | 6936492 | SINGLE PROOF MASS, 3 AXIS MEMS TRANSDUCER |
| FREESCALE SEMICONDUCTOR, INC. | 6936896 | SEMICONDUCTOR APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 6937047 | INTEGRATED CIRCUIT WITH TEST PAD STRUCTURE AND METHOD OF TESTING |
| FREESCALE SEMICONDUCTOR, INC. | 6937089 | OFFSET, DELAY AND PARASITICALLY IMMUNE RESISTOR-CAPACITOR (RC) TRACKING LOOP AND METHOD OF USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6937646 | LEAKAGE NULLING RECEIVER CORRELATOR STRUCTURE AND METHOD FOR ULTRA WIDE BANDWIDTH COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6939650 | METHOD OF PATTERNING PHOTORESIST ON A WAFER USING A TRANSMISSION MASK WITH A CARBON LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 6939767 | MULTI-BIT NON-VOLATILE INTEGRATED CIRCUIT MEMORY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6939781 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT THAT INCLUDES SELF-ALIGNING A GATE ELECTRODE TO A FIELD PLATE |
| FREESCALE SEMICONDUCTOR, INC. | 6943289 | SLOTTED PLANAR POWER CONDUCTOR |
| FREESCALE SEMICONDUCTOR, INC. | 6943650 | ELECTROMAGNETIC BAND GAP MICROWAVE FILTER |
| FREESCALE SEMICONDUCTOR, INC. | 6949398 | LOW COSE FABRICATION AND ASSEMBLY OF LID FOR SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 6949455 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE STRUCTURE IN A SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 6949816 | SEMICONDUCTOR COMPONENT HAVING FIRST SURFACE AREA FOR ELECTRICALLY COUPLING TO A SEMICONDUCTOR CHIP AND SECOND SURFACE AREA FOR ELECTRICALLY COUPLING TO A SUBSTRATE, AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6950476 | APPARATUS AND METHOD FOR PERFORMING SISO DECODING |
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| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6951783 | CONFINED SPACERS FOR DOUBLE GATE TRANSISTOR SEMICONDUCTOR FABRICATION PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 6951801 | METAL REDUCTION IN WAFER SCRIBE AREA |
| FREESCALE SEMICONDUCTOR, INC. | 6953738 | METHOD AND APPARATUS FOR FORMING AN SOI BODY-CONTACTED TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 6953985 | WAFER LEVEL MEMS PACKAGING |
| FREESCALE SEMICONDUCTOR, INC. | 6954100 | LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | 6954821 | CROSSBAR SWITCH THAT SUPPORTS A MULTI-PORT SLAVE DEVICE AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 6955967 | NON-VOLATILE MEMORY HAVING A REFERENCE TRANSISTOR AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 6956281 | SEMICONDUCTOR DEVICE FOR REDUCING PHOTOVOLTAIC CURRENT |
| FREESCALE SEMICONDUCTOR, INC. | 6957054 | RADIO RECEIVER HAVING A VARIABLE BANDWIDTH IF FILTER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6958265 | SEMICONDUCTOR DEVICE WITH NANOCLUSTERS |
| FREESCALE SEMICONDUCTOR, INC. | 6958548 | SEMICONDUCTOR DEVICE WITH MAGNETICALLY PERMEABLE HEAT SINK |
| FREESCALE SEMICONDUCTOR, INC. | 6959014 | |
| FREESCALE SEMICONDUCTOR, INC. | 6959309 | INTERFACE BETWEEN PROGRAMMING LANGUAGES AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6960509 | METHOD OF FABRICATING THREE DIMENSIONAL GATE STRUCTURE USING OXYGEN DIFFUSION |
| FREESCALE SEMICONDUCTOR, INC. | 6961423 | METHOD AND APPARATUS FOR PERFORMING ADAPTIVE FILTERING |
| FREESCALE SEMICONDUCTOR, INC. | 6961669 | DE-EMBEDDING DEVICES UNDER TEST |
| FREESCALE SEMICONDUCTOR, INC. | 6963090 | ENHANCMENT MODE METAL-OXIDE-SEMICONDUCTOR FIELD EFFECT TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 6963963 | MEMORY MANAGEMENT IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6964902 | METHOD FOR REMOVING NANOCLUSTERS FROM SELECTED REGIONS |
| FREESCALE SEMICONDUCTOR, INC. | 6964911 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING ISOLATION REGIONS |
| FREESCALE SEMICONDUCTOR, INC. | 6965128 | STRUCTURE AND METHOD FOR FABRICATING SEMICONDUCTOR MICRORESONATOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 6965357 | LIGHT EMITTING ELEMENT DRIVING CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6965630 | MODE CONTROLLER FOR SIGNAL ACQUISITION AND TRACKING IN AN ULTRA WIDEBAND COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6965653 | CIRCUIT AND METHOD FOR PROCESSING AN AUTOMATIC FREQUENCY CONTROL SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 6967143 | SEMICONDUCTOR FABRICATION PROCESS WITH ASYMMETRICAL CONDUCTIVE SPACERS |
| FREESCALE SEMICONDUCTOR, INC. | 6967390 | ELECTRONIC COMPONENT AND METHOD OF MANUFACTURNG SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6967611 | OPTIMIZED REFERENCE VOLTAGE GENERATION USING SWITCHED CAPACITOR SCALING FOR DATA CONVERTERS |
| FREESCALE SEMICONDUCTOR, INC. | 6967993 | ULTRAWIDE BANDWIDTH SYSTEM AND METHOD FOR FAST SYNCHRONIZATION USING SUB-CODE SPINS |
| FREESCALE SEMICONDUCTOR, INC. | 6969568 | METHOD FOR ETCHING A QUARTZ LAYER IN A PHOTORESISTLESS SEMICONDUCTOR MASK |
| FREESCALE SEMICONDUCTOR, INC. | 6969656 | METHOD AND CIRCUIT FOR MULTIPLYING SIGNALS WITH A TRANSISTOR HAVING MORE THAN ONE INDEPENDENT GATE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6969883 | NON-VOLATILE MEMORY HAVING A REFERENCE TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 6970336 | ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT AND METHOD OF OPERATION |
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| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 6972224 | METHOD FOR FABRICATING DUAL-METAL GATE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 6972571 | LOAD BOARD WITH EMBEDDED RELAY TRACKER |
| FREESCALE SEMICONDUCTOR, INC. | 6973417 | METHOD AND SYSTEM FOR SIMULATING EXECUTION OF A TARGET PROGRAM IN A SIMULATED TARGET SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 6973471 | METHOD AND APPARATUS FOR IMPLEMENTING SIGNED MULTIPLICATION OF OPERANDS HAVING DIFFERING BIT WIDTHS WITHOUT SIGN EXTENSION OF THE MULTIPLICAND |
| FREESCALE SEMICONDUCTOR, INC. | 6973540 | METHOD AND APPARATUS FOR SELECTING CACHE WAYS AVAILABLE FOR REPLACEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 6974776 | ACTIVATION PLATE FOR ELECTROLESS AND IMMERSION PLATING OF INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 6975665 | LOW POWER, HIGH RESOLUTION TIMING GENERATOR FOR ULTRA-WIDE BANDWIDTH COMMUNICATION SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 6976110 | METHOD AND APPARATUS FOR REDUCING INTERRUPT LATENCY BY DYNAMIC BUFFER SIZING |
| FREESCALE SEMICONDUCTOR, INC. | 6978392 | ENABLE PROPAGATION CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | 6979622 | SEMICONDUCTOR TRANSISTOR HAVING STRUCTURAL ELEMENTS OF DIFFERING MATERIALS AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 6979627 | ISOLATION TRENCH |
| FREESCALE SEMICONDUCTOR, INC. | 6980541 | MEDIA ACCESS CONTROLLER HAVING PSEUDO-STATIC GUARANTEED TIME SLOTS |
| FREESCALE SEMICONDUCTOR, INC. | 6982483 | HIGH IMPEDANCE RADIO FREQUENCY POWER PLASTIC PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 6982689 | LIGHT-EMITTING ELEMENT DRIVE APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 6986971 | REFLECTIVE MASK USEFUL FOR TRANSFERRING A PATTERN USING EXTREME ULTRAVIOLET (EUV) RADIATION AND METHOD OF MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 6986974 | ATTENUATED PHASE SHIFT MASK FOR EXTREME ULTRAVIOLET LITHOGRAPHY AND METHOD THEREFORE |
| FREESCALE SEMICONDUCTOR, INC. | 6987063 | METHOD TO REDUCE IMPURITY ELEMENTS DURING SEMICONDUCTOR FILM DEPOSITION |
| FREESCALE SEMICONDUCTOR, INC. | 6987423 | TWO PORT VOLTAGE CONTROLLED OSCILLATOR FOR USE IN WIRELESS PERSONAL AREA NETWORK SYNTHESIZERS |
| FREESCALE SEMICONDUCTOR, INC. | 6989229 | NON-RESOLVING MASK TILING METHOD FOR FLARE REDUCTION |
| FREESCALE SEMICONDUCTOR, INC. | 6990164 | DUAL STEERED FREQUENCY SYNTHESIZER |
| FREESCALE SEMICONDUCTOR, INC. | 6991984 | METHOD FOR FORMING A MEMORY STRUCTURE USING A MODIFIED SURFACE TOPOGRAPHY AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 6992003 | INTEGRATION OF ULTRA LOW K DIELECTRIC IN A SEMICONDUCTOR FABRICATION PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 6992371 | DEVICE INCLUDING AN AMORPHOUS CARBON LAYER FOR IMPROVED ADHESION OF ORGANIC LAYERS AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 6992377 | SEMICONDUCTOR PACKAGE WITH CROSSING CONDUCTOR ASSEMBLY AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 6993311 | RADIO RECEIVER HAVING AN ADAPTIVE EQUALIZER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6993693 | ANALOGUE/DIGITAL INTERFACE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 6995482 | SWITCHING CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 6995791 | AUTOMATIC WHITE BALANCE FOR DIGITAL IMAGING |
| FREESCALE SEMICONDUCTOR, INC. | 6996651 | ON CHIP NETWORK WITH MEMORY DEVICE ADDRESS DECODING |
| FREESCALE SEMICONDUCTOR, INC. | 6996897 | MOUNTING SURFACES FOR ELECTRONIC DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 6998952 | INDUCTIVE DEVICE INCLUDING BOND WIRES |

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| FREESCALE SEMICONDUCTOR, INC. | 6999014 | INCREMENTAL-DELTA ANALOGUE-TO-DIGITAL CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | 6999627 | DETERMINISTIC PREDICTION IN AN IMAGE PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7000473 | MEM STRUCTURE HAVING REDUCED SPRING STICTION |
| FREESCALE SEMICONDUCTOR, INC. | 7001852 | METHOD OF MAKING A HIGH QUALITY THIN DIELECTRIC LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7002371 | LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | 7002940 | MULTIPLE-STAGE FILTERING DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7003056 | SYMBOL TIMING TRACKING AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7003743 | METHOD AND SYSTEM OF DATA PROCESSOR DESIGN |
| FREESCALE SEMICONDUCTOR, INC. | 7005193 | METHOD OF ADDING MASS TO MEMS STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | 7005717 | SEMICONDUCTOR DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7006318 | REMOVABLE MEDIA STORAGE SYSTEM WITH MEMORY FOR STORING OPERATIONAL DATA |
| FREESCALE SEMICONDUCTOR, INC. | 7006439 | METHOD AND APPARATUS FOR DETERMINING AN UPPER DATA RATE FOR A VARIABLE DATA RATE SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 7006553 | ANALOG SIGNAL SEPARATOR FOR UWB VERSUS NARROWBAND SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 7007154 | METHOD AND APPARATUS FOR INTERFACING A PROCESSOR TO A COPROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 7009424 | SINGLE SUPPLY LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | 7010056 | SYSTEM AND METHOD FOR GENERATING ULTRA WIDEBAND PULSES |
| FREESCALE SEMICONDUCTOR, INC. | 7012324 | LEAD FRAME WITH FLAG SUPPORT STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7013357 | ARBITER HAVING PROGRAMMABLE ARBITRATION POINTS FOR UNDEFINED LENGTH BURST ACCESSES AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7013409 | METHOD AND APPARATUS FOR DEBUGGING A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7013447 | METHOD FOR CONVERTING A PLANAR TRANSISTOR DESIGN TO A VERTICAL DOUBLE GATE TRANSISTOR DESIGN |
| FREESCALE SEMICONDUCTOR, INC. | 7014888 | METHOD AND STRUCTURE FOR FABRICATING SENSORS WITH A SACRIFICIAL GEL DOME |
| FREESCALE SEMICONDUCTOR, INC. | 7015075 | DIE ENCAPSULATION USING A POROUS CARRIER |
| FREESCALE SEMICONDUCTOR, INC. | 7015153 | METHOD FOR FORMING A LAYER USING A PURGING GAS IN A SEMICONDUCTOR PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 7015517 | SEMICONDUCTOR DEVICE INCORPORATING A DEFECT CONTROLLED STRAINED CHANNEL STRUCTURE AND METHOD OF MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7015585 | A PACKAGED INTEGRATED CIRCUIT HAVING WIRE BONDS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7015679 | CIRCUIT AND METHOD FOR SUPPLYING AN ELECTRICAL AC LOAD |
| FREESCALE SEMICONDUCTOR, INC. | 7015852 | CYCLIC ANALOG-TO-DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 7016488 | METHOD AND APPARATUS FOR NON-LINEAR PROCESSING OF AN AUDIO SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 7018747 | PHOTOMASK HAVING LINE END PHASE ANCHORS |
| FREESCALE SEMICONDUCTOR, INC. | 7018876 | TRANSISTOR WITH VERTICAL DIELECTRIC STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7018901 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING A STRAINED CHANNEL AND A HETEROJUNCTION SOURCE/DRAIN |
| FREESCALE SEMICONDUCTOR, INC. | 7018939 | MICELLAR TECHNOLOGY FOR POST-ETCH RESIDUES |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7019332 | FABRICATION OF A WAVELENGTH LOCKER WITHIN A SEMICONDUCTOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7019403 | ADHESIVE FILM AND TACKING PADS FOR PRINTED WIRING ASSEMBLIES |
| FREESCALE SEMICONDUCTOR, INC. | 7020374 | OPTICAL WAVEGUIDE STRUCTURE AND METHOD FOR FABRICATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7023195 | MODULE, SYSTEM AND METHOD FOR TESTING A PHASE LOCKED LOOP |
| FREESCALE SEMICONDUCTOR, INC. | 7023981 | METHOD AND APPARATUS FOR SIGNAL DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | 7026076 | METHOD OF PATTERNING PHOTORESIST ON A WAFER USING A REFLECTIVE MASK WITH A MULTI-LAYER ARC |
| FREESCALE SEMICONDUCTOR, INC. | 7026204 | TRANSISTOR WITH REDUCED GATE-TO-SOURCE CAPACITANCE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7029980 | METHOD OF MANUFACTURING SOI TEMPLATE LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7030001 | METHOD FOR FORMING A GATE ELECTRODE HAVING A METAL |
| FREESCALE SEMICONDUCTOR, INC. | 7030469 | METHOD OF FORMING A SEMICONDUCTOR PACKAGE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7030663 | MONOCYCLE GENERATOR |
| FREESCALE SEMICONDUCTOR, INC. | 7030849 | ROBUST LCD CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | 7031680 | STOP-ON-STATION METHOD AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 7033866 | METHOD FOR MAKING DUAL GAUGE LEADFRAME |
| FREESCALE SEMICONDUCTOR, INC. | 7034558 | TEST SYSTEM FOR DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7037795 | LOW RC PRODUCT TRANSISTORS IN SOI SEMICONDUCTOR PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 7037857 | METHOD FOR ELIMINATING OF EXCESSIVE FIELD OXIDE RECESS FOR THIN SI SOI |
| FREESCALE SEMICONDUCTOR, INC. | 7038547 | AMPLIFIER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7038959 | MRAM SENSE AMPLIFIER HAVING A PRECHARGE CIRCUIT AND METHOD FOR SENSING |
| FREESCALE SEMICONDUCTOR, INC. | 7039392 | SYSTEM AND METHOD FOR PROVIDING DEVICE AUTHENTICATION IN A WIRELESS NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 7039438 | MULTI-MODE RADIO COMMUNICATIONS DEVICE USING A COMMON REFERENCE OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | 7040154 | MOTION SENSING FOR TIRE PRESSURE MONITORING |
| FREESCALE SEMICONDUCTOR, INC. | 7041562 | METHOD FOR FORMING MULTIPLE GATE OXIDE THICKNESS UTILIZING ASHING AND CLEANING |
| FREESCALE SEMICONDUCTOR, INC. | 7041576 | SEPARATELY STRAINED N-CHANNEL AND P-CHANNEL TRANSISTORS |
| FREESCALE SEMICONDUCTOR, INC. | 7042098 | BONDING PAD FOR A PACKAGED INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7042103 | LOW STRESS SEMICONDUCTOR DIE ATTACH |
| FREESCALE SEMICONDUCTOR, INC. | 7042377 | ANALOGUE-TO-DIGITAL SIGMA-DELTA MODULATOR WITH FIR FILTERS |
| FREESCALE SEMICONDUCTOR, INC. | 7042765 | MEMORY BIT LINE SEGMENT ISOLATION |
| FREESCALE SEMICONDUCTOR, INC. | 7042868 | METHOD AND SYSTEM FOR PERFORMING RANGING FUNCTIONS IN AN ULTRAWIDE BANDWIDTH SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7042964 | VITERBI DECODER, METHOD AND UNIT THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7043017 | KEY STREAM CIPHER DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7045432 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE WITH LOCAL SEMICONDUCTOR-ON-INSULATOR (SOI) |

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7045815 | A SEMICONDUCTOR STRUCTURE EXHIBITING REDUCED LEAKAGE CURRENT AND METHOD OF FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7047174 | METHOD FOR PRODUCING TEST PATTERNS FOR TESTING AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7049694 | SEMICONDUCTOR PACKAGE WITH CROSSING CONDUCTOR ASSEMBLY AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7050354 | LOW-POWER COMPILER-PROGRAMMABLE MEMORY WITH FAST ACCESS TIMING |
| FREESCALE SEMICONDUCTOR, INC. | 7051150 | SCALABLE ON CHIP NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 7052939 | STRUCTURE TO REDUCE SIGNAL CROSS-TALK THROUGH SEMICONDUCTOR SUBSTRATE FOR SYSTEM ON CHIP APPLICATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 7056766 | METHOD OF FORMING LAND GRID ARRAY PACKAGED DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7056778 | SEMICONDUCTOR LAYER FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7057427 | POWER ON RESET CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7057462 | TEMPERATURE COMPENSATED ON-CHIP BIAS CIRCUIT FOR LINEAR RF HBT POWER AMPLIFIERS |
| FREESCALE SEMICONDUCTOR, INC. | 7057564 | MULTYLAYER CAVITY SLOT ANTENNA |
| FREESCALE SEMICONDUCTOR, INC. | 7058149 | SYSTEM FOR PROVIDING A CALIBRATED CLOCK AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7058414 | METHOD AND SYSTEM FOR ENABLING DEVICE FUNCTIONS BASED ON DISTANCE INFORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7061299 | BIDIRECTIONAL LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | 7063919 | LITHOGRAPHIC TEMPLATE HAVING A REPAIRED GAP DEFECT METHOD OF REPAIR AND USE |
| FREESCALE SEMICONDUCTOR, INC. | 7064030 | METHOD FOR FORMING A MULTI-BIT NON-VOLATILE MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7064396 | INTEGRATED CIRCUIT WITH MULTIPLE SPACER INSULATING REGION WIDTHS |
| FREESCALE SEMICONDUCTOR, INC. | 7064615 | METHOD AND APPARATUS FOR DOHERTY AMPLIFIER BIASING |
| FREESCALE SEMICONDUCTOR, INC. | 7064700 | MULTI-CHANNEL ANALOG TO DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 7065136 | RECEIVER HAVING AN EQUALIZING DEMODULATOR AND A NON-EQUALIZING DEMODULATOR AND METHOD FOR CONTROLLING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7065207 | CONTROLLING ATTENUATION DURING ECHO SUPPRESSION |
| FREESCALE SEMICONDUCTOR, INC. | 7067856 | SEMICONDUCTOR STRUCTURE, SEMICONDUCTOR DEVICE, COMMUNICATING DEVICE, INTEGRATED CIRCUIT, AND PROCESS FOR FABRICATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7067868 | DOUBLE GATE DEVICE HAVING A HETEROJUNCTION SOURCE/DRAIN AND STRAINED CHANNEL |
| FREESCALE SEMICONDUCTOR, INC. | 7067907 | SEMICONDUCTOR PACKAGE HAVING ANGULATED INTERCONNECT SURFACES |
| FREESCALE SEMICONDUCTOR, INC. | 7068198 | DOUBLE-SAMPLED INTEGRATOR SYSTEM AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7069384 | SYSTEM AND METHOD FOR CACHE EXTERNAL WRITING AND WRITE SHADOWING |
| FREESCALE SEMICONDUCTOR, INC. | 7071038 | METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING A DIELECTRIC LAYER WITH HIGH DIELECTRIC CONSTANT |
| FREESCALE SEMICONDUCTOR, INC. | 7071518 | SCHOTTKY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7072635 | METHOD FOR COMBINING DATA FROM PHASE INDETERMINATE DATA STREAMS FOR RAKING |
| FREESCALE SEMICONDUCTOR, INC. | 7074118 | POLISHING CARRIER HEAD WITH A MODIFIED PRESSURE PROFILE |

7074527 METHOD FOR FABRICATING A MASK USNG A HARDMASK AND METHOD FOR

MAKING A SEMICONDUCTOR DEVICE USING THE SAME

FREESCALE SEMICONDUCTOR, INC.

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7074627 | LEAD SOLDER INDICATOR AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7074647 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7074664 | DUAL METAL GATE ELECTRODE SEMICONDUCTOR FABRICATION PROCESS AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7074681 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | 7074687 | METHOD FOR FORMING AN ESD PROTECTION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7074713 | PLASMA ENHANCED NITRIDE LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7076584 | METHOD AND APPARATUS FOR INTERCONNECTING PORTIONS OF CIRCUITRY WITHIN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7078297 | MEMORY WITH RECESSED DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7078785 | SEMICONDUCTOR DEVICE AND MAKING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7078796 | CORROSION-RESISTANT COPPER BOND PAD AND INTEGRATED DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7078966 | POWER AMPLIFIER SATURATION DETECTION AND OPERATION AT MAXIMUM POWER |
| FREESCALE SEMICONDUCTOR, INC. | 7079068 | ANALOG TO DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 7079604 | ULTRAWIDE BANDWIDTH SYSTEM AND METHOD FOR FAST SYNCHRONIZATION USING MULTIPLE DETECTION ARMS |
| FREESCALE SEMICONDUCTOR, INC. | 7080373 | METHOD AND DEVICE FOR CREATING AND USING PRE-INTERNALIZED PROGRAM FILES |
| FREESCALE SEMICONDUCTOR, INC. | 7082451 | RECONFIGURABLE VECTOR-FFT/IFFT, VECTOR-MULTIPLIER/DIVIDER |
| FREESCALE SEMICONDUCTOR, INC. | 7083880 | LITHOGRAPHIC TEMPLATE AND METHOD OF FORMATION AND USE |
| FREESCALE SEMICONDUCTOR, INC. | 7084485 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT, AND SEMICONDUCTOR COMPONENT FORMED THEREBY |
| FREESCALE SEMICONDUCTOR, INC. | 7084698 | BAND-GAP REFERENCE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7085175 | WORD LINE DRIVER CIRCUIT FOR A STATIC RANDOM ACCESS MEMORY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7088009 | WIREBONDED ASSEMBLAGE METHOD AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 7088162 | CIRCUIT GENERATING CONSTANT NARROW-PULSE-WIDTH BIPOLARITY MONOCYCLES |
| FREESCALE SEMICONDUCTOR, INC. | 7088632 | AUTOMATIC HIDDEN REFRESH IN A DRAM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7088702 | METHOD FOR CONTROLLING A DATA STREAM IN A WIRELESS NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 7089170 | SYSTEM AND METHOD FOR TESTING AN EMBEDDED MICROPROCESSOR SYSTEM CONTAINING PHYSICAL AND/OR SIMULATED HARDWARE |
| FREESCALE SEMICONDUCTOR, INC. | 7089467 | ASYNCHRONOUS DEBUG INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | 7091071 | SEMICONDUCTOR FABRICATION PROCESS INCLUDING RECESSED SOURCE/DRAIN REGIONS IN AN SOI WAFER |
| FREESCALE SEMICONDUCTOR, INC. | 7091089 | METHOD OF FORMING A NANOCLUSTER CHARGE STORAGE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7091130 | METHOD OF FORMING A NANOCLUSTER CHARGE STORAGE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7091568 | DIELECTRIC LAYER, AN ELECTRONIC DEVICE INCLUDING THE DIELECTRIC LAYER, AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7091602 | MINIATURE MOLDLOCKS FOR HEATSINK OR FLAG FOR AN OVERMOLDED |

PLASTIC PACKAGE

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7091712 | CIRCUIT FOR PERFORMING VOLTAGE REGULATION |
| FREESCALE SEMICONDUCTOR, INC. | 7092465 | METHOD AND APPARATUS FOR PROCESSING AN AMPLITUDE MODULATED (AM) SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 7092890 | METHOD FOR MANUFACTURING THIN GAAS DIE WITH COPPER-BACK METAL STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | 7094645 | PROGRAMMING AND ERASING STRUCTURE FOR A FLOATING GATE MEMORY CELL AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 7095092 | SEMICONDUCTOR DEVICE AND METHOD OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7095246 | VARIABLE IMPEDANCE OUTPUT BUFFER |
| FREESCALE SEMICONDUCTOR, INC. | 7096307 | SHARED WRITE BUFFER IN A PERIPHERAL INTERFACE AND METHOD OF OPERATING |
| FREESCALE SEMICONDUCTOR, INC. | 7096348 | METHOD AND APPARATUS FOR ALLOCATING ENTRIES IN A BRANCH TARGET BUFFER |
| FREESCALE SEMICONDUCTOR, INC. | 7096378 | DATA STORAGE SYSTEM HAVING A NON-VOLATILE IC BASED MEMORY FOR STORING USER DATA |
| FREESCALE SEMICONDUCTOR, INC. | 7098073 | METHOD FOR STACKING AN INTEGRATED CIRCUIT ON ANOTHER INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7098502 | TRANSISTOR HAVING THREE ELECTRICALLY ISOLATED ELECTRODES AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7098877 | DRIVER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7099973 | METHOD AND SYSTEM OF BUS MASTER ARBITRATION |
| FREESCALE SEMICONDUCTOR, INC. | 7100020 | DIGITAL COMMUNICATIONS PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 7100152 | SOFTWARE ANALYSIS SYSTEM HAVING AN APPARATUS FOR SELECTIVELY COLLECTING ANALYSIS DATA FROM A TARGET SYSTEM EXECUTING SOFTWARE INSTRUMENTED WITH TAG STATEMENTS AND METHOD FOR USE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7101736 | METHOD OF ASSEMBLING A SEMICONDUCTOR COMPONENT AND APPARATUS THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7102359 | INTEGRATED FAULT DETECTOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7102365 | APPARATUS FOR CURRENT SENSING |
| FREESCALE SEMICONDUCTOR, INC. | 7102410 | HIGH VOLTAGE LEVEL CONVERTER USING LOW VOLTAGE DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7102669 | DIGITAL COLOR IMAGE PRE-PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 7105383 | PACKAGED SEMICONDUCTOR WITH COATED LEADS AND METHOD THEREFORE |
| FREESCALE SEMICONDUCTOR, INC. | 7105395 | PROGRAMMING AND ERASING STRUCTURE FOR AN NVM CELL |
| FREESCALE SEMICONDUCTOR, INC. | 7105429 | METHOD OF INHIBITING METAL SILICIDE ENCROACHMENT IN A TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 7105430 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING A NOTCHED CONTROL ELECTRODE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7105866 | HETEROJUNCTION TUNNELING DIODES AND PROCESS FOR FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7105886 | HIGH K DIELECTRIC FILM |
| FREESCALE SEMICONDUCTOR, INC. | 7107436 | CONDITIONAL NEXT PORTION TRANSFERRING OF DATA STREAM TO OR FROM REGISTER BASED ON SUBSEQUENT INSTRUCTION ASPECT |
| FREESCALE SEMICONDUCTOR, INC. | 7108755 | SIMPLIFICATION OF BALL ATTACH METHOD USING SUPER-SATURATED FINE CRYSTAL FLUX |
| FREESCALE SEMICONDUCTOR, INC. | 7109051 | METHOD OF INTEGRATING OPTICAL DEVICES AND ELECTRONIC DEVICES ON AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7109055 | METHODS AND APPARATUS HAVING WAFER LEVEL CHIP SCALE PACKAGE FOR SENSING ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | 7109079 | METAL GATE TRANSISTOR CMOS PROCESS AND METHOD FOR MAKING |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7109550 | SEMICONDUCTOR FABRICATION PROCESS WITH ASYMMETRICAL CONDUCTIVE SPACERS |
| FREESCALE SEMICONDUCTOR, INC. | 7109782 | WELL BIAS VOLTAGE GENERATOR |
| FREESCALE SEMICONDUCTOR, INC. | 7109906 | NICAM ENCODER FEATURING SYNCHRONIZATION OF A NICAM PROCESSOR WITH FRONT-END INPUT AND OUTPUT SECTIONS |
| FREESCALE SEMICONDUCTOR, INC. | 7110380 | SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR SHARING BANDWIDTH IN A WIRELESS PERSONAL AREA NETWORK OR A WIRELESS LOCAL AREA NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 7110473 | MODE CONTROLLER FOR SIGNAL ACQUISITION AND TRACKING IN AN ULTRA WIDEBAND COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7111184 | SYSTEM AND METHOD FOR DETERMINISTIC COMMUNICATION ACROSS CLOCK DOMAINS |
| FREESCALE SEMICONDUCTOR, INC. | 7112455 | SEMICONDUCTOR OPTICAL DEVICES AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 7112490 | HOT CARRIER INJECTION PROGRAMMABLE STRUCTURE INCLUDING DISCONTINUOUS STORAGE ELEMENTS AND SPACER CONTROL GATES IN A TRENCH |
| FREESCALE SEMICONDUCTOR, INC. | 7112832 | TRANSISTOR HAVING MULTIPLE CHANNELS |
| FREESCALE SEMICONDUCTOR, INC. | 7112871 | FLIPCHIP QFN PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7113054 | ARRANGEMENT AND METHOD IMPEDANCE MATCHING |
| FREESCALE SEMICONDUCTOR, INC. | 7113430 | DEVICE FOR REDUCING THE EFFECTS OF LEAKAGE CURRENT WITHIN ELECTRONIC DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7115949 | METHOD OF FORMING A SEMICONDUCTOR DEVICE IN A SEMICONDUCTOR LAYER AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7116147 | CIRCUIT AND METHOD FOR INTERPOLATIVE DELAY |
| FREESCALE SEMICONDUCTOR, INC. | 7116537 | SURGE CURRENT PREVENTION CIRCUIT AND DC POWER SUPPLY |
| FREESCALE SEMICONDUCTOR, INC. | 7117346 | DATA PROCESSING SYSTEM HAVING MULTIPLE REGISTER CONTEXTS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7119381 | COMPLEMENTARY METAL-OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7120126 | METHOD FOR IMPROVED MEDIA QUALITY FEEDBACK |
| FREESCALE SEMICONDUCTOR, INC. | 7120661 | BIT EXACTNESS SUPPORT IN DUAL-MAC ARCHITECTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7121141 | Z-AXIS ACCELEROMETER WITH AT LEAST TWO GAP SIZES AND TRAVEL STOPS DISPOSED OUTSIDE AN ACTIVE CAPACITOR AREA |
| FREESCALE SEMICONDUCTOR, INC. | 7122395 | METHOD OF FORMING SEMICONDUCTOR DEVICES THROUGH EPITAXY |
| FREESCALE SEMICONDUCTOR, INC. | 7122421 | SEMICONDUCTOR DEVICE INCLUDING A TRANSISTOR AND A CAPACITOR HAVING AN ALIGNED TRANSISTOR AND CAPATIVE ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 7123068 | FLIP-FLOP CIRCUIT HAVING LOW POWER DATA RETENTION |
| FREESCALE SEMICONDUCTOR, INC. | 7123647 | CHIP RATE BASE BAND RECEIVER PROCESSOR WHICH RECEIVES DIGITAL INFORMATION CONTAINING SYMBOL INFORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7123677 | VARIABLE SAMPLING DATA OUTPUT CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7123892 | ARCHITECTURE FOR AN AM/FM DIGITAL INTERMEDIATE FREQUENCY RADIO |
| FREESCALE SEMICONDUCTOR, INC. | 7124162 | ADDER TREE STRUCTURE DSP SYSTEM AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7124385 | METHOD FOR AUTOMATED TRANSISTOR FOLDING |
| FREESCALE SEMICONDUCTOR, INC. | 7125805 | METHOD OF SEMICONDUCTOR FABRICATION INCORPORATING DISPOSABLE SPACER INTO ELEVATED SOURCE/DRAIN PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 7126172 | INTEGRATION OF MULTIPLE GATE DIELECTRICS BY SURFACE PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 7126192 | TRANSISTOR WITH REDUCED GATE-TO-SOURCE CAPACITANCE AND METHOD |

THEREFOR

| FREESCALE SEMICONDUCTOR, INC. FREESC | <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. 7127384 FAST SIMULATION OF CIRCUITRY HAVING SOLTRANSISTORS FREESCALE SEMICONDUCTOR, INC. 7129365 SCRIBE STREET STRUCTURE FOR BACKEND INTERCONNECT FREESCALE SEMICONDUCTOR, INC. 7130346 METHOD AND APPARATUS HAVING A DIGITAL PWM SIGNAL GENERATOR WITH INTEGRAL NOISE SHAPING FREESCALE SEMICONDUCTOR, INC. 7132327 DECOUPLED COMPLEMENTARY MASK PATTERNING TRANSFER METHOD FREESCALE SEMICONDUCTOR, INC. 7132329 SCOURCE SIDE INJECTION STORAGE DEVICE ASSEMBLY AND METHOD FOR FORMING FREESCALE SEMICONDUCTOR, INC. 7132329 SOURCE SIDE INJECTION STORAGE DEVICE WITH SPACER GATES AND METHOD THEREFOR FREESCALE SEMICONDUCTOR, INC. 7132320 METHOD FOR TREATING A SEMICONDUCTOR SUBFACE TO FORM A METAL- CONTAINING LANGE FREESCALE SEMICONDUCTOR, INC. 713240 TRANSISTOR SIDEWALL SPACER STRESS MODULATION FREESCALE SEMICONDUCTOR, INC. 713240 TRANSISTOR SIDEWALL SPACER STRESS MODULATION FREESCALE SEMICONDUCTOR, INC. 7132570 DIELECTRIC STORAGE MEMORY CELL HAVING HIGH PERMITTIVITY TOP DIELECTRIC AND METHOD THEREFOR FREESCALE SEMICONDUCTOR, INC. 7133470 SIGNAL ALL SPRING A SEMICONDUCTOR INC. 7133570 DIELECTRIC AND METHOD THEREFOR FREESCALE SEMICONDUCTOR, INC. 7133570 SIGNAL THROUGH FROM THE MEMORY CELL HAVING HIGH PERMITTIVITY TOP DIELECTRIC AND METHOD THEREFOR FREESCALE SEMICONDUCTOR, INC. 7136029 FREQUENCY SELECTIVE HIGH IMPEDANCE SURFACE FREESCALE SEMICONDUCTOR, INC. 7138029 FREQUENCY SELECTIVE HIGH IMPEDANCE SURFACE FREESCALE SEMICONDUCTOR, INC. 7138020 FREQUENCY SELECTIVE HIGH IMPEDANCE SURFACE FREESCALE SEMICONDUCTOR, INC. 7138020 FREQUENCY SELECTIVE HIGH IMPEDANCE SURFACE FREESCALE SEMICONDUCTOR, INC. 7138020 FREQUENCY SELECTIVE HIGH IMPEDANCE SURFACE FREESCALE SEMICONDUCTOR, INC. 7138020 FREQUENCY SELECTIVE HIGH IMPEDANCE SURFACE FREESCALE SEMICONDUCTOR, INC. 7138020 FREQUENCY SELECTIVE HIGH IMPEDANCE SURFACE FREESCALE SEMICONDUCTOR, INC. 7138020 FREQUENCY SELECTIVE HIGH IMPEDANCE SURFACE FREESCALE SEMICONDUCTOR, INC. 7144050 FREDERIC SEMICONDUCTOR, INC. 714405 FREEDOM SEMICONDUCTOR, INC | FREESCALE SEMICONDUCTOR, INC. | 7126433 | SELF-CALIBRATING OSCILLATOR SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. 7130346 METHOD AND APPARATUS HAVING A DIGITAL PWM SIGNAL GENERATOR WITH INTEGRAL NOISE SHAPING FREESCALE SEMICONDUCTOR, INC. 7130343 STACKED SEMICONDUCTOR DEVICE ASSEMBLY AND METHOD FOR FORMING FREESCALE SEMICONDUCTOR, INC. 7132337 DECOUPLED COMPLEMENTARY MASK PATTERNING TRANSFER METHOD FREESCALE SEMICONDUCTOR, INC. 7132337 DECOUPLED COMPLEMENTARY MASK PATTERNING TRANSFER METHOD FREESCALE SEMICONDUCTOR, INC. 7132337 DECOUPLED COMPLEMENTARY MASK PATTERNING TRANSFER METHOD FREESCALE SEMICONDUCTOR, INC. 7132337 DECOUPLED COMPLEMENTARY MASK PATTERNING TRANSFER METHOD FREESCALE SEMICONDUCTOR, INC. 7132337 DECOUPLED COMPLEMENTARY MASK PATTERNING TRANSFER METHOD PRESCALE SEMICONDUCTOR, INC. 7132337 METHOD FOR TREATING A SEMICONDUCTOR SURFACE TO FORM A METAL CONTAINING LAYER FREESCALE SEMICONDUCTOR, INC. 713247 METHOD FOR TREATING A SEMICONDUCTOR SURFACE TO FORM A METAL CONTAINING LAYER FREESCALE SEMICONDUCTOR, INC. 713263 DISTRICT CONTROL DEVICE FABRICATION FREESCALE SEMICONDUCTOR, INC. 7132630 DISTRICT CLOCK FREQUENCY DOUBLER FREESCALE SEMICONDUCTOR, INC. 7132630 DISTRICT CLOCK FREQUENCY DOUBLER FREESCALE SEMICONDUCTOR, INC. 7132630 DISTRICT CONTROL FREESCALE SEMICONDUCTOR, INC. 7132630 PREJUDITION THE PREMITTER METAL FOR THRESHOLD VOLTAGE CONTROL FREESCALE SEMICONDUCTOR, INC. 7136022 APPLICATION FOR THE METAL FOR THRESHOLD VOLTAGE CONTROL FREESCALE SEMICONDUCTOR, INC. 7136028 PREJUDITION FOR THE METAL FOR THRESHOLD VOLTAGE CONTROL FREESCALE SEMICONDUCTOR, INC. 7136029 FREQUENCY SELECTIVE HIGH IMPEDANCE SURFACE FREESCALE SEMICONDUCTOR, INC. 7136020 PREDICT OF METAL CLOCK FROM THE MID MAD FROM THE PROPER SIGNAL NOISE ISOLATION AND METHOD FOR METAL THRESHOLD WIRE FREESCALE SEMICONDUCTOR, INC. 7136020 PREDICT OF THE METAL THRESHOLD WIRE FREESCALE SEMICONDUCTOR, INC. 7136020 PREDICT OF THE PREDICT OF THE MID FOR DIVINAMIC PREFETCH BUFFER CONFIGURATION AND REPLACEMENT FREESCALE SEMICONDUCTOR, INC. 7138020 PREDICT OF THE METAL THRESHOLD OF THE PREDICT OF THE P | FREESCALE SEMICONDUCTOR, INC. | 7127254 | METHOD OF USING SUB-RATE SLOTS IN AN ULTRAWIDE BANDWIDTH SYSTEM |
| SEMICONDUCTOR WAFER INTEGRATION FREESCALE SEMICONDUCTOR, INC. 713048 METHOD AND APPBARTUS HAVING A DIGITAL PWM SIGNAL GENERATOR WITH INTEGRAL NOISE SHAPING FREESCALE SEMICONDUCTOR, INC. 7132031 DATA PROCESSING SYSTEM WITH BUS ACCESS RETRACTION FREESCALE SEMICONDUCTOR, INC. 7132032 DECOUPLED COMPLEMENTARY MASK PAITERNING TRANSFER METHOD FREESCALE SEMICONDUCTOR, INC. 7132032 DECOUPLED COMPLEMENTARY MASK PAITERNING TRANSFER METHOD FREESCALE SEMICONDUCTOR, INC. 7132032 DECOUPLED COMPLEMENTARY MASK PAITERNING TRANSFER METHOD FREESCALE SEMICONDUCTOR, INC. 713203 DETHOD FOR TREATING A SEMICONDUCTOR SURFACE TO FORM A METAL- CONTAINING LAYER FREESCALE SEMICONDUCTOR, INC. 713207 METHOD FOR PREPARING A SEMICONDUCTOR SUBSTRATE SURFACE FOR FREESCALE SEMICONDUCTOR, INC. 713207 DELECTRIC STORAGE MEMORY CELL HAVING HIGH PERMITTIVITY TOP DELECTRIC STORAGE MEMORY CELL HAVING HIGH PERMITTIVITY TOP DELECTRIC STORAGE MEMORY CELL HAVING HIGH PERMITTIVITY TOP FREESCALE SEMICONDUCTOR, INC. 713602 PRECEDENCY DOUGH IN PREPARING A SEMICONDUCTOR SURFACE FREESCALE SEMICONDUCTOR, INC. 713602 PRECEDENCY DOUGH IN PREPARING DEVICE ABRICATION FREESCALE SEMICONDUCTOR, INC. 713603 DELECTRIC STORAGE MEMORY CELL HAVING HIGH PERMITTIVITY TOP DELECTRIC STORAGE MEMORY CELL HAVING HIMPEOANCE SURFACE FREESCALE SEMICONDUCTOR, INC. 713604 PROCESCALE SEMICONDUCTOR, INC. 713605 PREPARED AND A PREPARATUS FOR DAVINAL PROPERTY OF THE PR | FREESCALE SEMICONDUCTOR, INC. | 7127384 | FAST SIMULATION OF CIRCUITRY HAVING SOI TRANSISTORS |
| WITH INTEGRAIL, NOISE SHAPING FREESCALE SEMICONDUCTOR, INC. FREESC | FREESCALE SEMICONDUCTOR, INC. | 7129566 | |
| FREESCALE SEMICONDUCTOR, INC. FREESC | FREESCALE SEMICONDUCTOR, INC. | 7130346 | |
| FREESCALE SEMICONDUCTOR, INC. 7132329 SOURCE SIDE INJECTION STORAGE DEVICE WITH SPACER GATES AND METHOD THEREFOR FREESCALE SEMICONDUCTOR, INC. 7132360 METHOD FOR TREATING A SEMICONDUCTOR SURFACE TO FORM A METAL-CONTAINING LAYER FREESCALE SEMICONDUCTOR, INC. 713273 METHOD FOR PREPARING A SEMICONDUCTOR SURFACE TO FORM A METAL-CONTAINING LAYER FREESCALE SEMICONDUCTOR, INC. 713274 TRANSISTOR SIDEWALL SPACER STRESS MODULATION FREESCALE SEMICONDUCTOR, INC. 713276 DIGITAL CLOCK FREQUENCY DOUBLER FREESCALE SEMICONDUCTOR, INC. 713276 DIGITAL CLOCK FREQUENCY DOUBLER FREESCALE SEMICONDUCTOR, INC. 713279 DIELECTRIC STORAGE MEMORY CELL HAVING HIGH PERMITTIVITY TOP DIELECTRIC STORAGE MEMORY CELL HAVING HIGH PERMITTIVITY OF | FREESCALE SEMICONDUCTOR, INC. | 7130943 | DATA PROCESSING SYSTEM WITH BUS ACCESS RETRACTION |
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| FREESCALE SEMICONDUCTOR, INC. 7141476 METHOD OF FORMING A TRANSISTOR WITH A BOTTOM GATE FREESCALE SEMICONDUCTOR, INC. 7141857 SEMICONDUCTOR STRUCTURES AND METHODS OF FABRICATING SEMICONDUCTOR STRUCTURES COMPRISING HAFNIUM OXIDE MODIFIED WITH LANTHANUM, A LANTHANIDE-SERIES METAL, OR A COMBINATION THEREOF FREESCALE SEMICONDUCTOR, INC. 7141860 LDMOS TRANSISTOR FREESCALE SEMICONDUCTOR, INC. 7141989 METHODS AND APPARATUS FOR A MEMS VARACTOR FREESCALE SEMICONDUCTOR, INC. 7142058 ON-CHIP TEMPERATURE COMPENSATION CIRCUIT FOR AN ELECTRONIC DEVICE FREESCALE SEMICONDUCTOR, INC. 7142401 DETECTING OVERCURRENTS IN A SWITCHING REGULATOR USING A VOLTAGE DEPENDENT REFERENCE FREESCALE SEMICONDUCTOR, INC. 7142597 FULL BRIDGE INTEGRAL NOISE SHAPING FOR QUANTIZATION OF PULSE WIDTH MODULATION SIGNALS FREESCALE SEMICONDUCTOR, INC. 7142606 METHOD AND APPARATUS FOR SHARED PROCESSING A PLURALITY OF | FREESCALE SEMICONDUCTOR, INC. | 7139860 | SCALABLE ON CHIP NETWORK |
| FREESCALE SEMICONDUCTOR, INC. 7141857 SEMICONDUCTOR STRUCTURES AND METHODS OF FABRICATING SEMICONDUCTOR STRUCTURES COMPRISING HAFNIUM OXIDE MODIFIED WITH LANTHANUM, A LANTHANIDE-SERIES METAL, OR A COMBINATION THEREOF FREESCALE SEMICONDUCTOR, INC. 7141860 LDMOS TRANSISTOR FREESCALE SEMICONDUCTOR, INC. 7141989 METHODS AND APPARATUS FOR A MEMS VARACTOR FREESCALE SEMICONDUCTOR, INC. 7142058 ON-CHIP TEMPERATURE COMPENSATION CIRCUIT FOR AN ELECTRONIC DEVICE FREESCALE SEMICONDUCTOR, INC. 7142401 DETECTING OVERCURRENTS IN A SWITCHING REGULATOR USING A VOLTAGE DEPENDENT REFERENCE FREESCALE SEMICONDUCTOR, INC. 7142597 FULL BRIDGE INTEGRAL NOISE SHAPING FOR QUANTIZATION OF PULSE WIDTH MODULATION SIGNALS FREESCALE SEMICONDUCTOR, INC. 7142606 METHOD AND APPARATUS FOR SHARED PROCESSING A PLURALITY OF | FREESCALE SEMICONDUCTOR, INC. | 7139878 | |
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| FREESCALE SEMICONDUCTOR, INC. 7141989 METHODS AND APPARATUS FOR A MEMS VARACTOR FREESCALE SEMICONDUCTOR, INC. 7142058 ON-CHIP TEMPERATURE COMPENSATION CIRCUIT FOR AN ELECTRONIC DEVICE FREESCALE SEMICONDUCTOR, INC. 7142401 DETECTING OVERCURRENTS IN A SWITCHING REGULATOR USING A VOLTAGE DEPENDENT REFERENCE FREESCALE SEMICONDUCTOR, INC. 7142597 FULL BRIDGE INTEGRAL NOISE SHAPING FOR QUANTIZATION OF PULSE WIDTH MODULATION SIGNALS FREESCALE SEMICONDUCTOR, INC. 7142606 METHOD AND APPARATUS FOR SHARED PROCESSING A PLURALITY OF | FREESCALE SEMICONDUCTOR, INC. | 7141857 | SEMICONDUCTOR STRUCTURES COMPRISING HAFNIUM OXIDE MODIFIED WITH LANTHANUM, A LANTHANIDE-SERIES METAL, OR A COMBINATION |
| FREESCALE SEMICONDUCTOR, INC. 7142058 ON-CHIP TEMPERATURE COMPENSATION CIRCUIT FOR AN ELECTRONIC DEVICE FREESCALE SEMICONDUCTOR, INC. 7142401 DETECTING OVERCURRENTS IN A SWITCHING REGULATOR USING A VOLTAGE DEPENDENT REFERENCE FREESCALE SEMICONDUCTOR, INC. 7142597 FULL BRIDGE INTEGRAL NOISE SHAPING FOR QUANTIZATION OF PULSE WIDTH MODULATION SIGNALS FREESCALE SEMICONDUCTOR, INC. 7142606 METHOD AND APPARATUS FOR SHARED PROCESSING A PLURALITY OF | FREESCALE SEMICONDUCTOR, INC. | 7141860 | LDMOS TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. 7142401 DETECTING OVERCURRENTS IN A SWITCHING REGULATOR USING A VOLTAGE DEPENDENT REFERENCE FREESCALE SEMICONDUCTOR, INC. 7142597 FULL BRIDGE INTEGRAL NOISE SHAPING FOR QUANTIZATION OF PULSE WIDTH MODULATION SIGNALS FREESCALE SEMICONDUCTOR, INC. 7142606 METHOD AND APPARATUS FOR SHARED PROCESSING A PLURALITY OF | FREESCALE SEMICONDUCTOR, INC. | 7141989 | METHODS AND APPARATUS FOR A MEMS VARACTOR |
| FREESCALE SEMICONDUCTOR, INC. 7142597 FULL BRIDGE INTEGRAL NOISE SHAPING FOR QUANTIZATION OF PULSE WIDTH MODULATION SIGNALS FREESCALE SEMICONDUCTOR, INC. 7142606 METHOD AND APPARATUS FOR SHARED PROCESSING A PLURALITY OF | FREESCALE SEMICONDUCTOR, INC. | 7142058 | |
| WIDTH MODULATION SIGNALS FREESCALE SEMICONDUCTOR, INC. 7142606 METHOD AND APPARATUS FOR SHARED PROCESSING A PLURALITY OF | FREESCALE SEMICONDUCTOR, INC. | 7142401 | |
| | FREESCALE SEMICONDUCTOR, INC. | 7142597 | · · · · · · · · · · · · · · · · · · · |
| | FREESCALE SEMICONDUCTOR, INC. | 7142606 | |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7142665 | AUTOMATIC GAIN CONTROL FOR AN ADAPTIVE FINITE IMPULSE RESPONSE AND METHOD THEREFORE |
| FREESCALE SEMICONDUCTOR, INC. | 7142669 | CIRCUIT FOR GENERATING HASH VALUES |
| FREESCALE SEMICONDUCTOR, INC. | 7144784 | METHOD OF FORMING A SEMICONDUCTOR DEVICE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7144825 | MULTI-LAYER DIELECTRIC CONTAINING DIFFUSION BARRIER MATERIAL |
| FREESCALE SEMICONDUCTOR, INC. | 7145084 | RADIATION SHIELDED MODULE AND METHOD OF SHIELDING MICROELECTRONIC DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7145309 | OPEN LOOP MOTOR PARKING METHOD AND SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7146593 | METHOD OF IMPLEMENTING POLISHING UNIFORMITY AND MODIFYING LAYOUT DATA |
| FREESCALE SEMICONDUCTOR, INC. | 7149674 | METHODS FOR ANALYZING INTEGRATED CIRCUITS AND APPARATUS THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7151302 | METHOD AND APPARATUS FOR MAINTAINING TOPOGRAPHICAL UNIFORMITY OF A SEMICONDUCTOR MEMORY ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | 7151387 | ANALYSIS MODULE, INTEGRATED CIRCUIT, SYTEM AND METHOD FOR TESTING AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7151396 | CLOCK DELAY COMPENSATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7151695 | INTEGRATED CIRCUIT HAVING A NON-VOLATILE MEMORY WITH DISCHARGE RATE CONTROL AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7153726 | SEMICONDUCTOR DEVICE WITH MAGNETICALLY PERMEABLE HEAT SINK |
| FREESCALE SEMICONDUCTOR, INC. | 7154314 | COMMUNICATION APPARATUS INCLUDING DRIVER MEANS FOR APPLYING A SWITCHED SIGNAL TO A COMMUNICATION LINE WITH A CONTROLLED SLEW RATE |
| FREESCALE SEMICONDUCTOR, INC. | 7154719 | CIRCUIT FOR ELECTROSTATIC DISCHARGE PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 7157345 | SOURCE SIDE INJECTION STORAGE DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7157355 | METHOD OF MAKING A SEMICONDUCTOR DEVICE HAVING A STRAINED SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7157377 | METHOD OF MAKING A SEMICONDUCTOR DEVICE USING TREATED PHOTORESIST |
| FREESCALE SEMICONDUCTOR, INC. | 7158432 | MEMORY WITH ROBUST DATA SENSING AND METHOD FOR SENSING DATA |
| FREESCALE SEMICONDUCTOR, INC. | 7159459 | MULTIPLE MICROELECTROMECHANICAL (MEM) DEVICES FORMED ON A SINGLE SUBSTRATE AND SEALED AT DIFFERENT PRESSURES AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7160755 | METHOD OF FORMING A SUBSTRATELESS SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7160769 | CHANNEL ORIENTATION TO ENHANCE TRANSISTOR PERFORMANCE |
| FREESCALE SEMICONDUCTOR, INC. | 7160775 | METHOD OF DISCHARGING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7160798 | METHOD OF MAKING REINFORCED SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7161199 | TRANSISTOR STRUCTURE WITH STRESS MODIFICATION AND CAPACITIVE REDUCTION FEATURE IN A WIDTH DIRECTION AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7161822 | COMPACT NON-VOLATILE MEMORY ARRAY WITH REDUCED DISTURB |
| FREESCALE SEMICONDUCTOR, INC. | 7161827 | SRAM HAVING IMPROVED CELL STABILITY AND METHOD THEREFOR |
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| FREQUENCY AND SUPPLY VOLTAGE CORRELATION IN AN INTEGRATED CIRCUIT FREESCALE SEMICONDUCTOR, INC. 7166897 METHOD AND APPARATUS FOR PERFORMANCE ENHANCEMENT IN AN ASYMMETRICAL SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. 7169639 A METHOD FOR FABRICATING SEMICONDUCTOR STRUCTURES AND DEVICES ON VICINAL SUBSTRAITS IS INING A LOW TEMPERATURE, LOW PRESSURE, ALKALINE EARTH METAL RICH PROCESS FREESCALE SEMICONDUCTOR, INC. 7169694 METHOD FOR FORMING A BOND PAD INTERFACE FREESCALE SEMICONDUCTOR, INC. 7170165 ARRANGEMENT AND METHOD FOR ESD PROTECTION FREESCALE SEMICONDUCTOR, INC. 7170165 ARRANGEMENT AND METHOD FOR ESD PROTECTION FREESCALE SEMICONDUCTOR, INC. 7170165 ARRANGEMENT AND METHOD FOR ESD PROTECTION FREESCALE SEMICONDUCTOR, INC. 7170166 MISMATCH MODELING TOOL FREESCALE SEMICONDUCTOR, INC. 7170175 WARPAGE CONTROL OF ARRAY PACKAGING FREESCALE SEMICONDUCTOR, INC. 7170180 PARAMATICAL EXPOSURE CONTROL SYSTEM FOR A DIGITAL CAMERA FREESCALE SEMICONDUCTOR, INC. 7170191 PARAMATICAL EXPOSURE CONTROL SYSTEM FOR A DIGITAL CAMERA FREESCALE SEMICONDUCTOR, INC. 7170191 PARAMATICAL PROVINCE OF SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. 7170191 PARAMATICAL PROJECTION FREESCALE SEMICONDUCTOR, INC. 7170191 PARAMATICAL PROJECTION FOR SYSTEM FOR A DIGITAL CAMERA FREESCALE SEMICONDUCTOR, INC. 7170191 POLISHING PAD A POLISHING APPLATUS, AND A PROCESS FOR USING THE POLISHING PAD A PO | FREESCALE SEMICONDUCTOR, INC. | 7164566 | ELECTROSTATIC DISCHARGE PROTECTION DEVICE AND METHOD THEREFORE |
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| RERESCALE SEMICONDUCTOR, INC. 7170115 INTEGRATED CIRCUIT WELL BIAS CIRCUITRY PREESCALE SEMICONDUCTOR, INC. 7170135 ARRANGEMENT AND METHOD FOR ESD PROTECTION PREESCALE SEMICONDUCTOR, INC. 7171366 MISMATCH MODELING TOOL PREESCALE SEMICONDUCTOR, INC. 717367 WARPAGE CONTROLLER USEABLE IN A DATA PROCESSING SYSTEM PREESCALE SEMICONDUCTOR, INC. 717367 AUTOMATIC EXPOSURE CONTROL SYSTEM FOR A DIGITAL CAMERA PREESCALE SEMICONDUCTOR, INC. 7176130 PLASMA TREATMENT FOR SURFACE OF SEMICONDUCTOR DEVICE PREESCALE SEMICONDUCTOR, INC. 7176131 PLASMA TREATMENT FOR SURFACE OF SEMICONDUCTOR DEVICE PREESCALE SEMICONDUCTOR, INC. 7176134 ULTRA WIDE BANDWIDTH NOISE CANCELLATION MECHANISM AND METHOD PREESCALE SEMICONDUCTOR, INC. 7179151 POLISHING PAD, A POLISHING APPARATUS, AND A PROCESS FOR USING THE POLISHING PAD, A POLISHING APPARATUS, AND A PROCESS FOR USING THE POLISHING PAD, A POLISHING PAD A POLISHING SAME PREESCALE SEMICONDUCTOR, INC. 7179700 SEMICONDUCTOR DEVICE AND METHOD OF FORMING SAME PREESCALE SEMICONDUCTOR, INC. 7179712 MULTIBIT ROM CELL AND METHOD THEREFOR PREESCALE SEMICONDUCTOR, INC. 7180188 METHOD AND APPARATUS FOR ENTERING A LOW POWER MODE PREESCALE SEMICONDUCTOR, INC. 7181188 METHOD AND APPARATUS FOR ENTERING A LOW POWER MODE PREESCALE SEMICONDUCTOR, INC. 7181163 NETHOD OF FORMING AN INTEGRATED CIRCUIT HAVING NANOCLUSTER DEVICES AND NON-NANOCLUSTER DEVICES PREESCALE SEMICONDUCTOR, INC. 7183151 PROFINING AND INTEGRACE DIRECTION OF MANUNG PREESCALE SEMICONDUCTOR, INC. 7183161 PROGRAMMING AND ERASING STRUCTURE FOR A FLOATING GATE MEMORY CELL AND METHOD OF MAKING PREESCALE SEMICONDUCTOR, INC. 7183161 PROGRAMMING AND ERASING STRUCTURE FOR A FLOATING GATE MEMORY CELL AND METHOD OF MAKING PREESCALE SEMICONDUCTOR, INC. 7183161 PROGRAMMING AND ERASING STRUCTURE FOR A FLOATING GATE MEMORY CELL AND METHOD OF MAKING PREESCALE SEMICONDUCTOR, INC. 7183161 PROGRAMMING AND ERASING STRUCTURE FOR A FLOATING WIRELESS NETWORKS PREESCALE SEMICONDUCTOR, INC. 7183161 PROGRAMMING AND ERASING STRUCTURE FOR A FLOATING WIRELESS NETWORKS PREES | FREESCALE SEMICONDUCTOR, INC. | 7169619 | ON VICINAL SUBSTRATES USING A LOW TEMPERATURE, LOW PRESSURE, |
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| FREESCALE SEMICONDUCTOR, INC. 7180158 SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE FREESCALE SEMICONDUCTOR, INC. 7181188 METHOD AND APPARATUS FOR ENTERING A LOW POWER MODE FREESCALE SEMICONDUCTOR, INC. 7181638 METHOD AND APPARATUS FOR SKEWING DATA WITH RESPECT TO COMMAND ON A DDR INTERFACE FREESCALE SEMICONDUCTOR, INC. 7183159 METHOD OF FORMING AN INTEGRATED CIRCUIT HAVING NANOCLUSTER DEVICES AND NON-NANOCLUSTER DEVICES FREESCALE SEMICONDUCTOR, INC. 7183161 PROGRAMMING AND ERASING STRUCTURE FOR A FLOATING GATE MEMORY CELL AND METHOD OF MAKING FREESCALE SEMICONDUCTOR, INC. 7183817 HIGH SPEED OUTPUT BUFFER WITH AC-COUPLED LEVEL SHIFT AND DC LEVEL DETECTION AND CORRECTION FREESCALE SEMICONDUCTOR, INC. 7183848 TRANSCONDUCTANCE AMPLIFIER FREESCALE SEMICONDUCTOR, INC. 7184767 SYSTEM AND METHOD OF COMMUNICATION BETWEEN MULTIPLE POINT- COORDINATED WIRELESS NETWORKS FREESCALE SEMICONDUCTOR, INC. 7185121 METHOD OF ACCESSING MEMORY VIA MULTIPLE SLAVE PORTS FREESCALE SEMICONDUCTOR, INC. 7185170 DATA PROCESSING SYSTEM HAVING TRANSLATION LOOKASIDE BUFFER VALID BITS WITH LOCK AND METHOD THEREFOR | FREESCALE SEMICONDUCTOR, INC. | 7179700 | SEMICONDUCTOR DEVICE WITH LOW RESISTANCE CONTACTS |
| FREESCALE SEMICONDUCTOR, INC. 7181188 METHOD AND APPARATUS FOR ENTERING A LOW POWER MODE FREESCALE SEMICONDUCTOR, INC. 7181638 METHOD AND APPARATUS FOR SKEWING DATA WITH RESPECT TO COMMAND ON A DDR INTERFACE FREESCALE SEMICONDUCTOR, INC. 7183159 METHOD OF FORMING AN INTEGRATED CIRCUIT HAVING NANOCLUSTER DEVICES AND NON-NANOCLUSTER DEVICES FREESCALE SEMICONDUCTOR, INC. 7183161 PROGRAMMING AND ERASING STRUCTURE FOR A FLOATING GATE MEMORY CELL AND METHOD OF MAKING FREESCALE SEMICONDUCTOR, INC. 7183817 HIGH SPEED OUTPUT BUFFER WITH AC-COUPLED LEVEL SHIFT AND DC LEVEL DETECTION AND CORRECTION FREESCALE SEMICONDUCTOR, INC. 7183848 TRANSCONDUCTANCE AMPLIFIER FREESCALE SEMICONDUCTOR, INC. 7184719 METHOD FOR OPERATING MULTIPLE OVERLAPPING WIRELESS NETWORKS FREESCALE SEMICONDUCTOR, INC. 7184767 SYSTEM AND METHOD OF COMMUNICATION BETWEEN MULTIPLE POINT- COORDINATED WIRELESS NETWORKS FREESCALE SEMICONDUCTOR, INC. 7185121 METHOD OF ACCESSING MEMORY VIA MULTIPLE SLAVE PORTS FREESCALE SEMICONDUCTOR, INC. 7185170 DATA PROCESSING SYSTEM HAVING TRANSLATION LOOKASIDE BUFFER VALID BITS WITH LOCK AND METHOD THEREFOR | FREESCALE SEMICONDUCTOR, INC. | 7179712 | MULTIBIT ROM CELL AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. 7181638 METHOD AND APPARATUS FOR SKEWING DATA WITH RESPECT TO COMMAND ON A DDR INTERFACE FREESCALE SEMICONDUCTOR, INC. 7183159 METHOD OF FORMING AN INTEGRATED CIRCUIT HAVING NANOCLUSTER DEVICES AND NON-NANOCLUSTER DEVICES FREESCALE SEMICONDUCTOR, INC. 7183161 PROGRAMMING AND ERASING STRUCTURE FOR A FLOATING GATE MEMORY CELL AND METHOD OF MAKING FREESCALE SEMICONDUCTOR, INC. 7183817 HIGH SPEED OUTPUT BUFFER WITH AC-COUPLED LEVEL SHIFT AND DC LEVEL DETECTION AND CORRECTION FREESCALE SEMICONDUCTOR, INC. 7183825 STATE RETENTION WITHIN A DATA PROCESSING SYSTEM FREESCALE SEMICONDUCTOR, INC. 7183848 TRANSCONDUCTANCE AMPLIFIER FREESCALE SEMICONDUCTOR, INC. 7184719 METHOD FOR OPERATING MULTIPLE OVERLAPPING WIRELESS NETWORKS FREESCALE SEMICONDUCTOR, INC. 7185170 DATA PROCESSING MEMORY VIA MULTIPLE SLAVE PORTS 7185170 DATA PROCESSING SYSTEM HAVING TRANSLATION LOOKASIDE BUFFER VALID BITS WITH LOCK AND METHOD THEREFOR | FREESCALE SEMICONDUCTOR, INC. | 7180158 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE |
| ON A DDR INTERFACE FREESCALE SEMICONDUCTOR, INC. 7183159 METHOD OF FORMING AN INTEGRATED CIRCUIT HAVING NANOCLUSTER DEVICES AND NON-NANOCLUSTER DEVICES FREESCALE SEMICONDUCTOR, INC. 7183161 PROGRAMMING AND ERASING STRUCTURE FOR A FLOATING GATE MEMORY CELL AND METHOD OF MAKING FREESCALE SEMICONDUCTOR, INC. 7183817 HIGH SPEED OUTPUT BUFFER WITH AC-COUPLED LEVEL SHIFT AND DC LEVEL DETECTION AND CORRECTION FREESCALE SEMICONDUCTOR, INC. 7183825 STATE RETENTION WITHIN A DATA PROCESSING SYSTEM FREESCALE SEMICONDUCTOR, INC. 7183848 TRANSCONDUCTANCE AMPLIFIER FREESCALE SEMICONDUCTOR, INC. 7184719 METHOD FOR OPERATING MULTIPLE OVERLAPPING WIRELESS NETWORKS FREESCALE SEMICONDUCTOR, INC. 7184767 SYSTEM AND METHOD OF COMMUNICATION BETWEEN MULTIPLE POINT-COORDINATED WIRELESS NETWORKS FREESCALE SEMICONDUCTOR, INC. 7185121 METHOD OF ACCESSING MEMORY VIA MULTIPLE SLAVE PORTS FREESCALE SEMICONDUCTOR, INC. 7185170 DATA PROCESSING SYSTEM HAVING TRANSLATION LOOKASIDE BUFFER VALID BITS WITH LOCK AND METHOD THEREFOR | FREESCALE SEMICONDUCTOR, INC. | 7181188 | METHOD AND APPARATUS FOR ENTERING A LOW POWER MODE |
| DEVICES AND NON-NANOCLUSTER DEVICES FREESCALE SEMICONDUCTOR, INC. 7183161 PROGRAMMING AND ERASING STRUCTURE FOR A FLOATING GATE MEMORY CELL AND METHOD OF MAKING FREESCALE SEMICONDUCTOR, INC. 7183817 HIGH SPEED OUTPUT BUFFER WITH AC-COUPLED LEVEL SHIFT AND DC LEVEL DETECTION AND CORRECTION FREESCALE SEMICONDUCTOR, INC. 7183825 STATE RETENTION WITHIN A DATA PROCESSING SYSTEM FREESCALE SEMICONDUCTOR, INC. 7183848 TRANSCONDUCTANCE AMPLIFIER FREESCALE SEMICONDUCTOR, INC. 7184719 METHOD FOR OPERATING MULTIPLE OVERLAPPING WIRELESS NETWORKS FREESCALE SEMICONDUCTOR, INC. 7184767 SYSTEM AND METHOD OF COMMUNICATION BETWEEN MULTIPLE POINT-COORDINATED WIRELESS NETWORKS FREESCALE SEMICONDUCTOR, INC. 7185121 METHOD OF ACCESSING MEMORY VIA MULTIPLE SLAVE PORTS FREESCALE SEMICONDUCTOR, INC. 7185170 DATA PROCESSING SYSTEM HAVING TRANSLATION LOOKASIDE BUFFER VALID BITS WITH LOCK AND METHOD THEREFOR | FREESCALE SEMICONDUCTOR, INC. | 7181638 | METHOD AND APPARATUS FOR SKEWING DATA WITH RESPECT TO COMMAND ON A DDR INTERFACE |
| CELL AND METHOD OF MAKING FREESCALE SEMICONDUCTOR, INC. 7183817 HIGH SPEED OUTPUT BUFFER WITH AC-COUPLED LEVEL SHIFT AND DC LEVEL DETECTION AND CORRECTION FREESCALE SEMICONDUCTOR, INC. 7183825 STATE RETENTION WITHIN A DATA PROCESSING SYSTEM FREESCALE SEMICONDUCTOR, INC. 7183848 TRANSCONDUCTANCE AMPLIFIER FREESCALE SEMICONDUCTOR, INC. 7184719 METHOD FOR OPERATING MULTIPLE OVERLAPPING WIRELESS NETWORKS FREESCALE SEMICONDUCTOR, INC. 7184767 SYSTEM AND METHOD OF COMMUNICATION BETWEEN MULTIPLE POINT-COORDINATED WIRELESS NETWORKS FREESCALE SEMICONDUCTOR, INC. 7185121 METHOD OF ACCESSING MEMORY VIA MULTIPLE SLAVE PORTS FREESCALE SEMICONDUCTOR, INC. 7185170 DATA PROCESSING SYSTEM HAVING TRANSLATION LOOKASIDE BUFFER VALID BITS WITH LOCK AND METHOD THEREFOR | FREESCALE SEMICONDUCTOR, INC. | 7183159 | |
| LEVEL DETECTION AND CORRECTION FREESCALE SEMICONDUCTOR, INC. 7183825 STATE RETENTION WITHIN A DATA PROCESSING SYSTEM FREESCALE SEMICONDUCTOR, INC. 7183848 TRANSCONDUCTANCE AMPLIFIER FREESCALE SEMICONDUCTOR, INC. 7184719 METHOD FOR OPERATING MULTIPLE OVERLAPPING WIRELESS NETWORKS FREESCALE SEMICONDUCTOR, INC. 7184767 SYSTEM AND METHOD OF COMMUNICATION BETWEEN MULTIPLE POINT- COORDINATED WIRELESS NETWORKS FREESCALE SEMICONDUCTOR, INC. 7185121 METHOD OF ACCESSING MEMORY VIA MULTIPLE SLAVE PORTS FREESCALE SEMICONDUCTOR, INC. 7185170 DATA PROCESSING SYSTEM HAVING TRANSLATION LOOKASIDE BUFFER VALID BITS WITH LOCK AND METHOD THEREFOR | FREESCALE SEMICONDUCTOR, INC. | 7183161 | |
| FREESCALE SEMICONDUCTOR, INC. 7183848 TRANSCONDUCTANCE AMPLIFIER 7184719 METHOD FOR OPERATING MULTIPLE OVERLAPPING WIRELESS NETWORKS FREESCALE SEMICONDUCTOR, INC. 7184767 SYSTEM AND METHOD OF COMMUNICATION BETWEEN MULTIPLE POINT- COORDINATED WIRELESS NETWORKS FREESCALE SEMICONDUCTOR, INC. 7185121 METHOD OF ACCESSING MEMORY VIA MULTIPLE SLAVE PORTS 7185170 DATA PROCESSING SYSTEM HAVING TRANSLATION LOOKASIDE BUFFER VALID BITS WITH LOCK AND METHOD THEREFOR | FREESCALE SEMICONDUCTOR, INC. | 7183817 | |
| FREESCALE SEMICONDUCTOR, INC. 7184719 METHOD FOR OPERATING MULTIPLE OVERLAPPING WIRELESS NETWORKS 7184767 SYSTEM AND METHOD OF COMMUNICATION BETWEEN MULTIPLE POINT- COORDINATED WIRELESS NETWORKS FREESCALE SEMICONDUCTOR, INC. 7185121 METHOD OF ACCESSING MEMORY VIA MULTIPLE SLAVE PORTS FREESCALE SEMICONDUCTOR, INC. 7185170 DATA PROCESSING SYSTEM HAVING TRANSLATION LOOKASIDE BUFFER VALID BITS WITH LOCK AND METHOD THEREFOR | FREESCALE SEMICONDUCTOR, INC. | 7183825 | STATE RETENTION WITHIN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. 7184767 SYSTEM AND METHOD OF COMMUNICATION BETWEEN MULTIPLE POINT-COORDINATED WIRELESS NETWORKS FREESCALE SEMICONDUCTOR, INC. 7185121 METHOD OF ACCESSING MEMORY VIA MULTIPLE SLAVE PORTS 7185170 DATA PROCESSING SYSTEM HAVING TRANSLATION LOOKASIDE BUFFER VALID BITS WITH LOCK AND METHOD THEREFOR | FREESCALE SEMICONDUCTOR, INC. | 7183848 | TRANSCONDUCTANCE AMPLIFIER |
| COORDINATED WIRELESS NETWORKS FREESCALE SEMICONDUCTOR, INC. 7185121 METHOD OF ACCESSING MEMORY VIA MULTIPLE SLAVE PORTS 7185170 DATA PROCESSING SYSTEM HAVING TRANSLATION LOOKASIDE BUFFER VALID BITS WITH LOCK AND METHOD THEREFOR | FREESCALE SEMICONDUCTOR, INC. | 7184719 | METHOD FOR OPERATING MULTIPLE OVERLAPPING WIRELESS NETWORKS |
| FREESCALE SEMICONDUCTOR, INC. 7185170 DATA PROCESSING SYSTEM HAVING TRANSLATION LOOKASIDE BUFFER VALID BITS WITH LOCK AND METHOD THEREFOR | FREESCALE SEMICONDUCTOR, INC. | 7184767 | |
| VALID BITS WITH LOCK AND METHOD THEREFOR | FREESCALE SEMICONDUCTOR, INC. | 7185121 | METHOD OF ACCESSING MEMORY VIA MULTIPLE SLAVE PORTS |
| FREESCALE SEMICONDUCTOR, INC. 7185249 METHOD AND APPARATUS FOR SECURE SCAN TESTING | FREESCALE SEMICONDUCTOR, INC. | 7185170 | |
| | FREESCALE SEMICONDUCTOR, INC. | 7185249 | METHOD AND APPARATUS FOR SECURE SCAN TESTING |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7185251 | METHOD AND APPARATUS FOR AFFECTING A PORTION OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7186596 | VERTICAL DIODE FORMATION IN SOI APPLICATION |
| FREESCALE SEMICONDUCTOR, INC. | 7186616 | METHOD OF REMOVING NANOCLUSTERS IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7187197 | TRANSMISSION LINE DRIVER |
| FREESCALE SEMICONDUCTOR, INC. | 7187205 | INTEGRATED CIRCUIT STORAGE ELEMENT HAVING LOW POWER DATA RETENTION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7187600 | METHOD AND APPARATUS FOR PROTECTING AN INTEGRATED CIRCUIT FROM ERRONEOUS OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7188630 | METHOD TO PASSIVATE CONDUCTIVE SURFACES DURING SEMICONDUCTOR PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 7190150 | DC-DC CONVERTER FOR POWER LEVEL TRACKING POWER AMPLIFIERS |
| FREESCALE SEMICONDUCTOR, INC. | 7190213 | DIGITAL TIME CONSTANT TRACKING TECHNIQUE AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 7190279 | AUDIO MODULATED LIGHT SYSTEM FOR PERSONAL ELECTRONIC DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7190293 | ANALOG-TO-DIGITAL CONVERTER ARRANGEMENT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7191089 | SYSTEM AND METHOD FOR FALL DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | 7192855 | PECVD NITRIDE FILM |
| FREESCALE SEMICONDUCTOR, INC. | 7192876 | TRANSISTOR WITH INDEPENDENT GATE STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | 7193924 | DUAL-PORT STATIC RANDOM ACCESS MEMORY HAVING IMPROVED CELL STABILITY AND WRITE MARGIN |
| FREESCALE SEMICONDUCTOR, INC. | 7196427 | STRUCTURE HAVING AN INTEGRATED CIRCUIT ON ANOTHER INTEGRATED CIRCUIT WITH AN INTERVENING BENT ADHESIVE ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 7199306 | MULTI-STRAND SUBSTRATE FOR BALL-GRID ARRAY ASSEMBLIES AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7200056 | MEMORY ROW/COLUMN REPLACEMENT IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7200137 | ON CHIP NETWORK THAT MAXIMIZES INTERCONNECT UTILIZATION BETWEEN PROCESSING ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | 7200378 | ROCKING POTENTIAL-WELL SWITCH AND MIXER |
| FREESCALE SEMICONDUCTOR, INC. | 7200719 | PREFETCH CONTROL IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7202117 | METHOD OF MAKING A PLANAR DOUBLE-GATED TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 7202182 | METHOD OF PASSIVATING OXIDE/COMPOUND SEMICONDUCTOR INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | 7205178 | LAND GRID ARRAY PACKAGED DEVICE AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7205202 | SEMICONDUCTOR DEVICE AND METHOD FOR REGIONAL STRESS CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 7205210 | SEMICONDUCTOR STRUCTURE HAVING STRAINED SEMICONDUCTOR AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7205235 | METHOD FOR REDUCING CORROSION OF METAL SURFACES DURING SEMICONDUCTOR PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 7205608 | ELECTRONIC DEVICE INCLUDING DISCONTINUOUS STORAGE ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | 7206244 | TEMPERATURE BASED DRAM REFRESH |
| FREESCALE SEMICONDUCTOR, INC. | 7208357 | TEMPLATE LAYER FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7208390 | SEMICONDUCTOR DEVICE STRUCTURE AND METHOD FOR FORMING |
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7208424 METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING A METAL LAYER

FREESCALE SEMICONDUCTOR, INC.

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7208841 | SEMICONDUCTOR DEVICE WITH STRAIN RELIEVING BUMP DESIGN |
| FREESCALE SEMICONDUCTOR, INC. | 7209332 | TRANSIENT DETECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7209469 | METHOD AND SYSTEM FOR PERFORMING RANGING FUNCTIONS IN AN ULTRAWIDE BANDWIDTH SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7211466 | STACKED DIE SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7211477 | HIGH VOLTAGE FIELD EFFECT DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7211487 | PROCESS FOR FORMING AN ELECTRONIC DEVICE INCLUDING DISCONTINUOUS STORAGE ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | 7211852 | STRUCTURE AND METHOD FOR FABRICATING GAN DEVICES UTILIZING THE FORMATION OF A COMPLIANT SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 7211858 | SPLIT GATE STORAGE DEVICE INCLUDING A HORIZONTAL FIRST GATE AND A VERTICAL SECOND GATE IN A TRENCH |
| FREESCALE SEMICONDUCTOR, INC. | 7212587 | APPARATUS FOR REDUCING DC OFFSET IN A RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 7212799 | METHOD AND APPARATUS FOR ACQUIRING AND TRACKING ULTRAWIDE BANDWIDTH SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 7214590 | METHOD OF FORMING AN ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7215014 | SOLDERABLE METAL FINISH FOR INTEGRATED CIRCUIT PACKAGE LEADS AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 7215150 | METHOD AND CIRCUIT FOR MAINTAINING I/O PAD CHARACTERISTICS ACROSS DIFFERENT I/O SUPPLY VOLTAGES |
| FREESCALE SEMICONDUCTOR, INC. | 7215188 | INTEGRATED CIRCUIT HAVING A LOW POWER MODE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7215268 | SIGNAL CONVERTERS WITH MULTIPLE GATE DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7215765 | METHOD AND APPARATUS FOR PURE DELAY ESTIMATION IN A COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7217643 | SEMICONDUCTOR STRUCTURES AND METHODS FOR FABRICATING SEMICONDUCTOR STRUCTURES COMPRISING HIGH DIELECTRIC CONSTANT STACKED STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | 7217667 | PROCESSES FOR FORMING ELECTRONIC DEVICES INCLUDING A SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7218119 | SYSTEM AND METHOD FOR REDUCING CURRENT IN A DEVICE DURING TESTING |
| FREESCALE SEMICONDUCTOR, INC. | 7220632 | METHOD OF FORMING A SEMICONDUCTOR DEVICE AND AN OPTICAL DEVICE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7221006 | GeSOI TRANSISTOR WITH LOW JUNCTION CURRENT AND LOW JUNCTION CAPACITANCE AND METHOD FOR MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7221188 | LOGIC CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | 7221221 | POWER AMPLIFIER WITH PRE-DISTORTER |
| FREESCALE SEMICONDUCTOR, INC. | 7221613 | MEMORY WITH SERIAL INPUT/OUTPUT TERMINALS FOR ADDRESS AND DATA AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7224711 | SYSTEM AND METHOD FOR THE MITIGATION OF SPECTRAL LINES IN AN ULTRAWIDE BANDWIDTH TRANSCEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 7224938 | METHOD OF COMMUNICATING WITH A NETWORK DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7226802 | TUNGSTEN COATED SILICON FINGERS |
| FREESCALE SEMICONDUCTOR, INC. | 7226820 | TRANSISTOR FABRICATION USING DOUBLE ETCH/REFILL PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 7226833 | SEMICONDUCTOR DEVICE STRUCTURE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7226840 | PROCESS FOR FORMING AN ELECTRONIC DEVICE INCLUDING DISCONTINUOUS STORAGE ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | 7227366 | DEVICE AND METHOD FOR BIASING A TRANSISTOR THAT IS CONNECTED TO A POWER CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 7227783 | MEMORY STRUCTURE AND METHOD OF PROGRAMMING |

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7228120 | CIRCUIT AND METHOD FOR REDUCING DIRECT CURRENT BIASES |
| FREESCALE SEMICONDUCTOR, INC. | 7228401 | INTERFACING A PROCESSOR TO A COPROCESSOR IN WHICH THE PROCESSOR SELECTIVELY ALTERS AN EXECUTION MODE OF THE COPROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 7229903 | RECESSED SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7230264 | SEMICONDUCTOR TRANSISTOR HAVING STRUCTURAL ELEMENTS OF DIFFERING MATERIALS |
| FREESCALE SEMICONDUCTOR, INC. | 7230505 | VOLTAGE CONTROLLED OSCILLATOR WITH GAIN CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 7232701 | MICROELECTROMECHANICAL (MEM) DEVICE WITH A PROTECTIVE CAP THAT FUNCTIONS AS A MOTION STOP |
| FREESCALE SEMICONDUCTOR, INC. | 7233539 | NON-VOLATILE MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | 7235471 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING A SILICIDE LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7235473 | DUAL SILICIDE SEMICONDUCTOR FABRICATION PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 7235502 | TRANSITIONAL DIELECTRIC LAYER TO IMPROVE RELIABILITY AND PERFORMANCE OF HIGH DIELECTRIC CONSTANT TRANSISTORS |
| FREESCALE SEMICONDUCTOR, INC. | 7235823 | SOURCE SIDE INJECTION STORAGE DEVICE WITH SPACER GATES AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7235847 | SEMICONDUCTOR DEVICE HAVING A GATE WITH A THIN CONDUCTIVE LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7235959 | LOW DROP-OUT VOLTAGE REGULATOR AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7236014 | CIRCUIT AND METHOD FOR PEAK DETECTION OF AN ANALOG SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 7236190 | DIGITAL IMAGE PROCESSING USING WHITE BALANCE AND GAMMA CORRECTION |
| FREESCALE SEMICONDUCTOR, INC. | 7236339 | ELECTROSTATIC DISCHARGE CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7236402 | METHOD AND APPARATUS FOR PROGRAMMING/ERASING A NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 7236756 | TUNING SIGNAL GENERATOR AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7238555 | SINGLE TRANSISTOR MEMORY CELL WITH REDUCED PROGRAMMING VOLTAGES |
| FREESCALE SEMICONDUCTOR, INC. | 7238561 | METHOD FOR FORMING UNIAXIALLY STRAINED DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7238579 | SEMICONDUCTOR DEVICE FOR REDUCING PHOTOVOLTAIC CURRENT |
| FREESCALE SEMICONDUCTOR, INC. | 7238580 | SEMICONDUCTOR FABRICATION PROCESS EMPLOYING STRESS INDUCING SOURCE DRAIN STRUCTURES WITH GRADED IMPURITY CONCENTRATION |
| FREESCALE SEMICONDUCTOR, INC. | 7238601 | SEMICONDUCTOR DEVICE HAVING CONDUCTIVE SPACERS IN SIDEWALL REGIONS AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 7238990 | INTERLAYER DIELECTRIC UNDER STRESS FOR AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7239182 | PREDRIVER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7240041 | NETWORK MESSAGE PROCESSING USING INVERSE PATTERN MATCHING |
| FREESCALE SEMICONDUCTOR, INC. | 7240304 | METHOD FOR VOLTAGE DROP ANALYSIS IN INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 7241636 | METHOD AND APPARATUS FOR PROVIDING STRUCTURAL SUPPORT FOR INTERCONNECT PAD WHILE ALLOWING SIGNAL CONDUCTANCE |
| FREESCALE SEMICONDUCTOR, INC. | 7241647 | GRADED SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7241691 | CONDUCTING METAL OXIDE WITH ADDITIVE AS P-MOS DEVICE ELECTRODE |
| FREESCALE SEMICONDUCTOR, INC. | 7241695 | SEMICONDUCTOR DEVICE HAVING NANO-PILLARS AND METHOD THEREFOR |

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| FREESCALE SEMICONDUCTOR, INC. | 7242285 | APPARATUS AND METHOD FOR POWER MANAGEMENT IN A TIRE PRESSURE MONITORING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7242626 | METHOD AND APPARATUS FOR LOW VOLTAGE WRITE IN A STATIC RANDOM ACCESS MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 7242762 | MONITORING AND CONTROL OF AN ADAPTIVE FILTER IN A COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7244989 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7245246 | CONVERTER, CIRCUIT AND METHOD FOR COMPENSATION OF NON-IDEALITIES IN CONTINOUS TIME SIGMA DELTA CONVERTERS. |
| FREESCALE SEMICONDUCTOR, INC. | 7245519 | DIGITALLY PROGRAMMABLE CAPACITOR ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | 7247552 | INTEGRATED CIRCUIT HAVING STRUCTURAL SUPPORT FOR A FLIP-CHIP INTERCONNECT PAD AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7248069 | METHOD AND APPARATUS FOR PROVIDING SECURITY FOR DEBUG CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | 7248172 | SYSTEM AND METHOD FOR HUMAN BODY FALL DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | 7248659 | METHOD FOR ADJUSTING ACQUISITION SPEED IN A WIRELESS NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 7249223 | PREFETCHING IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7249288 | METHOD AND APPARATUS FOR NON-INTRUSIVE TRACING |
| FREESCALE SEMICONDUCTOR, INC. | 7250340 | METHOD OF FABRICATING PROGRAMMABLE STRUCTURE INCLUDING DISCONTINUOUS STORAGE ELEMENTS AND SPACER CONTROL GATES IN A TRENCH |
| FREESCALE SEMICONDUCTOR, INC. | 7251797 | PESSIMISM REDUCTION IN CROSSTALK NOISE AWARE STATIC TIMING ANALYSIS |
| FREESCALE SEMICONDUCTOR, INC. | 7253455 | PHEMT WITH BARRIER OPTIMIZED FOR LOW TEMPERATURE OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7253486 | FIELD PLATE TRANSISTOR WITH REDUCED FIELD PLATE RESISTANCE |
| FREESCALE SEMICONDUCTOR, INC. | 7253595 | LOW DROP-OUT VOLTAGE REGULATOR |
| FREESCALE SEMICONDUCTOR, INC. | 7254003 | DIFFERENTIAL NULLING AVALANCHE (DNA) CLAMP CIRCUIT AND METHOD OF USE |
| FREESCALE SEMICONDUCTOR, INC. | 7254080 | FUSE CIRCUIT AND ELECTRONIC CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7256077 | METHOD FOR REMOVING A SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7256454 | ELECTRONIC DEVICE INCLUDING DISCONTINUOUS STORAGE ELEMENTS AND A PROCESS FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7256471 | ANTIFUSE ELEMENT AND ELECTRICALLY REDUNDANT ANTIFUSE ARRAY FOR CONTROLLED RUPTURE LOCATION |
| FREESCALE SEMICONDUCTOR, INC. | 7256488 | SEMICONDUCTOR PACKAGE WITH CROSSING CONDUCTOR ASSEMBLY AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7256657 | VOLTAGE CONTROLLED OSCILLATOR HAVING DIGITALLY CONTROLLED PHASE ADJUSTMENT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7259634 | ARRANGEMENT AND METHOD FOR DIGITAL DELAY LINE |
| FREESCALE SEMICONDUCTOR, INC. | 7259999 | NON-VOLATILE EMORY CELL ARRAY FOR IMPROVED DATA RETENTION AND METHOD OF OPERATING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7260105 | REDUCED PEAK EMI BUS USING VARIABLE BIT RATE SPREADING |
| FREESCALE SEMICONDUCTOR, INC. | 7260163 | NOISE BLANKER USING AN ADAPTIVE ALL-POLE PREDICTOR AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7261003 | FLOWMETER AND METHOD FOR THE MAKING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7261230 | WIREBONDING INSULATED WIRE AND CAPILLARY THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7262105 | SEMICONDUCTOR DEVICE WITH SILICIDED SOURCE/DRAINS |

7262494 THREE DIMENSIONAL PACKAGE

FREESCALE SEMICONDUCTOR, INC.

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7262615 | METHOD AND APPARATUS FOR TESTING A SEMICONDUCTOR STRUCTURE HAVING TOP-SIDE AND BOTTOM-SIDE CONNECTIONS |
| FREESCALE SEMICONDUCTOR, INC. | 7262617 | METHOD FOR TESTING INTEGRATED CIRCUIT, AND WAFER |
| FREESCALE SEMICONDUCTOR, INC. | 7262655 | HIGH BANDWIDTH RESISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 7262667 | RADIO FREQUENCY POWER AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 7262671 | AMPLITUDE LEVEL CONTROL CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7262997 | ELECTRONIC DEVICE INCLUDING A MEMORY ARRAY AND CONDUCTIVE LINES |
| FREESCALE SEMICONDUCTOR, INC. | 7264986 | MICROELECTRONIC ASSEMBLY AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7265004 | ELECTRONIC DEVICES INCLUDING A SEMICONDUCTOR LAYER AND A PROCESS FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7265059 | MULTIPLE FIN FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7265534 | TEST SYSTEM FOR DEVICE CHARACTERIZATION |
| FREESCALE SEMICONDUCTOR, INC. | 7265994 | UNDERFILL FILM FOR PRINTED WIRING ASSEMBLIES |
| FREESCALE SEMICONDUCTOR, INC. | 7266848 | INTEGRATED CIRCUIT SECURITY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7268463 | STRESS RELEASE MECHANISM IN MEMS DEVICE AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7268524 | VOLTAGE REGULATOR WITH ADAPTIVE FREQUENCY COMPENSATION |
| FREESCALE SEMICONDUCTOR, INC. | 7268588 | CASCADABLE LEVEL SHIFTER CELL |
| FREESCALE SEMICONDUCTOR, INC. | 7268715 | GAIN CONTROL IN A SIGNAL PATH WITH SIGMA-DELTA ANALOG-TO DIGITAL CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | 7269090 | MEMORY ACCESS WITH CONSECUTIVE ADDRESSES CORRESPONDING TO DIFFERENT ROWS |
| FREESCALE SEMICONDUCTOR, INC. | 7271013 | SEMICONDUCTOR DEVICE HAVING A BOND PAD AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7271069 | SEMICONDUCTOR DEVICE HAVING A PLURALITY OF DIFFERENT LAYERS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7271469 | METHODS OF MAKING INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 7272053 | INTEGRATED CIRCUIT HAVING A NON-VOLATILE MEMORY WITH DISCHARGE RATE CONTROL AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7272178 | METHOD AND APPARATUS FOR CONTROLLING THE BANDWIDTH FREQUENCY OF AN ANALOG FILTER |
| FREESCALE SEMICONDUCTOR, INC. | 7272767 | METHODS AND APPARATUS FOR INCORPORATING IDDQ TESTING INTO LOGIC BIST |
| FREESCALE SEMICONDUCTOR, INC. | 7273762 | MICROELECTROMECHANICAL (MEM) DEVICE INCLUDING A SPRING RELEASE BRIDGE AND METHOD OF MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7274203 | DESIGN-FOR-TEST CIRCUIT FOR LOW PIN COUNT DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7274247 | SYSTEM, METHOD AND PROGRAM PRODUCT FOR WELL-BIAS SET POINT ADJUSTMENT |
| FREESCALE SEMICONDUCTOR, INC. | 7275148 | DATA PROCESSING SYSTEM USING MULTIPLE ADDRESSING MODES FOR SIMD OPERATIONS AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7276406 | TRANSISTOR STRUCTURE WITH DUAL TRENCH FOR OPTIMIZED STRESS EFFECT AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7276419 | SEMICONDUCTOR DEVICE AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7276420 | METHOD OF MANUFACTURING A PASSIVE INTEGRATED MATCHING NETWORK FOR POWER AMPLIFIERS |
| FREESCALE SEMICONDUCTOR, INC. | 7276435 | DIE LEVEL METAL DENSITY GRADIENT FOR IMPROVED FLIP CHIP PACKAGE RELIABILITY |
| FREESCALE SEMICONDUCTOR, INC. | 7276456 | ARTICLE COMPRISING AN OXIDE LAYER ON A GAAS-BASED SEMICONDUCTOR STRUCTURE AND METHOD OF FORMING SAME |

| Owner | Patent # | Description |
|-------------------------------|----------|---|
| FREESCALE SEMICONDUCTOR, INC. | 7276974 | METHOD AND APPARATUS FOR PROTECTING RF POWER AMPLIFIERS |
| FREESCALE SEMICONDUCTOR, INC. | 7277449 | ON CHIP NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 7278062 | METHOD AND APPARATUS FOR RESPONDING TO ACCESS ERRORS IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7279409 | METHOD FOR FORMING MULTI-LAYER BUMPS ON A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 7279433 | DEPOSITION AND PATTERNING OF BORON NITRIDE NANOTUBE ILD |
| FREESCALE SEMICONDUCTOR, INC. | 7279907 | METHOD OF TESTING FOR POWER AND GROUND CONTINUITY OF A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7279959 | CHARGE PUMP SYSTEM WITH REDUCED RIPPLE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7279997 | VOLTAGE CONTROLLED OSCILLATOR WITH A MULTIPLE GATE TRANSISTOR AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7280518 | METHOD OF OPERATING A MEDIA ACCESS CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | 7280601 | METHOD FOR OPERATING MULTIPLE OVERLAPPING WIRELESS NETWORKS |
| FREESCALE SEMICONDUCTOR, INC. | 7280607 | ULTRA WIDE BANDWIDTH COMMUNICATIONS METHOD AND SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7280615 | METHOD FOR MAKING A CLEAR CHANNEL ASSESSMENT IN A WIRELESS NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 7282307 | REFLECTIVE MASK USEFUL FOR TRANSFERRING A PATTERN USING EXTREME ULTRAVIOLET (EUV) RADIATION AND METHOD OF MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7282386 | SCHOTTKY DEVICE AND METHOD OF FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 7282395 | METHOD OF MAKING EXPOSED PAD BALL GRID ARRAY PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7282402 | METHOD OF MAKING A DUAL STRAINED CHANNEL SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7282415 | METHOD FOR MAKING A SEMICONDUCTOR DEVICE WITH STRAIN ENHANCEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 7282426 | METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING ASYMMETRIC DIELECTRIC REGIONS AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7282929 | APPARATUS FOR CURRENT SENSING |
| FREESCALE SEMICONDUCTOR, INC. | 7283004 | PHASE LOCKED LOOP FILTER |
| FREESCALE SEMICONDUCTOR, INC. | 7284231 | LAYOUT MODIFICATION USING MULTILAYER-BASED CONSTRAINTS |
| FREESCALE SEMICONDUCTOR, INC. | 7285452 | METHOD TO SELECTIVELY FORM REGIONS HAVING DIFFERING PROPERTIES AND STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7285819 | NONVOLATILE STORAGE ARRAY WITH CONTINUOUS CONTROL GATE EMPLOYING HOT CARRIER INJECTION PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | 7285832 | MULTIPORT SINGLE TRANSISTOR BIT CELL |
| FREESCALE SEMICONDUCTOR, INC. | 7285855 | PACKAGED DEVICE AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7285976 | INTEGRATED CIRCUIT WITH PROGRAMMABLE-IMPEDENCE OUTPUT BUFFER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7286070 | RF CARRIER GENERATOR AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7286423 | BIT LINE PRECHARGE IN EMBEDDED MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 7287210 | CONVOLUTIONAL ENCODER AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7288447 | SEMICONDUCTOR DEVICE HAVING TRENCH ISOLATION FOR DIFFERENTIAL STRESS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7288448 | METHOD AND APPARATUS FOR MOBILITY ENHANCEMENT IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7288458 | SOI ACTIVE LAYER WITH DIFFERENT SURFACE ORIENTATION |

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7288820 | LOW VOLTAGE NMOS-BASED ELECTROSTATIC DISCHARGE CLAMP |
| FREESCALE SEMICONDUCTOR, INC. | 7289052 | SYSTEM AND METHOD FOR ANALOG-TO-DIGITAL CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | 7289352 | SEMICONDUCTOR STORAGE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7289535 | METHOD OF ACCOMMODATING FRAGMENTATION AND BURST IN A WIRELESS PROTOCOL |
| FREESCALE SEMICONDUCTOR, INC. | 7289790 | SYSTEM FOR PROVIDING DEVICE AUTHENTICATION IN A WIRELESS NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 7291521 | SELF CORRECTING SUPPRESSION OF THRESHOLD VOLTAGE VARIATION IN FULLY DEPLETED TRANSISTORS |
| FREESCALE SEMICONDUCTOR, INC. | 7292073 | TRANSMISSION LINE DRIVER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7292485 | SRAM HAVING VARIABLE POWER SUPPLY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7292495 | INTEGRATED CIRCUIT HAVING A MEMORY WITH LOW VOLTAGE READ/WRITE OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7292622 | METHOD AND APPARATUS FOR RAKING IN A WIRELESS NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 7292827 | SYSTEM AND METHOD FOR PROVIDING A SINGLE-ENDED RECEIVE PORTION AND A DIFFERENTIAL TRANSMIT PORTION IN A WIRELESS TRANSCEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 7293153 | METHOD AND SYSTEM FOR DIRECT ACCESS TO A NON-MEMORY MAPPED DEVICE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 7293188 | LOW VOLTAGE DETECTION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7295484 | TEMPERATURE BASED DRAM REFRESH |
| FREESCALE SEMICONDUCTOR, INC. | 7295487 | STORAGE CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7296137 | MEMORY MANAGEMENT CIRCUITRY TRANSLATION INFORMATION RETRIEVAL DURING DEBUGGING |
| FREESCALE SEMICONDUCTOR, INC. | 7296248 | METHOD AND APPARATUS FOR COMPILING A PARAMETERIZED CELL |
| FREESCALE SEMICONDUCTOR, INC. | 7297586 | NOVEL GATE DIELECTRIC AND METAL GATE INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | 7297588 | ELECTRONIC DEVICE COMPRISING A GATE ELECTRODE INCLUDING A METAL-CONTAINING LAYER HAVING ONE OR MORE IMPURITIES AND A PROCESS FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7299335 | TRANSLATION INFORMATION RETRIEVAL TRANSPARENT TO PROCESSOR CORE |
| FREESCALE SEMICONDUCTOR, INC. | 7301187 | HIGH VOLTAGE FIELD EFFECT DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7301225 | MULTI-ROW LEAD FRAME |
| FREESCALE SEMICONDUCTOR, INC. | 7301378 | CIRCUIT AND METHOD FOR DETERMINING OPTIMAL POWER AND FREQUENCY METRICS OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7301741 | INTEGRATED CIRCUIT WITH MULTIPLE INDEPENDENT GATE FIELD EFFECT TRANSISTOR (MIGFET) RAIL CLAMP CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7303983 | ALD GATE ELECTRODE |
| FREESCALE SEMICONDUCTOR, INC. | 7304975 | METHOD FOR PROVIDING RAPID DELAYED FRAME ACKNOWLEDGMENT IN A WIRELESS TRANSCEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 7305223 | RADIO FREQUENCY CIRCUIT WITH INTEGRATED ON-CHIP RADIO FREQUENCY SIGNAL COUPLER |
| FREESCALE SEMICONDUCTOR, INC. | 7305642 | METHOD OF TILING ANALOG CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 7305643 | METHOD OF TILING ANALOG CIRCUITS THAT INCLUDE RESISTORS AND CAPACITORS |
| FREESCALE SEMICONDUCTOR, INC. | 7306986 | METHOD OF MAKING A SEMICONDUCTOR DEVICE, AND SEMICONDUCTOR DEVICE MADE THEREBY |
| FREESCALE SEMICONDUCTOR, INC. | 7307572 | PROGRAMMABLE DUAL INPUT SWITCHED-CAPACITOR GAIN STAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7308658 | METHOD AND APPARATUS FOR MEASURING TEST COVERAGE |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7309638 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT |
| FREESCALE SEMICONDUCTOR, INC. | 7312129 | METHOD FOR PRODUCING TWO GATES CONTROLLING THE SAME CHANNEL |
| FREESCALE SEMICONDUCTOR, INC. | 7312654 | QUIET POWER UP AND POWER DOWN OF A DIGITAL AUDIO AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 7314798 | METHOD OF FABRICATING A NONVOLATILE STORAGE ARRAY WITH CONTINUOUS CONTROL GATE EMPLOYING HOT CARRIER INJECTION PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | 7315268 | INTEGRATOR CURRENT MATCHING |
| FREESCALE SEMICONDUCTOR, INC. | 7315564 | ANALOG SIGNAL SEPARATOR FOR UWB VERSUS NARROWBAND SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 7315932 | DATA PROCESSING SYSTEM HAVING INSTRUCTION SPECIFIERS FOR SIMD REGISTER OPERANDS AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7316965 | SUBSTRATE CONTACT FOR A CAPPED MEMS AND METHOD OF MAKING THE SUBSTRATE CONTACT AT THE WAFER LEVEL |
| FREESCALE SEMICONDUCTOR, INC. | 7317222 | MEMORY CELL USING A DIELECTRIC HAVING NON-UNIFORM THICKNESS |
| FREESCALE SEMICONDUCTOR, INC. | 7317345 | ANTI-GATE LEAKAGE PROGRAMMABLE CAPACITOR |
| FREESCALE SEMICONDUCTOR, INC. | 7320931 | INTERFACIAL LAYER FOR USE WITH HIGH K DIELECTRIC MATERIALS |
| FREESCALE SEMICONDUCTOR, INC. | 7322000 | METHODS AND APPARATUS FOR EXTENDING SEMICONDUCTOR CHIP TESTING WITH BOUNDARY SCAN REGISTERS |
| FREESCALE SEMICONDUCTOR, INC. | 7322014 | METHOD OF IMPLEMENTING POLISHING UNIFORMITY AND MODIFYING LAYOUT DATA |
| FREESCALE SEMICONDUCTOR, INC. | 7323094 | PROCESS FOR DEPOSITING A LAYER OF MATERIAL ON A SUBSTRATE AND A PLATING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7323355 | METHOD OF FORMING A MICROELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7323373 | METHOD OF FORMING A SEMICONDUCTOR DEVICE WITH DECREASED UNDERCUTTING OF SEMICONDUCTOR MATERIAL |
| FREESCALE SEMICONDUCTOR, INC. | 7323389 | METHOD OF FORMING A FINFET STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7324790 | WIRELESS TRANSCEIVER AND METHOD OF OPERATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7327194 | LOW VOLTAGE LOW POWER CLASS A/B OUTPUT STAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7327288 | VARIABLE INTERPOLATOR FOR NON-UNIFORMLY SAMPLED SIGNALS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7327993 | LOW LEAKAGE LOCAL OSCILLATOR SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7329566 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7332414 | CHEMICAL DIE SINGULATION TECHNIQUE |
| FREESCALE SEMICONDUCTOR, INC. | 7332979 | LOW NOISE REFERENCE OSCILLATOR WITH FAST START-UP |
| FREESCALE SEMICONDUCTOR, INC. | 7333814 | METHOD OF ACCOMMODATING OVERLAPPING ADJACENT NETWORKS |
| FREESCALE SEMICONDUCTOR, INC. | 7334059 | MULTIPLE BURST PROTOCOL DEVICE CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | 7335602 | CHARGE-FREE LAYER BY LAYER ETCHING OF DIELECTRICS |
| FREESCALE SEMICONDUCTOR, INC. | 7335955 | ESD PROTECTION FOR PASSIVE INTEGRATED DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7336533 | ELECTRONIC DEVICE AND METHOD FOR OPERATING A MEMORY CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7338894 | SEMICONDUCTOR DEVICE HAVING NITRIDATED OXIDE LAYER AND METHOD THEREFOR |
| | | |

FREESCALE SEMICONDUCTOR, INC. 7339241 FINFET STRUCTURE WITH CONTACTS

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7339267 | SEMICONDUCTOR PACKAGE AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7339275 | MULTI-CHIPS SEMICONDUCTOR DEVICE ASSEMBLIES AND METHODS FOR FABRICATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7339404 | DEGLITCH FILTER |
| FREESCALE SEMICONDUCTOR, INC. | 7339442 | BASEBAND RC FILTER POLE AND ON-CHIP CURRENT TRACKING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7339499 | KEYPAD SIGNAL INPUT APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 7339775 | OVERCURRENT PROTECTION CIRCUIT AND DC POWER SUPPLY |
| FREESCALE SEMICONDUCTOR, INC. | 7340178 | CONVERSION BETWEEN OPTICAL AND RADIO FREQUENCY SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 7340542 | DATA PROCESSING SYSTEM WITH BUS ACCESS RETRACTION |
| FREESCALE SEMICONDUCTOR, INC. | 7341914 | METHOD FOR FORMING A NON-VOLATILE MEMORY AND A PERIPHERAL DEVICE ON A SEMICONDUCTOR SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 7341915 | METHOD OF MAKING PLANAR DOUBLE GATE SILICON-ON INSULATOR STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | 7342276 | METHOD AND APPARATUS UTILIZING MONOCRYSTALLINE INSULATOR |
| FREESCALE SEMICONDUCTOR, INC. | 7342518 | DIGITAL RATE CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 7342833 | NONVOLATILE MEMORY CELL PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | 7344917 | METHOD FOR PACKAGING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7344933 | METHOD OF FORMING DEVICE HAVING A RAISED EXTENSION REGION |
| FREESCALE SEMICONDUCTOR, INC. | 7345344 | EMBEDDED SUBSTRATE INTERCONNECT FOR UNDERSIDE CONTACT TO SOURCE AND DRAIN REGIONS |
| FREESCALE SEMICONDUCTOR, INC. | 7345545 | ENHANCEMENT MODE TRANSCEIVER AND SWITCHED GAIN AMPLIFIER INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7346120 | METHOD AND SYSTEM FOR PERFORMING DISTANCE MEASURING AND DIRECTION FINDING USING ULTRAWIDE BANDWIDTH TRANSMISSIONS |
| FREESCALE SEMICONDUCTOR, INC. | 7346820 | TESTING OF DATA RETENTION LATCHES IN CIRCUIT DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7348829 | SLEW RATE CONTROL OF A CHARGE PUMP |
| FREESCALE SEMICONDUCTOR, INC. | 7349266 | MEMORY DEVICE WITH A DATA HOLD LATCH |
| FREESCALE SEMICONDUCTOR, INC. | 7352333 | FREQUENCY-NOTCHING ANTENNA |
| FREESCALE SEMICONDUCTOR, INC. | 7352631 | METHODS FOR PROGRAMMING A FLOATING BODY NONVOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 7352793 | SYSTEM AND METHOD FOR ULTRA WIDEBAND COMMUNICATIONS USING MULTIPLE CODE WORDS |
| FREESCALE SEMICONDUCTOR, INC. | 7353311 | METHOD OF ACCESSING INFORMATION AND SYSTEM THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7354814 | SEMICONDUCTOR PROCESS WITH FIRST TRANSISTOR TYPES ORIENTED IN A FIRST PLANE AND SECOND TRANSISTOR TYPES ORIENTED IN A SECOND PLANE |
| FREESCALE SEMICONDUCTOR, INC. | 7354831 | MULTI-CHANNEL TRANSISTOR STRUCTURE AND METHOD OF MAKING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7355260 | SCHOTTKY DEVICE AND METHOD OF FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 7355289 | PACKAGED INTEGRATED CIRCUIT WITH ENHANCED THERMAL DISSIPATION |
| FREESCALE SEMICONDUCTOR, INC. | 7355456 | WIDE LINEAR RANGE PEAK DETECTOR |
| FREESCALE SEMICONDUCTOR, INC. | 7356628 | PACKET SWITCH WITH MULTIPLE ADDRESSABLE COMPONENTS |
| FREESCALE SEMICONDUCTOR, INC. | 7358616 | SEMICONDUCTOR STACKED DIE/WAFER CONFIGURATION AND PACKAGING |

AND METHOD THEREOF SCHEDULE 1B (Patents)

| <u>Owner</u> | Patent # | Description |
|-------------------------------|----------|--|
| FREESCALE SEMICONDUCTOR, INC. | 7358743 | ACCUMULATED CURRENT COUNTER AND METHOD THEREOF |
| REESCALE SEMICONDUCTOR, INC. | 7358792 | DISCHARGE DEVICE AND DC POWER SUPPLY SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7358796 | INPUT CIRCUIT FOR RECEIVING A VARIABLE VOLTAGE INPUT SIGNAL AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7359459 | SYSTEM AND MEDHOT FOR LOW POWER CLEAR CHANNEL ASSESSMENT |
| FREESCALE SEMICONDUCTOR, INC. | 7360182 | METHOD AND SYSTEM FOR REDUCING DELAY NOISE IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7360183 | DESIGN ANALYSIS TOOL AND METHOD FOR DERIVING CORRESPONDENCE BETWEEN STORAGE ELEMENTS OF TWO MEMORY MODELS |
| FREESCALE SEMICONDUCTOR, INC. | 7361543 | METHOD OF FORMING A NANOCLUSTER CHARGE STORAGE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7361551 | METHOD FOR MAKING AN INTEGRATED CIRCUIT HAVING AN EMBEDDED NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 7361561 | A METHOD OF MAKING A METAL GATE SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7361567 | NON-VOLATILE NANOCRYSTAL MEMORY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7361985 | THERMALLY ENHANCED MOLDED PACKAGE FOR SEMICONDUCTORS |
| FREESCALE SEMICONDUCTOR, INC. | 7361987 | CIRCUIT DEVICE WITH AT LEAST PARTIAL PACKAGING AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 7362134 | CIRCUIT AND METHOD FOR LATCH BYPASS |
| FREESCALE SEMICONDUCTOR, INC. | 7362190 | OSCILLATOR CIRCUIT WITH HIGH PASS FILTER AND LOW PASS FILTER IN OUTPUT STAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7362645 | INTEGRATED CIRCUIT FUSES HAVING CORRESPONDING STORAGE CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | 7362840 | CIRCUIT AND METHOD FOR ADJUSTING TIMING ALIGNMENT USING PROGRAMMABLE CODES |
| FREESCALE SEMICONDUCTOR, INC. | 7363208 | POWER CONSUMPTION ESTIMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7364953 | MANUFACTURING METHOD TO CONSTRUCT SEMICONDUCTOR-ON- INSULATOR WITH CONDUCTOR LAYER SANDWICHED BETWEEN BURIED DIELECTRIC LAYER AND SEMICONDUCTOR LAYERS |
| FREESCALE SEMICONDUCTOR, INC. | 7364969 | SEMICONDUCTOR FABRICATION PROCESS FOR INTEGRATING FORMATION OF EMBEDDED NONVOLATILE STORAGE DEVICE WITH FORMATION OF MULTIPL TRANSISTOR DEVICE TYPES |
| FREESCALE SEMICONDUCTOR, INC. | 7364970 | A METHOD OF MAKING A MULTI-BIT NON-VOLATILE MEMORY (NVM) CELL AND STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7365410 | SEMICONDUCTOR STRUCTURE HAVING A METALLIC BUFFER LAYER AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 7365584 | SLEW-RATE CONTROL APPARATUS AND METHODS FOR A POWER TRANSISTO TO REDUCE VOLTAGE TRANSIENTS DURING INDUCTIVE FLYBACK |
| FREESCALE SEMICONDUCTOR, INC. | 7365587 | CONTENTION-FREE KEEPER CIRCUIT AND A METHOD FOR CONTENTION ELIMINATION |
| FREESCALE SEMICONDUCTOR, INC. | 7368668 | GROUND SHIELDS FOR SEMICONDUCTORS |
| FREESCALE SEMICONDUCTOR, INC. | 7368786 | PROCESS INSENSITIVE ESD PROTECTION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7369086 | MINIATURE VERTICALLY POLARIZED MULTIPLE FREQUENCY BAND ANTENN AND METHOD OF PROVIDING AN ANTENNA FOR A WIRELESS DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7369450 | NONVOLATILE MEMORY HAVING LATCHING SENSE AMPLIFIER AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7369452 | PROGRAMMABLE CELL |
| FREESCALE SEMICONDUCTOR, INC. | 7369974 | POLYNOMIAL GENERATION METHOD FOR CIRCUIT MODELING |
| FREESCALE SEMICONDUCTOR, INC. | 7370332 | ARRANGEMENT AND METHOD FOR ITERATIVE DECODING |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7371626 | METHOD AND APPARATUS FOR MAINTAINING TOPOGRAPHICAL UNIFORMITY OF A SEMICONDUCTOR MEMORY ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | 7371677 | LATERALLY GROWN NANOTUBES AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7372342 | OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | 7373539 | PARALLEL PATH ALIGNMENT METHOD AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 7374971 | SEMICONDUCTOR DIE EDGE RECONDITIONING |
| FREESCALE SEMICONDUCTOR, INC. | 7375002 | MIM CAPACITOR IN A SEMICONDUCTOR DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7376177 | CIRCUIT AND METHOD FOR RAKE TRAINING DURING ACQUISITION |
| FREESCALE SEMICONDUCTOR, INC. | 7376207 | APPARATUS FOR RECEIVING AND RECOVERING FREQUENCY SHIFT KEYED SYMBOLS |
| FREESCALE SEMICONDUCTOR, INC. | 7376568 | VOICE SIGNAL PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 7376777 | PERFORMING AN N-BIT WRITE ACCESS TO AN MXN-BIT-ONLY PERIPHERAL |
| FREESCALE SEMICONDUCTOR, INC. | 7378197 | METHOD OF PATTERNING PHOTORESIST ON A WAFER USING A REFLECTIVE MASK WITH A MULTI-LAYER ARC |
| FREESCALE SEMICONDUCTOR, INC. | 7378298 | METHOD OF MAKING STACKED DIE PACAKGE |
| FREESCALE SEMICONDUCTOR, INC. | 7378306 | SELECTIVE SILICON DEPOSITION FOR PLANARIZED DUAL SURFACE ORIENTATION INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | 7378314 | SOURCE SIDE INJECTION STORAGE DEVICE WITH CONTROL GATES ADJACENT TO SHARED SOURCE/DRAIN AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7378317 | SUPERJUNCTION POWER MOSFET |
| FREESCALE SEMICONDUCTOR, INC. | 7378339 | BARRIER FOR USE IN 3-D INTEGRATION OF CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 7378920 | METHODS AND APPARATUS FOR A HIGH-FREQUENCY OUTPUT MATCH CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7378993 | METHOD AND SYSTEM FOR TRANSMITTING DATA |
| FREESCALE SEMICONDUCTOR, INC. | 7379002 | METHODS AND APPARATUS FOR A MULTI-MODE ANALOG-TO-DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 7382158 | LEVEL SHIFTER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7383393 | SYSTEM AND METHOD FOR COOPERATIVE PREFETCHING |
| FREESCALE SEMICONDUCTOR, INC. | 7384819 | METHOD OF FORMING STACKABLE PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7385307 | DRIVE ARRANGEMENT FOR ACTIVATING A CAR SAFETY DEVICE ACTIVATION ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 7385451 | ARRANGEMENT, PHASE LOCKED LOOP AND METHOD FOR NOISE SHAPING IN A PHASE-LOCKED LOOP |
| FREESCALE SEMICONDUCTOR, INC. | 7386821 | PRIMITIVE CELL METHOD FOR FRONT END PHYSICAL DESIGN |
| FREESCALE SEMICONDUCTOR, INC. | 7387946 | METHOD OF FABRICATING A SUBSTRATE FOR A PLANAR, DOUBLE GATED, TRANSISTOR PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 7388419 | PVT VARIATION DETECTION AND COMPENSATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7388422 | CHARGE PUMP CIRCUIT FOR HIGH SIDE DRIVE CIRCUIT AND DRIVER DRIVING VOLTAGE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7388954 | METHOD AND APPARATUS FOR TONE INDICATION |
| FREESCALE SEMICONDUCTOR, INC. | 7391278 | OSCILLATOR WITH STACKED AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 7391659 | METHOD FOR MULTIPLE STEP PROGRAMMING A MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | 7393752 | SEMICONDUCTOR DEVICES AND METHOD OF FABRICATION |
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| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7394299 | DIGITAL CLOCK FREQUENCY MULTIPLIER |
| FREESCALE SEMICONDUCTOR, INC. | 7394686 | PROGRAMMABLE STRUCTURE INCLUDING DISCONTINUOUS STORAGE ELEMENTS AND SPACER CONTROL GATES IN A TRENCH |
| FREESCALE SEMICONDUCTOR, INC. | 7394866 | ULTRA WIDEBAND COMMUNICATION SYSTEM, METHOD, AND DEVICE WITH LOW NOISE PULSE FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7397001 | MULTI-STRAND SUBSTRATE FOR BALL-GRID ARRAY ASSEMBLIES AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7397291 | CLOCK JITTER MINIMIZATION IN A CONTINUOUS TIME SIGMA DELTA ANALOG-TO-DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 7397297 | LEVEL SHIFTER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7397703 | NON-VOLATILE MEMORY WITH CONTROLLED PROGRAM/ERASE |
| FREESCALE SEMICONDUCTOR, INC. | 7397722 | MULTIPLE BLOCK MEMORY WITH COMPLEMENTARY DATA PATH |
| FREESCALE SEMICONDUCTOR, INC. | 7399675 | ELECTRONIC DEVICE INCLUDING AN ARRAY AND PROCESS FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7400172 | MILLER CAPACITANCE TOLERANT BUFFER ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 7400669 | LEAKAGE NULLING RECEIVER CORRELATOR STRUCTURE AND METHOD FOR ULTRA WIDE BANDWIDTH COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7401201 | PROCESSOR AND METHOD FOR ALTERING ADDRESS TRANSLATION |
| FREESCALE SEMICONDUCTOR, INC. | 7401234 | AUTONOMOUS MEMORY CHECKER FOR RUNTIME SECURITY ASSURANCE AND METHOD THEREFORE |
| FREESCALE SEMICONDUCTOR, INC. | 7402476 | METHOD FOR FORMING AN ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7402477 | METHOD OF MAKING A MULTIPLE CRYSTAL ORIENTATION SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7403071 | HIGH LINEARITY AND LOW NOISE AMPLIFIER WITH CONTINUOUSLY VARIABLE GAIN CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 7403410 | SWITCH DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7403966 | HARDWARE FOR PERFORMING AN ARITHMETIC FUNCTION |
| FREESCALE SEMICONDUCTOR, INC. | 7404019 | METHOD AND APPARATUS FOR ENDIANNESS CONTROL IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7404139 | DECODER WITH M-AT-A-TIME TRACEBACK |
| FREESCALE SEMICONDUCTOR, INC. | 7405099 | WIDE AND NARROW TRENCH FORMATION IN HIGH ASPECT RATIO MEMS |
| FREESCALE SEMICONDUCTOR, INC. | 7405102 | METHODS AND APPARATUS FOR THERMAL MANAGEMENT IN A MULTI-LAYER EMBEDDED CHIP STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7405128 | DOTTED CHANNEL MOSFET AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7408973 | ULTRA WIDE BANDWIDTH SPREAD-SPECTRUM COMMUNICATIONS SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7409198 | WIDEBAND VARIABLE GAIN AMPLIFIER IN AN ULTRA WIDEBAND RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 7409502 | SELECTIVE CACHE LINE ALLOCATION INSTRUCTION EXECUTION AND CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | 7409654 | METHOD AND APPARATUS FOR PERFORMING TEST PATTERN AUTOGRADING |
| FREESCALE SEMICONDUCTOR, INC. | 7409738 | SYSTEM AND METHOD FOR PREDICTING ROTATIONAL IMBALANCE |
| FREESCALE SEMICONDUCTOR, INC. | 7410544 | METHOD FOR CLEANING ELECTROLESS PROCESS TANK |
| FREESCALE SEMICONDUCTOR, INC. | 7410876 | METHODOLOGY TO REDUCE SOI FLOATING-BODY EFFECT |
| FREESCALE SEMICONDUCTOR, INC. | 7411270 | COMPOSITE CAPACITOR AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7411466 | COIL-LESS OVERTONE CRYSTAL OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | 7411467 | OVERTONE CRYSTAL OSCILLATOR AUTOMATIC CALIBRATION SYSTEM |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7413970 | ELECTRONIC DEVICE INCLUDING A SEMICONDUCTOR FIN AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7414316 | METHODS AND APPARATUS FOR THERMAL ISOLATION IN VERTICALLY-INTEGRATED SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7414384 | SERIES REGULATOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7414439 | RECEIVER FOR A SWITCHED SIGNAL ON A COMMUNICATION LINE |
| FREESCALE SEMICONDUCTOR, INC. | 7414449 | DYNAMIC SCANNABLE LATCH AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7414462 | DIFFERENTIAL RECEIVER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7414877 | ELECTRONIC DEVICE INCLUDING A STATIC-RANDOM-ACCESS MEMORY CELL AND A PROCESS OF FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7415493 | ASYNCHRONOUS SAMPLING RATE CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | 7415558 | COMMUNICATION STEERING FOR USE IN A MULTI-MASTER SHARED RESOURCE SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7416605 | ANNEAL OF EPITAXIAL LAYER IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7416945 | METHOD FOR FORMING A SPLIT GATE MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7418251 | COMPACT RADIO FREQUENCY HARMONIC FILTER USING INTEGRATED PASSIVE DEVICE TECHNOLOGY |
| FREESCALE SEMICONDUCTOR, INC. | 7418675 | SYSTEM AND METHOD FOR REDUCING THE POWER CONSUMPTION OF CLOCK SYSTEMS $$ |
| FREESCALE SEMICONDUCTOR, INC. | 7419866 | ELECTRONIC DEVICE INCLUDING SEMICONDUCTOR ISLANDS OF DIFFERENT THICKNESSES OVER AN INSULATING LAYER AND A PROCESS OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7420202 | ELECTRONIC DEVICE INCLUDING A TRANSISTOR STRUCTURE HAVING AN ACTIVE REGION ADJACENT TO A STRESSOR LAYER AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7420296 | POWER SUPPLY CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7420394 | LATCHING INPUT BUFFER CIRCUIT WITH VARIABLE HYSTERESIS |
| FREESCALE SEMICONDUCTOR, INC. | 7420401 | LOW PIN COUNT RESET CONFIGURATION |
| FREESCALE SEMICONDUCTOR, INC. | 7420426 | FREQUENCY MODULATED OUTPUT CLOCK FROM A DIGITAL PHASE LOCKED LOOP |
| FREESCALE SEMICONDUCTOR, INC. | 7421610 | CLOCK GENERATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7422973 | METHOD FOR FORMING MULTI-LAYER BUMPS ON A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 7422979 | METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING A DIFFUSION BARRIER STACK AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7423416 | VOLTAGE REGULATOR AND METHOD FOR PROVIDING A REGULATED OUTPUT |
| FREESCALE SEMICONDUCTOR, INC. | 7425464 | SEMICONDUCTOR DEVICE PACKAGING |
| FREESCALE SEMICONDUCTOR, INC. | 7425485 | MICROELECTRONIC ASSEMBLY AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7427549 | METHOD OF SEPARATING STRUCTURE IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7428172 | CONCURRENT PROGRAMMING AND PROGRAM VERIFICATION OF FLOATING GATE TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 7429506 | PROCESS OF MAKING A III-V COMPOUND SEMICONDUCTOR HETEROSTRUCTURE MOSFET |
| FREESCALE SEMICONDUCTOR, INC. | 7429790 | SEMICONDUCTOR STRUCTURE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7430151 | MEMORY WITH CLOCKED SENSE AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 7430642 | SYSTEM AND METHOD FOR UNIFIED CACHE ACCESS USING SEQUENTIAL |

INSTRUCTION INFORMATION

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7432024 | LITHOGRAPHIC TEMPLATE AND METHOD OF FORMATION AND USE |
| FREESCALE SEMICONDUCTOR, INC. | 7432122 | ELECTRONIC DEVICE AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7432130 | METHOD OF PACKAGING SEMICONDUCTOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | 7432133 | PLASTIC PACKAGED DEVICE WITH DIE INTERFACE LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7432145 | POWER SEMICONDUCTOR DEVICE WITH A BASE REGION AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7432158 | METHOD FOR RETAINING NANOCLUSTER SIZE AND ELECTRICAL CHARACTERISTICS DURING PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 7432164 | SEMICONDUCTOR DEVICE COMPRISING A TRANSISTOR HAVING A COUNTER-DOPED CHANNEL REGION AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7432547 | NON-VOLATILE MEMORY DEVICE WITH IMPROVED DATA RETENTION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7432565 | III-V COMPOUND SEMICONDUCTOR HETEROSTRUCTURE MOSFET DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7432693 | LOW DROP-OUT DC VOLTAGE REGULATOR |
| FREESCALE SEMICONDUCTOR, INC. | 7432725 | ELECTRICAL FIELD SENSORS |
| FREESCALE SEMICONDUCTOR, INC. | 7432729 | METHODS OF TESTING ELECTRONIC DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7432748 | SEQUENCE-INDEPENDENT POWER-ON RESET FOR MULTIVOLTAGE CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 7432754 | VOLTAGE CONTROL CIRCUIT HAVING A POWER SWITCH |
| FREESCALE SEMICONDUCTOR, INC. | 7432778 | ARRANGEMENT AND METHOD FOR IMPEDANCE MATCHING |
| FREESCALE SEMICONDUCTOR, INC. | 7432792 | HIGH FRQUENCY THIN FILM ELECTRICAL CIRCUIT ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 7432838 | METHOD AND APPARATUS FOR REDUCED POWER CONSUMPTION ADC CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | 7434009 | APPARATUS AND METHOD FOR PROVIDING INFORMATION TO A CACHE MODULE USING FETCH BURSTS |
| FREESCALE SEMICONDUCTOR, INC. | 7434039 | COMPUTER PROCESSOR CAPABLE OF RESPONDING WITH A COMPARABLE EFFICIENCY TO BOTH SOFTWARE-STATE-INDEPENDENT AND STATE-DEPENDENT EVENTS |
| FREESCALE SEMICONDUCTOR, INC. | 7434108 | MASKING WITHIN A DATA PROCESSING SYSTEM HAVING APPLICABILITY FOR A DEVELOPMENT INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | 7434148 | TRACK BUFFER IN A PARALLEL DECODER |
| FREESCALE SEMICONDUCTOR, INC. | 7434264 | DATA PROCESSING SYSTEM WITH PERIPHERAL ACCESS PROTECTION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7434464 | METHODS AND APPARATUS FOR A MEMS GYRO SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | 7435625 | SEMICONDUCTOR DEVICE WITH REDUCED PACKAGE CROSS-TALK AND LOSS |
| FREESCALE SEMICONDUCTOR, INC. | 7435639 | DUAL SURFACE SOI BY LATERAL EPITAXIAL OVERGROWTH |
| FREESCALE SEMICONDUCTOR, INC. | 7435646 | METHOD FOR FORMING FLOATING GATES WITHIN NVM PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 7436025 | TERMINATION STRUCTURES FOR SUPER JUNCTION DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7437698 | METHOD AND PROGRAM PRODUCT FOR PROTECTING INFORMATION IN EDA TOOL DESIGN VIEWS |
| FREESCALE SEMICONDUCTOR, INC. | 7437951 | FLOWMETER AND METHOD FOR THE MAKING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7439105 | METAL GATE WITH ZIRCONIUM |
| FREESCALE SEMICONDUCTOR, INC. | 7439134 | METHOD FOR PROCESS INTEGRATION OF NON-VOLATILE MEMORY CELL |

TRANSISTORS WITH TRANSISTORS OF ANOTHER TYPE

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7439584 | STRUCTURE AND METHOD FOR RESURF LDMOSFET WITH A CURRENT DIVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 7439606 | METHOD OF MANUFACTURING A PASSIVE INTEGRATED MATCHING NETWORK FOR POWER AMPLIFIERS |
| FREESCALE SEMICONDUCTOR, INC. | 7439718 | APPARATUS AND METHOD FOR HIGH SPEED VOLTAGE REGULATION |
| FREESCALE SEMICONDUCTOR, INC. | 7439787 | METHODS AND APPARATUS FOR A DIGITAL PULSE WITDH MODULATOR USING MULTIPLE DELAY LOCKED LOOPS |
| FREESCALE SEMICONDUCTOR, INC. | 7439791 | TEMPERATURE COMPENSATION DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7440313 | TWO-PORT SRAM HAVING IMPROVED WRITE OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7440335 | CONTENTION-FREE HIERARCHICAL BIT LINE IN EMBEDDED MEMORY AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7440354 | MEMORY WITH LEVEL SHIFTING WORD LINE DRIVER AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7440731 | POWER AMPLIFIER WITH VSWR DETECTION AND CORRECTION FEATURE |
| FREESCALE SEMICONDUCTOR, INC. | 7440737 | NOISE BLANKER CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 7441102 | INTEGRATED CIRCUIT WITH FUNCTIONAL STATE CONFIGURABLE MEMORY AND METHOD OF CONFIGURING FUNCTIONAL STATES OF THE INTEGRATED CIRCUIT MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 7441262 | INTEGRATED VPN/FIREWALL SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7442581 | FLEXIBLE CARRIER AND RELEASE METHOD FOR HIGH VOLUME ELECTRONIC PACKAGE FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 7442590 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING A FIN AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7442591 | METHOD OF MAKING A MULTI-GATE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7442598 | METHOD OF FORMING AN INTERLAYER DIELECTRIC |
| FREESCALE SEMICONDUCTOR, INC. | 7442616 | METHOD OF MANUFACTURING A BIPOLAR TRANSISTOR AND BIPOLAR TRANSISTOR THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7442621 | SEMICONDUCTOR PROCESS FOR FORMING STRESS ABSORBENT SHALLOW TRENCH ISOLATIONS STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | 7442654 | METHOD OF FORMING AN OXIDE LAYER ON A COMPOUND SEMICONDUCTOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7443174 | ELECTRICAL FIELD RECIPROCAL DISPLACEMENT SENSORS |
| FREESCALE SEMICONDUCTOR, INC. | 7443223 | LEVEL SHIFTING CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7443256 | OSCILLATOR CIRCUIT WITH A VOLTAGE RESTRICTION BLOCK |
| FREESCALE SEMICONDUCTOR, INC. | 7443323 | CALIBRATING A DIGITAL-TO-ANALOG CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 7443325 | SIGMA-DELTA MODULATOR |
| FREESCALE SEMICONDUCTOR, INC. | 7443333 | SINGLE STAGE CYCLIC ANALOG TO DIGITAL CONVERTER WITH VARIABLE RESOLUTION |
| FREESCALE SEMICONDUCTOR, INC. | 7443745 | BYTE WRITEABLE MEMORY WITH BIT-COLUMN VOLTAGE SELECTION AND COLUMN REDUNDANCY |
| FREESCALE SEMICONDUCTOR, INC. | 7444012 | METHOD AND APPARATUS FOR PERFORMING FAILURE ANALYSIS WITH FLUORESCENCE INKS |
| FREESCALE SEMICONDUCTOR, INC. | 7444443 | METHOD OF REPEATING DATA TRANSMISSION BETWEEN NETWORK DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7444556 | SYSTEM AND METHOD OF INTERLEAVING TRANSMITTED DATA |
| FREESCALE SEMICONDUCTOR, INC. | 7444557 | MEMORY WITH FAULT TOLERANT REFERENCE CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | 7444568 | METHOD AND APPARATUS FOR TESTING A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7445967 | METHOD OF PACKAGING A SEMICONDUCTOR DIE AND PACKAGE THEREOF |

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7445976 | METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING AN INTERLAYER AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7445981 | METHOD FOR FORMING A DUAL METAL GATE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7445984 | METHOD FOR REMOVING NANOCLUSTERS FROM SELECTED REGIONS |
| FREESCALE SEMICONDUCTOR, INC. | 7446001 | METHOD FOR FORMING A SEMICONDUCTOR-ON-INSULATOR (SOI) BODY-CONTACTED DEVICE WITH A PORTION OF DRAIN REGION REMOVED |
| FREESCALE SEMICONDUCTOR, INC. | 7446006 | SEMICONDUCTOR FABRICATION PROCESS INCLUDING SILICIDE STRINGER REMOVAL PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 7446017 | METHODS AND APPARATUS FOR RF SHIELDING IN VERTICALLY-INTEGRATED SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7446026 | METHOD OF FORMING A SEMICONDUCTOR DEVICE WITH STRESSOR SOURCE/DRAIN REGIONS |
| FREESCALE SEMICONDUCTOR, INC. | 7446411 | SEMICONDUCTOR STRUCTURE AND METHOD OF ASSEMBLY |
| FREESCALE SEMICONDUCTOR, INC. | 7446566 | LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | 7446592 | PVT VARIATION DETECTION AND COMPENSATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7446990 | I/O CELL ESD SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7447272 | FILTER METHOD AND APPARATUS FOR POLAR MODULATION |
| FREESCALE SEMICONDUCTOR, INC. | 7447279 | METHOD AND SYSTEM FOR INDICATING ZERO-CROSSINGS OF A SIGNAL IN THE PRESENCE OF NOISE |
| FREESCALE SEMICONDUCTOR, INC. | 7447284 | METHOD AND APPARATUS FOR SIGNAL NOISE CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 7447503 | METHOD OF DESIGNATING A FUTURE NETWORK COORDINATOR |
| FREESCALE SEMICONDUCTOR, INC. | 7447867 | NON-INTRUSIVE ADDRESS MAPPING HAVING A MODIFIED ADDRESS SPACE IDENTIFIER AND CIRCUITRY THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7447886 | SYSTEM FOR EXPANDED INSTRUCTION ENCODING AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7449923 | AMPLIFIER CIRCUIT FOR DOUBLE SAMPLED ARCHITECTURES |
| FREESCALE SEMICONDUCTOR, INC. | 7450454 | LOW VOLTAGE DATA PATH IN MEMORY ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | 7450558 | METHOD FOR CONTROLLING OPERATION OF A CHILD OR NEIGHBOR NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 7450634 | DECISION FEED FORWARD EQUALIZER SYSTEM AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7450665 | METHOD AND APPARATUS TO IMPLEMENT DC OFFSET CORRECTION IN A SIGMA DELTA CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | | CAPACITOR ATTACHMENT METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7452768 | MULTIPLE DEVICE TYPES INCLUDING AN INVERTED-T CHANNEL TRANSISTOR AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7456055 | ELECTRONIC DEVICE INCLUDING A SEMICONDUCTOR FIN AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7456465 | SPLIT GATE MEMORY CELL AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7456679 | REFERENCE CIRCUIT AND METHOD FOR GENERATING A REFERENCE SIGNAL FROM A REFERENCE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7456798 | STACKED LOOP ANTENNA |
| FREESCALE SEMICONDUCTOR, INC. | 7457726 | SYSTEM AND METHOD FOR SELECTIVELY OBTAINING PROCESSOR DIAGNOSTIC DATA |
| FREESCALE SEMICONDUCTOR, INC. | 7457892 | DATA COMMUNICATION FLOW CONTROL DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7458008 | DECISION VOTING IN A PARALLEL DECODER |
| FREESCALE SEMICONDUCTOR, INC. | 7459744 | HOT CARRIER INJECTION PROGRAMMABLE STRUCTURE INCLUDING DISCONTINUOUS STORAGE ELEMENTS AND SPACER CONTROL GATES IN A TRENCH AND A METHOD OF USING THE SAME |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7466006 | STRUCTURE AND METHOD FOR RESURF DIODES WITH A CURRENT DIVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 7466146 | FROZEN MATERIAL DETECTION USING ELECTRIC FIELD SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | 7468313 | ENGINEERING STRAIN IN THICK STRAINED-SOI SUBSTRATES |
| FREESCALE SEMICONDUCTOR, INC. | 7470624 | INTEGRATED ASSIST FEATURES FOR EPITAXIAL GROWTH BULK/SOI HYBRID TILES WITH COMPENSATION |
| FREESCALE SEMICONDUCTOR, INC. | 7470951 | HYBRID-FET AND ITS APPLICATION AS SRAM |
| FREESCALE SEMICONDUCTOR, INC. | 7471560 | ELECTRONIC DEVICE INCLUDING A MEMORY ARRAY AND CONDUCTIVE LINES |
| FREESCALE SEMICONDUCTOR, INC. | 7471582 | MEMORY CIRCUIT USING A REFERENCE FOR SENSING |
| FREESCALE SEMICONDUCTOR, INC. | 7473586 | METHOD OF FORMING FLIP-CHIP BUMP CARRIER TYPE PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7474585 | MEMORY WITH SERIAL INPUT/OUTPUT TERMINALS FOR ADDRESS AND DATA AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7476563 | METHOD OF PACKAGING A DEVICE USING A DIELECTRIC LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7476593 | SEMICONDUCTOR DEVICE AND METHOD OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7477082 | METHOD AND CIRCUIT FOR DRIVING H-BRIDGE THAT REDUCES SWITCHING NOISE |
| FREESCALE SEMICONDUCTOR, INC. | 7479407 | DIGITAL AND RF SYSTEM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7479422 | SEMICONDUCTOR DEVICE WITH STRESSORS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7479429 | SPLIT GATE MEMORY CELL METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7479465 | TRANSFER OF STRESS TO A LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7479785 | CONTROL AND TESTING OF A MICRO ELECTROMECHANICAL SWITCH |
| FREESCALE SEMICONDUCTOR, INC. | 7479813 | LOW VOLTAGE CIRCUIT WITH VARIABLE SUBSTRATE BIAS |
| FREESCALE SEMICONDUCTOR, INC. | 7479824 | A DUAL MODE VOLTAGE SUPPLY CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7480837 | METHOD OF MONITORING TIMEOUT CONDITIONS AND DEVICE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7482679 | LEADFRAME FOR A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7482781 | POWER SUPPLY APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 7482880 | FREQUENCY MODULATED OUTPUT CLOCK FROM A DIGITAL FREQUENCY/PHASE LOCKED LOOP |
| FREESCALE SEMICONDUCTOR, INC. | 7483327 | APPARATUS AND METHOD FOR ADJUSTING AN OPERATING PARAMETER OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7484140 | MEMORY HAVING VARIABLE REFRESH CONTROL AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7484147 | SEMICONDUCTOR INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7486129 | LOW POWER VOLTAGE REFERENCE |
| FREESCALE SEMICONDUCTOR, INC. | 7486535 | METHOD AND DEVICE FOR PROGRAMMING ANTI-FUSES |
| FREESCALE SEMICONDUCTOR, INC. | 7487661 | SENSOR HAVING FREE FALL SELF-TEST CAPABILITY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7488635 | SEMICONDUCTOR STRUCTURE WITH REDUCED GATE DOPING AND METHODS FOR FORMING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7489026 | METHODS AND APPARATUS FOR A QUAD FLAT NO-LEAD (QFN) PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7489540 | BITCELL WITH VARIABLE-CONDUCTANCE TRANSFER GATE AND METHOD |

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| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7489723 | SYSTEM AND METHOD FOR ADJUSTING ACQUISITION PHASE |
| FREESCALE SEMICONDUCTOR, INC. | 7491594 | METHODS OF GENERATING PLANAR DOUBLE GATE TRANSISTOR SHAPES AND DATA PROCESSING SYSTEM READABLE MEDIA TO PERFORM THE METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 7491600 | NANOCRYSTAL BITCELL PROCESS INTEGRATION FOR HIGH DENSITY APPLICATION |
| FREESCALE SEMICONDUCTOR, INC. | 7491622 | PROCESS OF FORMING AN ELECTRONIC DEVICE INCLUDING A LAYER FORMED USING AN INDUCTIVELY COUPLED PLASMA |
| FREESCALE SEMICONDUCTOR, INC. | 7491630 | UNDOPED GATE POLY INTEGRATION FOR IMPROVED GATE PATTERNING AND COBALT SILICIDE EXTENDIBILITY |
| FREESCALE SEMICONDUCTOR, INC. | 7492627 | MEMORY WITH INCREASED WRITE MARGIN BITCELLS |
| FREESCALE SEMICONDUCTOR, INC. | 7492789 | METHOD AND SYSTEM FOR DYNAMIC PACKET AGGREGATION IN A WIRELESS NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 7493179 | DIGITAL AUDIO SYSTEM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7494825 | TOP CONTACT ALIGNMENT IN SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7494832 | SEMICONDUCTOR OPTICAL DEVICES AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 7494856 | SEMICONDUCTOR FABRICATION PROCESS USING ETCH STOP LAYER TO OPTIMIZE FORMATION OF SOURCE/DRAIN STRESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 7494924 | METHOD FOR FORMING REINFORCED INTERCONNECTS ON A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 7495465 | PVT VARIATION DETECTION AND COMPENSATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7495493 | CIRCUITRY FOR LATCHING |
| FREESCALE SEMICONDUCTOR, INC. | 7495939 | RIPPLE FILTER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7495987 | CURRENT-MODE MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | 7497763 | POLISHING PAD, A POLISHING APPARATUS, AND A PROCESS FOR USING THE POLISHING PAD |
| FREESCALE SEMICONDUCTOR, INC. | 7498848 | SYSTEM AND METHOD FOR MONITORING CLOCK SIGNAL IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7498864 | ELECTRONIC FUSE FOR OVERCURRENT PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 7499342 | DYNAMIC MODULE OUTPUT DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7499442 | METHOD FOR SHARING BANDWIDTH USING REDUCED DUTY CYCLE SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 7500033 | UNIVERSAL SERIAL BUS TRANSMITTER |
| FREESCALE SEMICONDUCTOR, INC. | 7500152 | APPARATUS AND METHOD FOR TIME ORDERING EVENTS IN A SYSTEM HAVING MULTIPLE TIME DOMAINS |
| FREESCALE SEMICONDUCTOR, INC. | 7501876 | LEVEL SHIFTER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7502410 | METHOD AND SYSTEM FOR CONTROLLING A NOTCHING MECHANISM |
| FREESCALE SEMICONDUCTOR, INC. | 7504289 | ELECTRONIC DEVICE INCLUDING TRANSISTOR STRUCTURES WITH SIDEWALL SPACERS AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7504302 | NON-VOLATILE MEMORY CELL INCLUDING A CAPACITOR STRUCTURE AND PROCESSES FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7504677 | MULTI-GATE ENHANCEMENT MODE RF SWITCH AND BIAS ARRANGEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 7505538 | ULTRA WIDEBAND COMMUNICATION SYSTEM, METHOD, AND DEVICE WITH LOW NOISE RECEPTION |
| FREESCALE SEMICONDUCTOR, INC. | 7505748 | LINEAR VOLTAGE CONTROLLED VARIABLE ATTENUATOR WITH LINEAR DB/V GAIN SLOPE |
| FREESCALE SEMICONDUCTOR, INC. | 7506105 | PREFETCHING USING HASHED PROGRAM COUNTER |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7506438 | LOW PROFILE INTEGRATED MODULE INTERCONNECTS AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 7507638 | ULTRA-THIN DIE AND METHOD OF FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7508021 | RF POWER TRANSISTOR DEVICE WITH HIGH PERFORMANCE SHUNT CAPACITOR AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7508177 | METHOD AND CIRCUIT FOR REDUCING REGULATOR OUTPUT NOISE |
| FREESCALE SEMICONDUCTOR, INC. | 7508246 | PERFORMANCE VARIATION COMPENSATING CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7508260 | BYPASSABLE LOW NOISE AMPLIFIER TOPOLOGY WITH MULTI-TAP TRANSFORMER |
| FREESCALE SEMICONDUCTOR, INC. | 7508865 | SYSTEM AND METHOD FOR TRACKING AN ULTRAWIDE BANDWIDTH SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 7508896 | CIRCUIT AND METHOD FOR DYNAMICALLY ADJUSTING A FILTER BANDWIDTH |
| FREESCALE SEMICONDUCTOR, INC. | 7510922 | SPACER T-GATE STRUCTURE FOR CoSi2 EXTENDIBILITY |
| FREESCALE SEMICONDUCTOR, INC. | 7510938 | SEMICONDUCTOR SUPERJUNCTION STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7510956 | MOS DEVICE WITH MULTI-LAYER GATE STACK |
| FREESCALE SEMICONDUCTOR, INC. | 7511319 | METHOD AND APPARATUS FOR A STEPPED-DRIFT MOSFET |
| FREESCALE SEMICONDUCTOR, INC. | 7511360 | SEMICONDUCTOR DEVICE HAVING STRESSORS AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 7511537 | COMPARATOR CIRCUIT FOR REDUCING CURRENT CONSUMPTION BY SURPRESSING GLITCHES DURING A TRANSISTIONAL PERIOD |
| FREESCALE SEMICONDUCTOR, INC. | 7512171 | SYSTEM AND METHOD FOR CALIBRATING AN ANALOG SIGNAL PATH IN AN ULTRA WIDEBAND RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 7512391 | SELF-ALIGNING RESONATOR FILTER CIRCUIT AND WIDEBAND TUNER CIRCUIT INCORPORATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7512723 | METHODS AND APPARATUS FOR SHARING A PERIPHERAL IN A MULTI-CORE SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7514313 | ELECTRONIC DEVICE AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7514340 | COMPOSITE INTEGRATED DEVICE AND METHODS FOR FORMING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7517741 | SINGLE TRANSISTOR MEMORY CELL WITH REDUCED RECOMBINATION RATES |
| FREESCALE SEMICONDUCTOR, INC. | 7517742 | AREA DIODE FORMATION IN SOI APPLICATION |
| FREESCALE SEMICONDUCTOR, INC. | 7517747 | NANOCRYSTAL NON-VOLATILE MEMORY CELL AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7518177 | SEMICONDUCTOR STORAGE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7518179 | VIRTUAL GROUND MEMORY ARRAY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7518352 | BOOTSTRAP CLAMPING CIRCUIT FOR DC/DC REGULATORS AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7518933 | CIRCUIT FOR USE IN A MULTIPLE BLOCK MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 7518947 | SELF-TIMED MEMORY HAVING COMMON TIMING CONTROL CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7519099 | PSEUDORANDOM NOISE LOCK DETECTOR |
| FREESCALE SEMICONDUCTOR, INC. | 7520170 | OUTPUT CORRECTION CIRCUIT FOR THREE-AXIS ACCELEROMETER |
| FREESCALE SEMICONDUCTOR, INC. | 7520797 | PLATEN ENDPOINT WINDOW WITH PRESSURE RELIEF |
| FREESCALE SEMICONDUCTOR, INC. | 7521314 | METHOD FOR SELECTIVE REMOVAL OF A LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7521317 | METHOD OF FORMING A SEMICONDUCTOR DEVICE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7521720 | SEMICONDUCTOR OPTICAL DEVICES AND METHOD FOR FORMING |

| FREESCALE SEMICONDUCTOR, INC. 7521974 A TRANSITIONAL PHASE LOCKED LOOP USING A QUANTIZE EDGE TIMED SYNTHESIZER FREESCALE SEMICONDUCTOR, INC. 7522667 METHOD AND APPARATUS FOR DYNAMIC DETERMINATION REQUIRED TO BUILD A COMPLETE PICTURE IN A MPEG VID FREESCALE SEMICONDUCTOR, INC. 7523373 MINIMUM MEMORY OPERATING VOLTAGE TECHNIQUE FREESCALE SEMICONDUCTOR, INC. 7524693 METHOD AND APPARATUS FOR FORMING AN ELECTRICAL OF SEMICONDUCTOR SUBSTRATE FREESCALE SEMICONDUCTOR, INC. 7524707 MODIFIED HYBRID ORIENTATION TECHNOLOGY FREESCALE SEMICONDUCTOR, INC. 7524719 SELF-ALIGNED SPLIT GATE MEMORY CELL AND METHOD OF FORMING THE SAME FREESCALE SEMICONDUCTOR, INC. 7524721 ELECTRONIC DEVICE INCLUDING AN INDUCTOR AND A PROPOSED AND METHOD THEREOF FREESCALE SEMICONDUCTOR, INC. 7525152 RF POWER TRANSISTOR DEVICE WITH METAL ELECTROMIC AND METHOD THEREOF FREESCALE SEMICONDUCTOR, INC. 7525866 MEMORY CIRCUIT FREESCALE SEMICONDUCTOR, INC. 7525867 STORAGE CIRCUIT AND METHOD THEREFOR FREESCALE SEMICONDUCTOR, INC. 7527976 PROCESS FOR TESTING A REGION FOR AN ANALYTE AND A FORMING AN ELECTRONIC DEVICE FREESCALE SEMICONDUCTOR, INC. 7527976 PROCESS FOR TESTING A REGION FOR AN ANALYTE AND A FORMING AN ELECTRONIC DEVICE FREESCALE SEMICONDUCTOR, INC. 7528015 TUNABLE ANTIFUSE ELEMENT AND METHOD OF MANUFACTOR AND A METHOD THEREOF FREESCALE SEMICONDUCTOR, INC. 7528029 STRESSOR INTEGRATION AND METHOD THEREOF | ID IMPEDDOL APED |
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| FREESCALE SEMICONDUCTOR, INC. 7528047 SELF-ALIGNED SPLIT GATE MEMORY CELL AND METHOD O | F FORMING |
| FREESCALE SEMICONDUCTOR, INC. 7528062 INTEGRATED MATCHING NETWORK AND METHOD FOR MAINTEGRATED MATCHING NETWORKS | NUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. 7528069 FINE PITCH INTERCONNECT AND METHOD OF MAKING | |
| FREESCALE SEMICONDUCTOR, INC. 7528468 CAPACITOR ASSEMBLY WITH SHEILDED CONNECTIONS AND FORMING THE SAME | D METHOD FOR |
| FREESCALE SEMICONDUCTOR, INC. 7529363 TONE DETECTOR AND METHOD THEREFOR | |
| FREESCALE SEMICONDUCTOR, INC. 7530037 METHODS OF GENERATING PLANAR DOUBLE GATE TRANSI DATA PROCESSING SYSTEM READABLE MEDIA TO PERFORM | |
| FREESCALE SEMICONDUCTOR, INC. 7530039 METHODS AND APPARATUS FOR SIMULATING DISTRIBUTED |) EFFECTS |
| FREESCALE SEMICONDUCTOR, INC. 7531383 ARRAY QUAD FLAT NO-LEAD PACKAGE AND METHOD OF FO | ORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. 7532687 DUAL STAGE AUTOMATIC GAIN CONTROL IN AN ULTRA WIL | DEBAND RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. 7532696 CALIBRATION DEVICE FOR A PHASED LOCKED LOOP SYNTE | HESISER |
| FREESCALE SEMICONDUCTOR, INC. 7534162 GROOVED PLATEN WITH CHANNELS OR PATHWAY TO AMBI | ENT AIR |
| FREESCALE SEMICONDUCTOR, INC. 7534674 METHOD OF MAKING A SEMICONDUCTOR DEVICE WITH A S | STRESSOR |
| FREESCALE SEMICONDUCTOR, INC. 7534693 THIN-FILM CAPACITOR WITH A FIELD MODIFICATION LAYE FOR FORMING THE SAME | R AND METHODS |
| FREESCALE SEMICONDUCTOR, INC. 7534706 RECESSED POLY EXTENSION T-GATE | |
| FREESCALE SEMICONDUCTOR, INC. 7535060 CHARGE STORAGE STRUCTURE FORMATION IN TRANSISTO CHANNEL REGION | R WITH VERTICAL |
| FREESCALE SEMICONDUCTOR, INC. 7535078 SEMICONDUCTOR DEVICE HAVING A FUSE AND METHOD O THEREOF | |
| FREESCALE SEMICONDUCTOR, INC. 7535079 SEMICONDUCTOR DEVICE COMPRISING PASSIVE COMPONE | F FORMING |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7535391 | ANALOG-TO-DIGITAL CONVERTER HAVING RANDOM CAPACITOR ASSIGNMENT AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7538000 | STRUCTURE AND MANUFACTURING METHOD OF MULTI-GATE DIELECTRIC THICKNESSES FOR PLANAR DOUBLE GATE DEVICE HAVING MULTI-THRESHOLD VOLTAGES |
| FREESCALE SEMICONDUCTOR, INC. | 7538002 | SEMICONDUCTOR PROCESS INTEGRATING SOURCE/DRAIN STRESSORS AND INTERLEVEL DIELECTRIC LAYER STRESSORS |
| FREESCALE SEMICONDUCTOR, INC. | 7538559 | SYSTEM AND METHOD FOR REDUCING CURRENT IN A DEVICE DURING TESTING |
| FREESCALE SEMICONDUCTOR, INC. | 7538586 | TRANSMITTER FOR A CONTROLLED- SHAPE SWITCHED SIGNAL ON A COMMUNICATION LINE |
| FREESCALE SEMICONDUCTOR, INC. | 7538799 | SYSTEM AND METHOD FOR FLICKER DETECTION IN DIGITAL IMAGING |
| FREESCALE SEMICONDUCTOR, INC. | 7539277 | BINARY STREAM SWITCHING CONTROLLED MODULUS DIVIDER FOR FRACTIONAL FREQUENCY SYNTHESIS |
| FREESCALE SEMICONDUCTOR, INC. | 7539888 | MESSAGE BUFFER FOR A RECEIVER APPARATUS ON A COMMUNICATIONS BUS |
| FREESCALE SEMICONDUCTOR, INC. | 7539906 | SYSTEM FOR INTEGRATED DATA INTEGRITY VERIFICATION AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7542351 | INTEGRATED CIRCUIT FEATURING A NON-VOLATILE MEMORY WITH CHARGE/DISCHARGE RAMP RATE CONTROL AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7542360 | PROGRAMMABLE BIAS FOR A MEMORY ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | 7542365 | APPARATUS AND METHOD FOR ACCESSING A SYNCHRONOUS SERIAL MEMORY HAVING UNKNOWN ADDRESS BIT FIELD SIZE |
| FREESCALE SEMICONDUCTOR, INC. | 7542369 | INTEGRATED CIRCUIT HAVING A MEMORY WITH LOW VOLTAGE READ/WRITE OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7542412 | SELF-ROUTING, STAR-COUPLER-BASED COMMUNICATION NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 7542567 | METHOD AND APPARATUS FOR PROVIDING SECURITY IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7544548 | TRENCH LINER FOR DSO INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | 7544575 | A DUAL METAL SILICIDE SCHEME USING A DUAL SPACER PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 7544576 | DIFFUSION BARRIER FOR NICKEL SILICIDES IN A SEMICONDUCTOR FABRICATION PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 7544595 | FORMING A SEMICONDUCTOR DEVICE HAVING A METAL ELECTRODE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7544605 | METHOD OF MAKING A CONTACT ON A BACKSIDE OF A DIE |
| FREESCALE SEMICONDUCTOR, INC. | 7544980 | SPLIT GATE MEMORY CELL IN A FINFET |
| FREESCALE SEMICONDUCTOR, INC. | 7544997 | MULTI-LAYER SOURCE/DRAIN STRESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 7545679 | ELECTRICAL ERASABLE PROGRAMMABLE MEMORY TRANSCONDUCTANCE TESTING |
| FREESCALE SEMICONDUCTOR, INC. | 7545702 | MEMORY PIPELINING IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7548093 | SCHEME OF LEVEL SHIFTER CELL |
| FREESCALE SEMICONDUCTOR, INC. | 7548102 | DATA LATCH |
| FREESCALE SEMICONDUCTOR, INC. | 7548552 | METHOD FOR POLLING IN A MEDIUM ACCESS CONTROL PROTOCOL |
| FREESCALE SEMICONDUCTOR, INC. | 7548561 | METHOD OF TRANSMITTING AND RECEIVING DATA |
| FREESCALE SEMICONDUCTOR, INC. | 7550318 | INTERCONNECT FOR IMPROVED DIE TO SUBSTRATE ELECTRICAL COUPLING |
| FREESCALE SEMICONDUCTOR, INC. | 7550348 | SOURCE SIDE INJECTION STORAGE DEVICE WITH SPACER GATES AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7550804 | SEMICONDUCTOR DEVICE AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7553704 | ANTIFUSE ELEMENT AND METHOD OF MANUFACTURE |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7553753 | METHOD OF FORMING CRACK ARREST FEATURES IN EMBEDDED DEVICE BUILD-UP PACKAGE AND PACKAGE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7554185 | FLIP CHIP AND WIRE BOND SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7554391 | AMPLIFIER HAVING A VIRTUAL GROUND AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7554841 | CIRCUIT FOR STORING INFORMATION IN AN INTEGRATED CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7555075 | ADJUSTABLE NOISE SUPPRESSION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7556978 | PIEZOELECTRIC MEMS SWITCHES AND METHODS OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 7556992 | METHOD FOR FORMING VERTICAL STRUCTURES IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7557008 | METHOD OF MAKING A NON-VOLATILE MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7557042 | METHOD FOR MAKING A SEMICONDUCTOR DEVICE WITH REDUCED SPACING |
| FREESCALE SEMICONDUCTOR, INC. | 7558539 | POWER CONTROL FEEDBACK LOOP FOR ADJUSTING A MAGNITUDE OF AN OUTPUT SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 7559041 | METHOD AND APPARATUS FOR DESIGNING SEMICONDUCTOR INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7560318 | ELECTRONIC DEVICE AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7560354 | PROCESS OF FORMING AN ELECTRONIC DEVICE INCLUDING A DOPED SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7560965 | SCANNABLE FLIP-FLOP WITH NON-VOLATILE STORAGE ELEMENT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7560970 | LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | 7561076 | FRONT-END METHOD FOR NICAM ENCODING |
| FREESCALE SEMICONDUCTOR, INC. | 7563662 | ELECTRONIC DEVICES INCLUDING NON-VOLATILE MEMORY AND PROCESSES FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7563681 | DOUBLE-GATED NON-VOLATILE MEMORY AND METHODS FOR FORMING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7563700 | METHOD FOR IMPROVING SELF-ALIGNED SILICIDE EXTENDIBILITY WITH SPACER RECESS USING AN AGGREGATED SPACER RECESS ETCH (ASRE) INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | 7564275 | SWITCHING CIRCUIT AND A METHOD OF DRIVING A LOAD |
| FREESCALE SEMICONDUCTOR, INC. | 7564716 | MEMORY DEVICE WITH RETAINED INDICATOR OF READ REFERENCE LEVEL |
| FREESCALE SEMICONDUCTOR, INC. | 7564738 | DOUBLE-RATE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 7565639 | INTEGRATED ASSIST FEATURES FOR EPITAXIAL GROWTH BULK TILES WITH COMPENSATION |
| FREESCALE SEMICONDUCTOR, INC. | 7566623 | ELECTRONIC DEVICE INCLUDING A SEMICONDUCTOR FIN HAVING A PLURALITY OF GATE ELECTRODES AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7566648 | METHOD OF MAKING SOLDER PAD |
| FREESCALE SEMICONDUCTOR, INC. | 7570627 | METHOD FOR SHARING BANDWIDTH USING REDUCED DUTY CYCLE SIGNALS AND MEDIA ACCESS CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 7570712 | SYSTEM AND METHOD FOR TRANSMITTING ULTRAWIDE BANDWIDTH SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 7571404 | A FAST ON-CHIP DECOUPLING CAPACITANCE BUDGETING METHOD AND DEVICE FOR REDUCED POWER SUPPLY NOISE |
| FREESCALE SEMICONDUCTOR, INC. | 7571406 | CLOCK TREE ADJUSTABLE BUFFER |
| FREESCALE SEMICONDUCTOR, INC. | 7572680 | PACKAGED INTEGRATED CIRCUIT WITH ENHANCED THERMAL DISSIPATION |
| FREESCALE SEMICONDUCTOR, INC. | 7572699 | ELECTRONIC DEVICE INCLUDING FINS AND DISCONTINUOUS STORAGE |

ELEMENTS AND PROCESSES OF FORMING AND USING THE SAME

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7572706 | SOURCE/DRAIN STRESSOR AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7572723 | A MICROPAD FOR BONDING AND A METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7573101 | EMBEDDED SUBSTRATE INTERCONNECT FOR UNDERSIDE CONTACT TO SOURCE AND DRAIN REGIONS |
| FREESCALE SEMICONDUCTOR, INC. | 7573114 | ELECTRONIC DEVICE INCLUDING A GATED DIODE |
| FREESCALE SEMICONDUCTOR, INC. | 7573247 | SERIES REGULATOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7573332 | AMPLIFIER WITH ACTIVE INDUCTOR |
| FREESCALE SEMICONDUCTOR, INC. | 7573416 | ANALOG TO DIGITAL CONVERTER WITH LOW POWER CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 7573762 | ONE TIME PROGRAMMABLE ELEMENT SYSTEM IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7573865 | METHOD OF SYNCHRONIZING A WIRELESS DEVICE USING AN EXTERNAL CLOCK |
| FREESCALE SEMICONDUCTOR, INC. | 7574219 | METHOD AND SYSTEM FOR ENABLING DEVICE FUNCTIONS BASED ON DISTANCE INFORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7574564 | REPLACEMENT POINTER CONTROL FOR SET ASSOCIATIVE CACHE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7574682 | YIELD ANALYSIS AND IMPROVEMENT USING ELECTRICAL SENSITIVITY EXTRACTION |
| FREESCALE SEMICONDUCTOR, INC. | 7575958 | PROGRAMMABLE FUSE WITH SILICON GERMANIUM |
| FREESCALE SEMICONDUCTOR, INC. | 7575968 | INVERSE SLOPE ISOLATION AND DUAL SURFACE ORIENTATION INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | 7575975 | METHOD FOR FORMING A PLANAR AND VERTICAL SEMICONDUCTOR STRUCTURE HAVING A STRAINED SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7576526 | OVERCURRENT DETECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7578190 | SYMMETRICAL DIFFERENTIAL CAPACITIVE SENSOR AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7579219 | SEMICONDUCTOR DEVICE WITH A PROTECTED ACTIVE DIE REGION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7579228 | DISPOSABLE ORGANIC SPACERS |
| FREESCALE SEMICONDUCTOR, INC. | 7579238 | METHOD OF FORMING A MULTI-BIT NONVOLATILE MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7579243 | SPLIT GATE MEMORY CELL METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7579258 | SEMICONDUCTOR INTERCONNECT HAVING ADJACENT RESERVOIR FOR BONDING AND METHOD FOR FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7579279 | METHOD TO PASSIVATE CONDUCTIVE SURFACES DURING SEMICONDUCTOR PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 7579282 | METHOD FOR REMOVING METAL FOOT DURING HIGH-K DIELECTRIC/METAL DATE ETCHING |
| FREESCALE SEMICONDUCTOR, INC. | 7579590 | A METHOD OF MEASURING THIN LAYERS USING SIMS |
| FREESCALE SEMICONDUCTOR, INC. | 7579860 | DIGITAL BANDGAP REFERENCE AND METHOD FOR PRODUCING REFERENCE SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 7579898 | TEMPERATURE SENSOR DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7580001 | ANTENNA STRUCTURE FOR INTEGRATED CIRCUIT DIE USING BOND WIRE |
| FREESCALE SEMICONDUCTOR, INC. | 7580070 | SYSTEM AND METHOD FOR ROLL-OFF CORRECTION IN IMAGE PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 7580288 | MULTI-LEVEL VOLTAGE ADJUSTMENT |
| FREESCALE SEMICONDUCTOR, INC. | 7581151 | METHOD AND APPARATUS FOR AFFECTING A PORTION OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7581202 | METHOD FOR GENERATION, PLACEMENT, AND ROUTING OF TEST |

STRUCTURES IN TEST CHIPS

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7582929 | ELECTRONIC DEVICE INCLUDING DISCONTINUOUS STORAGE ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | 7583088 | SYSTEM AND METHOD FOR REDUCING NOISE IN SENSORS WITH CAPACITIVE PICKUP |
| FREESCALE SEMICONDUCTOR, INC. | 7583121 | FLIP-FLOP HAVING LOGIC STATE RETENTION DURING A POWER DOWN MODE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7583542 | MEMORY WITH CHARGE STORAGE LOCATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 7583554 | INTEGRATED CIRCUIT FUSE ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | 7583945 | AMPLIFIER WITH IMPROVED NOISE PERFORMANCE AND EXTENDED GAIN CONTROL RANGE |
| FREESCALE SEMICONDUCTOR, INC. | 7585735 | ASYMMETRIC SPACERS AND ASYMMETRIC SOURCE/DRAIN EXTENSION LAYERS |
| FREESCALE SEMICONDUCTOR, INC. | 7585744 | METHOD OF FORMING A SEAL FOR A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7586238 | CONTROL AND TESTING OF A MICRO ELECTROMECHANICAL SWITCH HAVING A PIEZO ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 7586367 | CURRENT SENSOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7588951 | METHOD OF PACKAGING A SEMICONDUCTOR DEVICE AND A PREFABRICATED CONNECTOR |
| FREESCALE SEMICONDUCTOR, INC. | 7589370 | RF POWER TRANSISTOR WITH LARGE PERIPHERY METAL-INSULATOR-SILICON SHUNT CAPACITOR |
| FREESCALE SEMICONDUCTOR, INC. | 7589550 | SEMICONDUCTOR DEVICE TEST SYSTEM HAVING REDUCED CURRENT LEAKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7589658 | ANALOG-TO-DIGITAL CONVERTER WITH VARIABLE GAIN AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7589945 | DISTRIBUTED ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT WITH VARYING CLAMP SIZE |
| FREESCALE SEMICONDUCTOR, INC. | 7592224 | PROGRAMMABLE STRUCTURE INCLUDING CONTROL GATE OVERLYING SELECT GATE FORMED IN A TRENCH |
| FREESCALE SEMICONDUCTOR, INC. | 7592230 | TRENCH POWER DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7592248 | SEMICONDUCTOR DEVICE HAVING NANOTUBE STRUCTURES AND METHOD OF FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 7592273 | SEMICONDUCTOR DEVICE WITH HYDROGEN BARRIER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7592673 | ESD PROTECTION CIRCUIT WITH ISOLATED DIODE ELEMENT AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7593202 | ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUIT FOR MULTIPLE POWER DOMAIN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7593422 | METHOD OF OPERATING A MEDIA ACCESS CONTROLLER HAVING PSEUDO- STATIC GUARANTEED TIME SLOTS |
| FREESCALE SEMICONDUCTOR, INC. | 7594423 | KNOCK SIGNAL DETECTION IN AUTOMOTIVE SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 7595226 | METHOD OF PACKAGING AN INTEGRATED CIRCUIT DIE |
| FREESCALE SEMICONDUCTOR, INC. | 7595257 | ELECTRONIC DEVICE INCLUDING A BARRIER LAYER AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7595666 | AMPLIFIER CIRCUIT FOR DOUBLE SAMPLED ARCHITECTURES |
| FREESCALE SEMICONDUCTOR, INC. | 7595699 | LOCK LOOP CIRCUIT AND METHOD HAVING IMPROVED LOCK TIME |
| FREESCALE SEMICONDUCTOR, INC. | 7598517 | SUPERJUNCTION TRENCH DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7598596 | METHODS AND APPARATUS FOR A DUAL-METAL MAGNETIC SHIELD STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7598716 | LOW PASS FILTER LOW DROP-OUT VOLTAGE REGULATOR |
| FREESCALE SEMICONDUCTOR, INC. | 7598784 | SYSTEM AND METHOD FOR CONTROLLING SIGNAL TRANSITIONS |
| FREESCALE SEMICONDUCTOR, INC. | 7598805 | LOAD INSENSITIVE BALANCED POWER AMPLIFIER AND RELATED OPERATING METHOD |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7599236 | IN-CIRCUIT VT DISTRIBUTION BIT COUNTER FOR NON-VOLATILE MEMORY DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7599432 | METHOD AND APPARATUS FOR DYNAMICALLY INSERTING GAIN IN AN ADAPTIVE FILTER SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7599976 | SYSTEM AND METHOD FOR CRYPTOGRAPHIC KEY GENERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7602014 | SUPERJUNCTION POWER MOSFET |
| FREESCALE SEMICONDUCTOR, INC. | 7602168 | VOLTAGE REGULATOR FOR INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 7602233 | A VOLTAGE MULTIPLIER WITH IMPROVED EFFICIENCY |
| FREESCALE SEMICONDUCTOR, INC. | 7603902 | TEMPERATURE COMPENSATION CIRCUIT, TRIMMING CIRCUIT, AND ACCELERATION DETECTOR |
| FREESCALE SEMICONDUCTOR, INC. | 7605652 | LOOP GAIN EQUALIZER FOR RF POWER AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 7608513 | DUAL GATE LDMOS DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7608893 | MULTI-CHANNEL TRANSISTOR STRUCTURE AND METHOD OF MAKING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7608898 | ONE TRANSISTOR DRAM CELL STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7608908 | ROBUST DEEP TRENCH ISOLATION |
| FREESCALE SEMICONDUCTOR, INC. | 7608913 | NOISE ISOLATION BETWEEN CIRCUIT BLOCKS IN AN INTEGRATED CIRCUIT CHIP |
| FREESCALE SEMICONDUCTOR, INC. | 7608942 | POWER MANAGEMENT SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7609541 | MEMORY CELLS WITH LOWER POWER CONSUMPTION DURING A WRITE OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7610466 | DATA PROCESSING SYSTEM USING INDEPENDENT MEMORY AND REGISTER OPERAND SIZE SPECIFIERS AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7610809 | DIFFERENTIAL CAPACITIVE SENSOR AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7611936 | METHOD TO CONTROL UNIFORMITY/COMPOSITION OF METAL ELECTRODES SILICIDES ON TOPOGRAPHY AND DEVICES USING THIS METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7611955 | METHOD OF FORMING A BIPOLAR TRANSISTOR AND SEMICONDUCTOR COMPONENT THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7612577 | SPEEDPATH REPAIR IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7612588 | POWER ON DETECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7612613 | SELF REGULATING BIASING CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7612619 | PHASE DETECTOR DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7613775 | NETWORK MESSAGE FILTERING USING HASHING AND PATTERN MATCHING |
| FREESCALE SEMICONDUCTOR, INC. | 7613981 | SYSTEM AND METHOD FOR REDUCING POWER CONSUMPTION IN A LOW- DENSITY PARITY-CHECK (LDPC) DECODER |
| FREESCALE SEMICONDUCTOR, INC. | 7615806 | METHOD FOR FORMING A SEMICONDUCTOR STRUCTURE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7615866 | CONTACT SURROUNDED BY PASSIVATION AND POLYIMIDE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7616509 | DYNAMIC VOLTAGE ADJUSTMENT FOR MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 7616676 | METHOD AND SYSTEM FOR PERFORMING DISTANCE MEASURING AND DIRECTION FINDING USING ULTRAWIDE BANDWIDTH TRANSMISSIONS |
| FREESCALE SEMICONDUCTOR, INC. | 7617437 | ERROR CORRECTION DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7618902 | PLASMA TREATMENT OF A SEMICONDUCTOR SURFACE FOR ENHANCED NUCLEATION OF A METAL-CONTAINING LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7619270 | ELECTRONIC DEVICE INCLUDING DISCONTINUOUS STORAGE ELEMENTS |
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| Owner EDEFICATE CEMICONDUCTOR INC. | Patent # | Description A MADA CTOP |
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| FREESCALE SEMICONDUCTOR, INC. | 7619273 | A VARACTOR |
| FREESCALE SEMICONDUCTOR, INC. | 7619275 | ELECTRONIC DEVICE INCLUDING DISCONTINUOUS STORAGE ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | 7619297 | ELECTRONIC DEVICE INCLUDING AN INDUCTOR |
| FREESCALE SEMICONDUCTOR, INC. | 7619440 | CIRCUIT HAVING LOGIC STATE RETENTION DURING POWER-DOWN AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7619464 | CURRENT COMPARISON BASED VOLTAGE BIAS GENERATOR FOR ELECTRONIC DATA STORAGE DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7620760 | NON-HIGH IMPENDENCE DEVICE AND METHOD FOR REDUCING ENERGY CONSUMPTION |
| FREESCALE SEMICONDUCTOR, INC. | 7622309 | MECHANICAL INTEGRITY EVALUATION OF LOW-K DEVICES WITH BUMP SHEAR |
| FREESCALE SEMICONDUCTOR, INC. | 7622313 | FABRICATION OF THREE DIMENSIONAL INTEGRATED CIRCUIT EMPLOYING MULTIPLE DIE PANELS |
| FREESCALE SEMICONDUCTOR, INC. | 7622339 | EPI T-GATE STRUCTURE FOR CoSi2 EXTENDIBILITY |
| FREESCALE SEMICONDUCTOR, INC. | 7622349 | FLOATING GATE NON-VOLATILE MEMORY AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7623404 | MEMORY DEVICE HAVING CONCURRENT WRITE AND READ CYCLES AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7623894 | CELLULAR MODEM PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 7624329 | PRGRAMMING A MEMORY DEVICE HAVING ERROR CORRECTION LOGIC |
| FREESCALE SEMICONDUCTOR, INC. | 7624361 | METHOD AND DEVICE FOR DESIGNING SEMICONDUCTOR INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7626276 | METHOD AND APPARATUS FOR PROVIDING STRUCTURAL SUPPORT FOR INTERCONNECT PAD WHILE ALLOWING SIGNAL CONDUCTANCE |
| FREESCALE SEMICONDUCTOR, INC. | 7626842 | PHOTON-BASED MEMORY DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7627030 | RADIO RECEIVER WITH SELECTIVELY DISABLED EQUALIZER |
| FREESCALE SEMICONDUCTOR, INC. | 7627795 | PIPELINED DATA PROCESSOR WITH DETERMINISTIC SIGNATURE GENERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7628072 | MEMS DEVICE AND METHOD OF REDUCING STICTION IN A MEMS DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7629182 | SPACE AND PROCESS EFFICIENT MRAM AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7629220 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7629711 | LOAD INDEPENDENT VOLTAGE REGULATOR |
| FREESCALE SEMICONDUCTOR, INC. | 7629840 | DIGITAL PULSE WIDTH MODULATED FEEDBACK SYSTEM FOR A SWITCHING AMPLIFIER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7630272 | MULTIPLE PORT MEMORY WITH PRIORITIZED WORD LINE DRIVER AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7630429 | EQUALIZER CO-EFFICIENT GENERATION APPARATUS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7630457 | METHOD AND APPARATUS FOR DEMODULATING A RECEIVED SIGNAL WITHIN A CODED SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7630693 | TRANSMITTER WITH IMPROVED POWER EFFICIENCY |
| FREESCALE SEMICONDUCTOR, INC. | 7631229 | SELECTIVE BIT ERROR DETECTION AT A BUS DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7632698 | INTEGRATED CIRCUIT ENCAPSULATION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7632715 | METHOD OF PACKAGING SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7633307 | METHOD FOR DETERMINING TEMPERATURE PROFILE IN SEMICONDUCTOR MANUFACTURING TEST |
| FREESCALE SEMICONDUCTOR, INC. | 7634275 | METHOD OF ACCOMODATING PERIODIC INTERFACING SIGNALS IN A |

WIRELESS NETWORK

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7634396 | METHOD AND COMPUTER PROGRAM PRODUCT FOR GENERATION OF BUS FUNCTIONAL MODELS |
| FREESCALE SEMICONDUCTOR, INC. | 7634703 | LINEAR APPROXIMATION OF TEH MAX*OPERATION FOR LOG-MAP DECODING |
| FREESCALE SEMICONDUCTOR, INC. | 7635920 | METHOD AND APPARATUS FOR INDICATING DIRECTIONALITY IN INTEGRATED CIRCUIT MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | 7635998 | PRE-DRIVER FOR BRIDGE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7637160 | MEMS SUSPENSION AND ANCHORING DESIGN |
| FREESCALE SEMICONDUCTOR, INC. | 7638386 | INTEGRATED CMOS AND BIPOLAR DEVICES METHOD AND STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7638903 | POWER SUPPLY SELECTION FOR MULTIPLE CIRCUITS ON AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7638995 | CLOCKED RAMP APPARATUS FOR VOLTAGE REGULATOR SOFTSTART AND METHOD FOR SOFTSTARTING VOLTAGE REGULATORS |
| FREESCALE SEMICONDUCTOR, INC. | 7639083 | COMPENSATION FOR PARASITIC COUPLING BETWEEN RF OR MICROWAVE TRANSISTORS IN THE SAME PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7639097 | CRYSTAL OSCILLATOR CIRCUIT HAVING FAST START-UP AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7639671 | ALLOCATING PROCESSING RESOURCES FOR MULTIPLE INSTANCES OF A SOFTWARE COMPONENT |
| FREESCALE SEMICONDUCTOR, INC. | 7639762 | METHOD FOR RECEIVING AND RECOVERING FREQUENCY SHIFT KEYED SYMBOLS |
| FREESCALE SEMICONDUCTOR, INC. | 7640389 | NON-VOLATILE MEMORY HAVING A MULTIPLE BLOCK ERASE MODE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7642163 | ELECTRONIC DEVICE INCLUDING DISCONTINUOUS STORAGE ELEMENTS WITHIN A DIELECTRIC LAYER AND PROCESS OF FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7642182 | ESD PROTECTION FOR PASSIVE INTEGRATED DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7642594 | ELECTRONIC DEVICE INCLUDING GATE LINES, BIT LINES, OR A COMBINATION THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7643533 | LOW POWER, HIGH RESOLUTION TIMING GENERATOR FOR ULTRA-WIDE BANDWIDTH COMMUNICATION SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 7643602 | METHOD AND SYSTEM FOR ESTIMATING FREQUENCY OFFSETS |
| FREESCALE SEMICONDUCTOR, INC. | 7644200 | METHOD OF REPEATING DATA TRANSMISSION BETWEEN NETWORK DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7645651 | LDMOS WITH CHANNEL STRESS |
| FREESCALE SEMICONDUCTOR, INC. | 7647472 | HIGH SPEED AND HIGH THROUGHPUT DIGITAL COMMUNICATIONS PROCESSOR WITH EFFICIENT COOPERATION BETWEEN PROGRAMMABLE PROCESSING COMPONENTS |
| FREESCALE SEMICONDUCTOR, INC. | 7647573 | METHOD AND DEVICE FOR TESTING DELAY PATHS OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7648858 | METHODS AND APPARATUS FOR EMI SHIELDING IN MULTI-CHIP MODULES |
| FREESCALE SEMICONDUCTOR, INC. | 7648884 | SEMICONDUCTOR DEVICE WITH INTEGRATED RESISTIVE ELEMENT AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 7649234 | SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7649764 | MEMORY WITH SHARED WRITE BIT LINE(S) |
| FREESCALE SEMICONDUCTOR, INC. | 7649781 | BIT CELL REFERENCE DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7649957 | NON-OVERLAPPING MULTI-STAGE CLOCK GENERATOR SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7649961 | SUPPRESSED CARRIER QUADRATURE PULSE MODULATOR |
| FREESCALE SEMICONDUCTOR, INC. | 7650579 | MODEL CORRESPONDENCE METHOD AND DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7651889 | ELECTROMAGNETIC SHIELD FORMATION FOR INTEGRATED CIRCUIT DIE |

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| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7651916 | ELECTRONIC DEVICE INCLUDING TRENCHES AND DISCONTINUOUS STORAGE ELEMENTS AND PROCESSES OF FORMING AND USING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7651918 | STRAINED SEMICONDUCTOR POWER DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7651935 | ELECTRONIC DEVICE WITH A GATE ELECTRODE HAVING AT LEAST TWO PORTIONS AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7651939 | METHOD OF BLOCKING A VOID DURING CONTACT FORMATION PROCESS AND DEVICE HAVING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7652357 | QUAD FLAT NO-LEAD (QFN) PACKAGES |
| FREESCALE SEMICONDUCTOR, INC. | 7652486 | CAPACITANCE DETECTION CIRCUIT INCLUDING VOLTAGE COMPENSATION FUNCTION |
| FREESCALE SEMICONDUCTOR, INC. | 7653448 | NICAM PROCESSING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7653678 | A DIRECT DIGITAL SYNTHESIS CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7653765 | INFORMATION COMMUNICATION CONTROLLER INTERFACE APPARATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7653822 | ENTRY INTO A LOW POWER MODE UPON APPLICATION OF POWER AT A PROCESSING DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7655502 | METHOD OF PACKAGING A SEMICONDUCTOR DEVICE AND A PREFABRICATED CONNECTOR |
| FREESCALE SEMICONDUCTOR, INC. | 7655550 | A METHOD OF MAKING METAL GATE TRANSISTORS |
| FREESCALE SEMICONDUCTOR, INC. | 7656045 | CAP LAYER FOR AN ALUMINUM COPPER BOND PAD |
| FREESCALE SEMICONDUCTOR, INC. | 7657682 | BUS INTERCONNECT WITH FLOW CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 7657757 | SEMICONDUCTOR DEVICE AND METHOD UTILIZING VARIABLE MODE CONTROL WITH BLOCK CIPHERS |
| FREESCALE SEMICONDUCTOR, INC. | 7657854 | METHOD AND SYSTEM FOR DESIGNING TEST CIRCUIT IN A SYSTEM ON CHIP |
| FREESCALE SEMICONDUCTOR, INC. | 7659156 | METHOD TO SELECTIVELY MODULATE GATE WORK FUNCTION THROUGH SELECTIVE GE CONDENSATION AND HIGH-K DIELECTRIC LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7659704 | REGULATOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7663470 | TRIMMING CIRCUIT AND ELECTRONIC CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7664212 | APPARATUS AND METHOD FOR SWITCHING CLOCKS WHILE PREVENTING GLITCHES AND DATA LOSS |
| FREESCALE SEMICONDUCTOR, INC. | 7665361 | METHOD AND APPARATUS FOR CLOSED LOOP OFFSET CANCELLATION |
| FREESCALE SEMICONDUCTOR, INC. | 7666698 | METHOD FOR FORMING AND SEALING A CAVITY FOR AN INTEGRATED MEMS DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7666730 | METHOD FOR FORMING A DUAL METAL GATE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7667334 | INTEGRATED MATCHING NETWORKS AND RF DEVICES THAT INCLUDE AN INTEGRATED MATCHING NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 7667491 | LOW VOLTAGE OUTPUT BUFFER AND METHOD FOR BUFFERING DIGITAL OUTPUT DATA |
| FREESCALE SEMICONDUCTOR, INC. | 7667492 | INPUT BUFFER |
| FREESCALE SEMICONDUCTOR, INC. | 7667545 | AUTOMATIC CALIBRATION LOCK LOOP CIRCUIT AND METHOD HAVING IMPROVED LOCK TIME |
| FREESCALE SEMICONDUCTOR, INC. | 7668029 | MEMORY HAVING SENSE TIME OF VARIABLE DURATION |
| FREESCALE SEMICONDUCTOR, INC. | 7668274 | EYE CENTER RETRAINING SYSTEM AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7669034 | SYSTEM AND METHOD FOR MEMORY ARRAY WITH FAST ADDRESS DECODER |
| FREESCALE SEMICONDUCTOR, INC. | 7669100 | SYSTEM AND METHOD FOR TESTING AND PROVIDING AN INTEGRATED |

CIRCUIT HAVING MULTIPLE MODULES OR SUBMODULES

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7670760 | TREATMENT FOR REDUCTION OF LINE EDGE ROUGHNESS |
| FREESCALE SEMICONDUCTOR, INC. | 7670895 | ELECTRONIC DEVICE INCLUDING A SEMICONDUCTOR LAYER AND ANOTHER LAYER ADJACENT TO AN OPENING WITHIN THE SEMICONDUCTOR LAYER AND A PROCESS OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7671629 | SINGLE-SUPPLY, SINGLE-ENDED LEVEL CONVERSION CIRCUIT FOR AN INTEGRATED CIRCUIT HAVING MULTIPLE POWER SUPPLY DOMAINS |
| FREESCALE SEMICONDUCTOR, INC. | 7671654 | DEVICE HAVING CLOCK GENERATING CAPABILITIES AND A METHOD FOR GENERATING A CLOCK SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 7671774 | ANALOG-TO-DIGITAL CONVERTER WITH INTEGRATOR CIRCUIT FOR OVERLOAD RECOVERY |
| FREESCALE SEMICONDUCTOR, INC. | 7673268 | METHOD AND SYSTEM FOR INCORPORATING VIA REDUNDANCY IN TIMING ANALYSIS |
| FREESCALE SEMICONDUCTOR, INC. | 7673519 | PRESSURE SENSOR FEATURING OFFSET CANCELLATION AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 7674646 | THREE DIMENSIONAL INTEGRATED PASSIVE DEVICE AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 7674656 | DIE POSITIONING FOR PACKAGED INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 7674725 | TREATMENT SOLUTION AND METHOD OF APPLYING A PASSIVATING LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7675806 | LOW VOLTAGE MEMORY DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7676204 | RADIO RECEIVER HAVING IGNITION NOISE DETECTOR AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7676715 | INTEGRATED CIRCUIT WITH CONTINUOUS TESTING OF REPETITIVE FUNCTIONAL BLOCKS |
| FREESCALE SEMICONDUCTOR, INC. | 7676769 | ADAPTIVE THRESHOLD WAFER TESTING DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7678620 | ANITFUSE ONE TIME PROGRAMMABLE MEMORY ARRAY AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7678665 | DEEP STI TRENCH AND SOI UNDERCUT ENABLING STI OXIDE STRSSOR |
| FREESCALE SEMICONDUCTOR, INC. | 7678698 | METHOD OF FORMING A SEMICONDUCTOR DEVICE WITH MULTIPLE TENSILE STRESSOR LAYERS |
| FREESCALE SEMICONDUCTOR, INC. | 7679125 | BACK-GATED SEMICONDUCTOR DEVICE WITH A STORAGE LAYER AND METHODS FOR FORMING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7679373 | TRIMMING CIRCUIT, ELECTRONIC CIRCUIT AND TRIMMING CONTROL SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7679974 | MEMORY DEVICE HAVING SELECTIVELY DECOUPLEABLE MEMORY PORTIONS AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7680229 | METHOD OF DETERMINING A SYNCHRONOUS PHASE |
| FREESCALE SEMICONDUCTOR, INC. | 7680231 | ADAPTIVE VARIABLE LENGTH PULSE SYNCHRONIZER |
| FREESCALE SEMICONDUCTOR, INC. | 7680622 | PROTECTION OF AN INTEGRATED CIRCUIT AND METHOD THEREFORE |
| FREESCALE SEMICONDUCTOR, INC. | 7681021 | DYNAMIC BRANCH PREDICTION PREDICTOR |
| FREESCALE SEMICONDUCTOR, INC. | 7681078 | DEBUGGING A PROCESSOR THROUGH A RESET EVENT |
| FREESCALE SEMICONDUCTOR, INC. | 7681106 | ERROR CORRECTION DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7682912 | III-V COMPOUND SEMICONDUCTOR DEVICE WITH A SURFACE LAYER IN ACCESS REGIONS HAVING CHARGE OF POLARITY OPPOSITE TO CHANNEL CHARGE AND METHOD OF MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7683439 | SEMICONDUCTOR DEVICE HAVING A METAL CARBIDE GATE WITH AN ELCTROPOSITIVE ELEMENT AND A METHOD OF MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7683443 | MOS DEVICES WITH MULTI-LAYER GATE STACK |
| FREESCALE SEMICONDUCTOR, INC. | 7683465 | INTEGRATED CIRCUIT INCLUDING CLIP |
| FREESCALE SEMICONDUCTOR, INC. | 7683480 | METHODS AND APPARATUS FOR A REDUCED INDUCTANCE WIREBOND ARRAY |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7683483 | ELECTRONIC DEVICE WITH CONNECTION BUMPS |
| FREESCALE SEMICONDUCTOR, INC. | 7683486 | ELECTRONIC APPARATUS INTERCONNECT ROUTING AND INTERCONNECT ROUTING METHOD FOR MINIMIZING PARASITIC RESISTANCE |
| FREESCALE SEMICONDUCTOR, INC. | 7683668 | LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | 7683697 | CIRCUITRY AND METHOD FOR BUFFERING A POWER MODE CONTROL SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 7683733 | BALUN TRANSFORMER WITH IMPROVED HARMONIC SUPRESSION |
| FREESCALE SEMICONDUCTOR, INC. | 7683948 | SYSTEM AND METHOD FOR BAD PIXEL REPLACEMENT IN IMAGE PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 7684264 | MEMORY SYSTEM WITH RAM ARRAY AND REDUNDANT RAM MEMORY CELLS HAVING A DIFFERENT DESIGNED CELL CIRCUIT TOPOLOGY THAN CELLS OF NON REDUNDANT RAM ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | 7684380 | SYSTEM AND METHOD FOR HANDLING ASYNCHRONOUS DATA IN A WIRELESS NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 7684504 | SYSTEM AND METHOD FOR REDUCING EDGE EFFECT |
| FREESCALE SEMICONDUCTOR, INC. | 7684518 | LOGIC THRESHOLD ACQUISITION CIRCUITS AND METHODS USING REVERSED PEAK DETECTORS |
| FREESCALE SEMICONDUCTOR, INC. | 7687337 | TRANSISTOR WITH DIFFERENTLY DOPED STRAINED CURRENT ELECTRODE REGION |
| FREESCALE SEMICONDUCTOR, INC. | 7687354 | FABRICATION OF A SEMICONDUCTOR DEVICE WITH STRESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 7687370 | METHOD OF FORMING A SEMICONDUCTOR ISOLATION TRENCH |
| FREESCALE SEMICONDUCTOR, INC. | 7688100 | AN INTEGRATED CIRCUIT AND A METHOD FOR MEASURING A QUIESCENT CURRENT OF A MODULE |
| FREESCALE SEMICONDUCTOR, INC. | 7688113 | CURRENT DRIVER SUITABLE FOR USE IN A SHARED BUS ENVIRONMENT |
| FREESCALE SEMICONDUCTOR, INC. | 7688127 | A METHOD FOR GENERATING A OUTPUT CLOCK SIGNAL HAVING A OUTPUT CYCLE AND A DEVICE HAVING A CLOCK SIGNAL GENERATING CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 7688656 | INTEGRATED CIRCUIT MEMORY HAVING DYNAMICALLY ADJUSTABLE READ MARGIN AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7689193 | SELF-ALIGNING RESONATOR FILTER CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 7689897 | METHOD AND DEVICE FOR HIGH SPEED TESTING OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7689951 | DESIGN RULE CHECKING SYSTEM AND METHOD, FOR CHECKING COMPLIANCE OF AN INTEGRATED CIRCUIT DESIGN WITH A PLURALITY OF DESIGN RULES |
| FREESCALE SEMICONDUCTOR, INC. | 7692224 | MOSFET STRUCTURE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7692464 | PULSE WIDTH MODULATION WAVE OUTPUT CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7692989 | NON-VOLATILE MEMORY HAVING A STATIC VERIFY-READ OUTPUT DATA PATH |
| FREESCALE SEMICONDUCTOR, INC. | 7693219 | SYSTEM AND METHOD FOR FAST MOTION ESTIMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7693242 | DC OFFSET CORRECTION FOR CONSTANT ENVELOPE SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 7694825 | CARRIER TAPE FOR ELECTRONIC COMPONENTS |
| FREESCALE SEMICONDUCTOR, INC. | 7696016 | METHOD OF PACKAGING A DEVICE HAVING A TANGIBLE ELEMENT AND DEVICE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7696739 | ELECTRONIC SWITCH CIRCUIT, CONVERTER AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7697614 | SYSTEM AND METHOD FOR CALIBRATING AN ANALOG SIGNAL PATH DURING OPERATION IN AN ULTRA WIDEBAND RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 7697630 | ULTRA WIDEBAND COMMUNICATION METHOD WITH LOW NOISE PULSE FORMATION |
| EDEECCALE CENTICONDITIONOD TOTAL | E60E600 | LOWER A DIO DECEMEN |

7697632 LOW IF RADIO RECEIVER

FREESCALE SEMICONDUCTOR, INC.

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7697907 | SYSTEM AND METHOD FOR CONTROLLING THE TRANSMIT POWER OF A WIRELESS MODULE |
| FREESCALE SEMICONDUCTOR, INC. | 7698353 | FLOATING POINT NORMALIZATION AND DENORMALIZATION |
| FREESCALE SEMICONDUCTOR, INC. | 7698610 | TECHNIQUES FOR DETECTING OPEN INTEGRATED CIRCUIT PINS |
| FREESCALE SEMICONDUCTOR, INC. | 7698677 | ON-CHIP DECOUPLING CAPACITANCE AND POWER/GROUND NETWORK WIRE CO-OPTIMIZATION TO REDUCE DYNAMIC NOISE |
| FREESCALE SEMICONDUCTOR, INC. | 7700405 | MICROELECTRONIC ASSEMBLY WITH IMPROVED ISOLATION VOLTAGE PERFORMANCE AND A METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7700417 | CASCODE CURRENT MIRROR AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7700420 | INTEGRATED CIRCUIT WITH DIFFERENT CHANNEL MATERIALS FOR P AND N CHANNEL TRANSISTORS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7700438 | MOS DEVICE WITH NANO-CRYSTAL GATE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7700439 | SILICIDED NONVOLATILE MEMORY AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7700499 | MULTILAYER SILICON NITRIDE DEPOSITION FOR A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7700996 | TUNABLE ANTIFUSE ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | 7701012 | COMPLEMENTARY ZENER TRIGGERED BIPOLAR ESD PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 7701074 | SEMICONDUCTOR DEVICE WITH A BUFFER REGION WITH TIGHTLY-PACKED FILLER PARTICLES |
| FREESCALE SEMICONDUCTOR, INC. | 7701682 | ELECTROSTATIC DISCHARGE PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 7701785 | MEMORY WITH HIGH SPEED SENSING |
| FREESCALE SEMICONDUCTOR, INC. | 7702042 | ARRANGEMENT AND METHOD FOR ITERATIVE CHANNEL IMPLUSE RESPONSE ESTIMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7702881 | METHOD AND SYSTEM FOR DATA TRANSFER ACROSS DIFFERENT ADDRESS SPACES |
| FREESCALE SEMICONDUCTOR, INC. | 7704821 | IN-SITU NITRIDATION OF HIGH-K DIELECTRICS |
| FREESCALE SEMICONDUCTOR, INC. | 7704830 | SPLIT GATE MEMORY CELL USING SIDEWALL SPACERS |
| FREESCALE SEMICONDUCTOR, INC. | 7704838 | METHOD FOR FORMING AN INDEPENDENT BOTTOM GATE CONNECTION FOR BURIED INTERCONNECTION INCLUDING BOTTOM GATE OF A PLANAR DOUBLE GATE MOSFET |
| FREESCALE SEMICONDUCTOR, INC. | 7705440 | SUBSTRATE HAVING THROUGH-WAFER VIAS AND METHOD OF FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 7705555 | METHOD AND CONTROLLER FOR DETECTING A STALL CONDITION IN A STEPPING MOTOR DURING MICRO-STEPPING |
| FREESCALE SEMICONDUCTOR, INC. | 7705885 | IMAGE AND VIDEO MOTION STABILIZATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7706207 | MEMORY WITH LEVEL SHIFTING WORD LINE DRIVER AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7707335 | DEVICE AND METHOD FOR MANAGING A RETRANSMIT OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7707466 | SHARED LATCH FOR MEMORY TEST/REPAIR AND FUNCTIONAL OPERATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 7709303 | PROCESS FOR FORMING AN ELECTRONIC DEVICE INCLUDING A FIN-TYPE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7709331 | DUAL GATE OXIDE DEVICE INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | 7710090 | SERIES REGULATOR WITH FOLD-BACK OVER CURRENT PROTECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7710096 | REFERENCE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7710177 | LATCH DEVICE HAVING LOW-POWER DATA RETENTION |
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| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7710204 | ADAPTIVE PROTECTION CIRCUIT FOR A POWER AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 7711039 | SYSTEM AND METHOD FOR PROTECTING LOW VOLTAGE TRANSCEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 7712695 | SPOOL BRAKING DEVICE FOR FISHING REEL |
| FREESCALE SEMICONDUCTOR, INC. | 7713781 | METHODS FOR FORMING QUAD FLAT NO-LEAD (QFN) PACKAGES |
| FREESCALE SEMICONDUCTOR, INC. | 7713801 | A METHOD OF MAKING A SEMICONDUCTOR STRUCTURE UTILIZING SPACER REMOVAL AND SEMICONDUCTOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7714318 | ELECTRONIC DEVICE INCLUDING A TRANSISTOR STRUCTURE HAVING AN ACTIVE REGION ADJACENT TO A STRESSOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7715227 | PROGRAMMABLE ROM USING TWO BONDED STRATA |
| FREESCALE SEMICONDUCTOR, INC. | 7716453 | MEMORY MANAGEMENT UNIT AND A METHOD FOR MEMORY MANAGEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 7716511 | DYNAMIC TIMING ADJUSTMENT IN A CIRCUIT DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7718485 | INTERLAYER DIELECTRIC UNDER STRESS FOR AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7719039 | PHASE CHANGE MEMORY STRUCTURES INCLUDING PILLARS |
| FREESCALE SEMICONDUCTOR, INC. | 7720448 | SIGNAL GENERATION POWER MANAGEMENT CONTROL SYSTEM FOR PORTABLE COMMUNICATIONS DEVICE AND METHOD OF USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7721245 | SYSTEM AND METHOD FOR ELECTROMIGRATION TOLERANT CELL SYNTHESIS |
| FREESCALE SEMICONDUCTOR, INC. | 7723163 | METHOD OF FORMING PREMOLDED LEAD FRAME |
| FREESCALE SEMICONDUCTOR, INC. | 7723204 | SEMICONDUCTOR DEVICE WITH A MULTI-PLATE ISOLATION STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7723224 | MICROELECTRONIC ASSEMBLY WITH BACK SIDE METALLIZATION AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7723805 | ELECTRONIC DEVICE INCLUDING A FIN-TYPE TRANSISTOR STRUCTURE AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7723821 | MICROELECTRONIC ASSEMBLY AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7723823 | BURIED ASSYMETRIC JUNCTION ESD PROTECTION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7723962 | HIGH VOLTAGE PROTECTION FOR A THIN OXIDE CMOS DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7723968 | TECHNIQUE FOR IMPROVING EFFICIENCY OF A LINEAR VOLTAGE REGULATOR |
| FREESCALE SEMICONDUCTOR, INC. | 7724077 | STACKED CASCODE CURRENT SOURCE |
| FREESCALE SEMICONDUCTOR, INC. | 7724603 | METHOD AND CIRCUIT FOR PREVENTING HIGH VOLTAGE MEMORY DISTURB |
| FREESCALE SEMICONDUCTOR, INC. | 7724622 | RECORDING DEVICE CAPABLE OF DETERMINING THE MEDIA TYPE BASED ON DETECTING THE CAPACITANCE OF PAIR ELECTRODES |
| FREESCALE SEMICONDUCTOR, INC. | 7724783 | SYSTEM AND METHOD FOR PASSING DATA FRAMES IN A WIRELESS NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 7724842 | SYSTEM AND METHOD FOR EVM SELF-TEST |
| FREESCALE SEMICONDUCTOR, INC. | 7725638 | APPLICATION PROCESSOR CIRCUIT INCORPORATING BOTH SD HOST AND SLAVE FUNCTIONS AND ELECTRONIC DEVICE INCLUDING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7725788 | METHOD AND APPARATUS FOR SECURE SCAN TESTING |
| FREESCALE SEMICONDUCTOR, INC. | 7727817 | SEMICONDUCTOR INTEGRATED CIRCUIT PACKAGE AND METHOD OF PACKAGING SEMICONDUCTOR INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7727829 | METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING A REMOVABLE SIDEWALL SPACER |
| FREESCALE SEMICONDUCTOR, INC. | 7727870 | METHOD OF MAKING A SEMICONDUCTOR DEVICE USING A STRESSOR |

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| FREESCALE SEMICONDUCTOR, INC. | 7732102 | CR-CAPPED CHROMELESS PHASE LITHOGRAPHY |
| FREESCALE SEMICONDUCTOR, INC. | 7732274 | HIGH VOLTAGE DEEP TRENCH CAPACITOR |
| FREESCALE SEMICONDUCTOR, INC. | 7732278 | SPLIT GATE MEMORY CELL AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7733117 | METHOD FOR PROTECTING A SECURITY REAL TIME CLOCK GENERATOR AND A DEVICE HAVING PROTECTION CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 7733126 | NEGATIVE VOLTAGE GENERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7733181 | AMPLIFIER CIRCUIT HAVING DYNAMICALLY BIASED CONFIGURATION |
| FREESCALE SEMICONDUCTOR, INC. | 7733191 | OSCILLATOR DEVICES AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7733258 | DATA CONVERSION CIRCUITRY FOR CONVERTING ANALOG SIGNALS TO DIGITAL SIGNALS AND VICE-VERSA AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7733711 | CIRCUIT AND METHOD FOR OPTIMIZING MEMORY SENSE AMPLIFIER TIMING |
| FREESCALE SEMICONDUCTOR, INC. | 7734674 | FAST FOURIER TRANSFORM (FFT) ARCHITECTURE IN A MULTI-MODE WIRELESS PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7735029 | METHOD AND SYSTEM FOR IMPROVING THE MANUFACTURABILITY OF INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 7736957 | METHOD OF MAKING A SEMICONDUCTOR DEVICE WITH EMBEDDED STRESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 7736996 | METHOD FOR DAMAGE AVOIDANCE IN TRANSFERRING AN ULTRA-THIN LAYER OF CRYSTALLINE MATERIAL WITH HIGH CRYSTALLINE QUALITY |
| FREESCALE SEMICONDUCTOR, INC. | 7737018 | PROCESS OF FORMING AN ELECTRONIC DEVICE INCLUDING FORMING A GATE ELECTRODE LAYER AND FORMING A PATTERNED MASKING LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7737670 | CONVERTER WITH IMPROVED EFFICIENCY |
| FREESCALE SEMICONDUCTOR, INC. | 7737676 | SERIES REGULATOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7737740 | INTEGRATED CIRCUIT WITH A PROGRAMMABLE DELAY AND A METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7738563 | METHOD AND SYSTEM FOR PERFORMING DEBLOCKING FILTERING |
| FREESCALE SEMICONDUCTOR, INC. | 7739674 | METHOD AND APPARATUS FOR SELECTIVELY OPTIMIZING INTERPRETED LANGUAGE CODE |
| FREESCALE SEMICONDUCTOR, INC. | 7740805 | INTEGRATED CMOS-COMPATIBLE BIOCHIP |
| FREESCALE SEMICONDUCTOR, INC. | 7741151 | INTEGRATED CIRCUIT PACKAGE FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7741183 | METHOD OF FORMING A GATE DIELECTRIC |
| FREESCALE SEMICONDUCTOR, INC. | 7741194 | REMOVABLE LAYER MANUFACTURING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7741195 | METHOD OF STIMULATING DIE CIRCUITRY AND STRUCTURE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7741196 | SEMICONDUCTOR WAFER WITH IMPROVED CRACK PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 7741218 | CONDUCTIVE VIA FORMATION UTILIZING ELECTROPLATING |
| FREESCALE SEMICONDUCTOR, INC. | 7741221 | METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING DUMMY FEATURES |
| FREESCALE SEMICONDUCTOR, INC. | 7741718 | ELECTRONIC APPARATUS INTERCONNECT ROUTING |
| FREESCALE SEMICONDUCTOR, INC. | 7741826 | DEVICE AND METHOD FOR COMPENSATING FOR GROUND VOLTAGE ELEVATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 7742275 | MEMS CAPACITOR WITH CONDUCTIVELY TETHERED MOVEABLE CAPACITOR PLATE |
| FREESCALE SEMICONDUCTOR, INC. | 7742340 | READ REFERENCE TECHNIQUE WITH CURRENT DEGRADATION PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 7743988 | AUTHENTICATION SYSTEM INCLUDING ELECTRIC FIELD SENSOR |

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| FREESCALE SEMICONDUCTOR, INC. | 7745260 | METHOD OF FORMING SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7745298 | METHOD OF FORMING A VIA |
| FREESCALE SEMICONDUCTOR, INC. | 7745344 | METHOD FOR INTEGRATING NVM CIRCUITRY WITH LOGIC CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | 7745870 | PROGRAMMING AND ERASING STRUCTURE FOR A FLOATING GATE MEMORY CELL AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 7746129 | AN ULTRA LOW POWER SERVO-CONTROLLED SINGLE CLOCK RAMP GENERATOR WITH AMPLITUDE INDEPENDENT TO CLOCK FREQUENCY |
| FREESCALE SEMICONDUCTOR, INC. | 7746716 | MEMORY HAVING A DUMMY BITLINE FOR TIMING CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 7747889 | BUS HAVING A DYNAMIC TIMING BRIDGE |
| FREESCALE SEMICONDUCTOR, INC. | 7749829 | STEP HEIGHT REDUCTION BETWEEN SOI AND EPI FOR DSO AND BOS INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | 7750374 | ELECTRONIC DEVICE INCLUDING A TRANSISTOR HAVING A METAL GATE ELECTRODE AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7750465 | PACKAGED INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7751177 | THIN-FILM CAPACITOR WITH A FIELD MODIFICATION LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7751443 | COMMUNICATION DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7751792 | HIGHER LINEARITY PASSIVE MIXER |
| FREESCALE SEMICONDUCTOR, INC. | 7754560 | INTEGRATED CIRCUIT USING FINFETS AND HAVING A STATIC RANDOM ACCESS MEMORY (SRAM) |
| FREESCALE SEMICONDUCTOR, INC. | 7754587 | SILICON DEPOSITION OVER DUAL SURFACE ORIENTATION SUBSTRATES TO PROMOTE UNIFORM POLISHING |
| FREESCALE SEMICONDUCTOR, INC. | 7756231 | DIGITAL CLOCK GENERATING CIRCUIT AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7759753 | INTEGRATED CIRCUIT DIE, INTEGRATED CIRCUIT PACKAGE, AND PACKAGING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7760114 | A SYSTEM AND A METHOD FOR GENERATING AN INTERLEAVED OUTPUT DURING A DECODING OF A DATA BLOCK |
| FREESCALE SEMICONDUCTOR, INC. | 7760536 | NON-VOLATILE MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | 7760816 | AUTOMATIC GAIN CONTROL USING MULTIPLE EQUALIZED ESTIMATES AND DYNAMIC HYSTERESIS |
| FREESCALE SEMICONDUCTOR, INC. | 7760960 | LOCALIZED CONTENT ADAPTIVE FILTER FOR LOW POWER SCALABLE IMAGE PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 7761760 | INTEGRATED CIRCUIT AND A METHOD FOR DESIGNING A BOUNDARY SCAN SUPER-CELL |
| FREESCALE SEMICONDUCTOR, INC. | 7763510 | METHOD FOR PFET ENHANCEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 7763538 | DUAL PLASMA TREATMENT BARRIER FILM TO REDUCE LOW-K DAMAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7763937 | VARIABLE RESURF SEMICONDUCTOR DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7763976 | INTEGRATED CIRCUIT MODULE WITH INTEGRATED PASSIVE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7764091 | SQUARE TO PSEUDO-SINUSOIDAL CLOCK CONVERSION CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7764123 | RAIL TO RAIL BUFFER AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 7764550 | METHOD OF PROGRAMMING A NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 7767588 | METHOD FOR FORMING A DEPOSITED OXIDE LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7768296 | ELECTRONIC DEVICE AND METHOD |

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| FREESCALE SEMICONDUCTOR, INC. | 7769112 | METHOD AND SYSTEM FOR GENERATING WAVELETS |
| FREESCALE SEMICONDUCTOR, INC. | 7770929 | VEHICULAR SEATBELT RESTRAINT WITH SELECTIVELY DISABLED INERTIA REEL ASSEMBLY |
| FREESCALE SEMICONDUCTOR, INC. | 7772036 | LEAD FRAME BASED, OVER-MOLDED SEMICONDUCTOR PACKAGE WITH INTEGRATED THROUGH HOLE TECHNOLOGY (THT) HEAT SPREADER PIN(S) AND ASSOCIATED METHOD OF MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | 7772048 | FORMING SEMICONDUCTOR FINS USING A SACRIFICIAL FIN |
| FREESCALE SEMICONDUCTOR, INC. | 7772104 | DYNAMIC PAD SIZE TO REDUCE SOLDER FATIGUE |
| FREESCALE SEMICONDUCTOR, INC. | 7772584 | LATERALLY GROWN NANOTUBES AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7772694 | INTEGRATED CIRCUIT MODULE AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7773003 | HUFFMAN SEARCH ALGORITHM FOR AAC DECODER |
| FREESCALE SEMICONDUCTOR, INC. | 7773424 | CIRCUIT FOR AND AN ELECTRONIC DEVICE INCLUDING A NONVOLATILE MEMORY CELL AND A PROCESS OF FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7773672 | SCALABLE RATE CONTROL SYSTEM FOR A VIDEO ENCODER |
| FREESCALE SEMICONDUCTOR, INC. | 7776700 | LDMOS DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7776731 | METHOD OF REMOVING DEFECTS FROM A DIELECTRIC MATERIAL IN A SEMICONDUCTOR |
| FREESCALE SEMICONDUCTOR, INC. | 7777257 | BIPOLAR SCHOTTKY DIODE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7777330 | HIGH BANDWIDTH CACHE-TO-PROCESSING UNIT COMMUNICATION IN A MULTIPLE PROCESSOR/CACHE SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7777364 | DRIVE ARRANGEMENT FOR ACTIVATING A CAR SAFETY DEVICE ACTIVATION ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 7777509 | METHOD AND APPARATUS FOR ELECTRICAL TESTING |
| FREESCALE SEMICONDUCTOR, INC. | 7777522 | CLOCKED SINGLE POWER SUPPLY LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | 7777998 | ELECTROSTATIC DISCHARGE CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7778030 | METHOD FOR COOLING USING IMPINGING JET CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 7778154 | TECHNIQUES FOR REDUCING INTERFERENCE IN A COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7778252 | HARDWARE MONITOR OF LIN TIME BUDGET |
| FREESCALE SEMICONDUCTOR, INC. | 7778347 | POWER DE-RATING REDUCTION IN A TRANSMITTER |
| FREESCALE SEMICONDUCTOR, INC. | 7779689 | MULTIPLE AXIS TRANSDUCER WITH MULTIPLE SENSING RANGE CAPABILITY |
| FREESCALE SEMICONDUCTOR, INC. | 7781277 | SELECTIVE UNIAXIAL STRESS RELAXATION BY LAYOUT OPTIMIZATION IN STRAINED SILICON ON INSULATOR INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7781831 | SEMICONDUCTOR DEVICE HAVING NITRIDATED OXIDE LAYER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7781839 | STRUCTURE AND METHOD FOR STRAINED TRANSISTOR DIRECTLY ON INSULATOR |
| FREESCALE SEMICONDUCTOR, INC. | 7781840 | SEMICONDUCTOR DEVICE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7782664 | METHOD FOR ELECTRICALLY TRIMMING AN NVM REFERENCE CELL |
| FREESCALE SEMICONDUCTOR, INC. | 7782925 | METHOD AND DEVICE FOR GENERATING HIGH FREQUENCY WAVEFORMS |
| FREESCALE SEMICONDUCTOR, INC. | 7782991 | FRACTIONALLY RELATED MULTIRATE SIGNAL PROCESSOR AND METHOD |
| EDERGCALE CELUCONDUCTOD TO | | |

FREESCALE SEMICONDUCTOR, INC. 7783321 CELL PHONE DEVICE

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| FREESCALE SEMICONDUCTOR, INC. | 7783908 | METHOD AND DEVICE TO WAKE-UP NODES IN A SERIAL DATA BUS |
| FREESCALE SEMICONDUCTOR, INC. | 7785983 | SEMICONDUCTOR DEVICE HAVING TILES FOR DUAL-TRENCH INTEGRATION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7786603 | ELECTRONIC ASSEMBLY HAVING GRADED WIRE BONDING |
| FREESCALE SEMICONDUCTOR, INC. | 7786713 | SERIES REGULATOR CIRCUIT WITH HIGH CURRENT MODE ACTIVATING PARALLEL CHARGING PATH |
| FREESCALE SEMICONDUCTOR, INC. | 7786714 | VOLTAGE CONVERTER APPARATUS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7786805 | A POWER AMPLIFIER MODULE AND A TIME DIVISION MULTIPLE ACCESS RADIO |
| FREESCALE SEMICONDUCTOR, INC. | 7786809 | METHOD OF LOW POWER PLL FOR LOW JITTER DEMANDING APPLICATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 7787323 | LEVEL DETECT CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7788424 | METHOD OF TRANSMITTING DATA FROM A TRANSMITTING DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7788471 | DATA PROCESSOR AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7790528 | DUAL SUBSTRATE ORIENTATION OR BULK ON SOI INTEGRATIONS USING OXIDATION FOR SILICON EPITAXY SPACER FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7791161 | SEMICONDUCTOR DEVICES EMPLOYING POLY-FILLED TRENCHES |
| FREESCALE SEMICONDUCTOR, INC. | 7791367 | DRIVER WITH SELECTABLE OUTPUT IMPEDANCE |
| FREESCALE SEMICONDUCTOR, INC. | 7791389 | STATE RETAINING POWER GATED LATCH AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7791956 | METHOD AND SYSTEM FOR SIMULTANEOUS READS OF MULTIPLE ARRAYS |
| FREESCALE SEMICONDUCTOR, INC. | 7793021 | METHOD FOR SYNCHRONIZING A TRANSMISSION OF INFORMATION AND A DEVICE HAVING SYNCHRONIZING CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 7793025 | HARDWARE MANAGED CONTEXT SENSITIVE INTERRUPT PRIORITY LEVEL CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 7793172 | CONTROLLED RELIABILITY IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7793542 | CADDIE-CORNER SINGLE PROOF MASS XYZ MEMS TRANSDUCER |
| FREESCALE SEMICONDUCTOR, INC. | 7795089 | FORMING A SEMICONDUCTOR DEVICE HAVING EPITAXIALLY GROWN SOURCE AND DRAIN REGIONS |
| FREESCALE SEMICONDUCTOR, INC. | 7795091 | METHOD OF FORMING A SPLIT GATE MEMORY DEVICE AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 7795674 | DUAL GATE LDMOS DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7795702 | MICROELECTRONIC ASSEMBLIES WITH IMPROVED ISOLATION VOLTAGE PERFORMANCE |
| FREESCALE SEMICONDUCTOR, INC. | 7795848 | METHOD AND CIRCUIT FOR GENERATING OUTPUT VOLTAGES FROM INPUT VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7795904 | SWITCHING CIRCUIT HAVING A DRIVER FOR PROVIDING A LINEAR VOLTAGE TRANSITION |
| FREESCALE SEMICONDUCTOR, INC. | 7795951 | HIGH-DYNAMIC RANGE LOW RIPPLE VOLTAGE MULTIPLIER |
| FREESCALE SEMICONDUCTOR, INC. | 7795980 | POWER AMPLIFIERS HAVING IMPROVED PROTECTION AGAINST AVALANCHE CURRENT |
| FREESCALE SEMICONDUCTOR, INC. | 7796079 | CHARGE REDISTRIBUTION SUCCESSIVE APPROXIMATION ANALOG-TO- DIGITAL CONVERTER AND RELATED OPERATING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7796688 | RADIO RECEIVER HAVING A CHANNEL EQUALIZER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7797618 | PARALLEL RECODER FOR ULTRAWIDE BANDWIDTH RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 7799634 | METHOD OF FORMING NANOCRYSTALS |
| FREESCALE SEMICONDUCTOR, INC. | 7799644 | TRANSISTOR WITH ASYMMETRY FOR DATA STORAGE CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | 7799647 | MOSFET DEVICE FEATURING A SUPERLATTICE BARRIER LAYER AND METHOD |

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| FREESCALE SEMICONDUCTOR, INC. | 7799650 | METHOD FOR MAKING A TRANSISTOR WITH A STRESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 7799657 | METHOD OF FABRICATING A SUBSTRATE FOR A PLANAR, DOUBLE GATED, TRANSISTOR PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 7799661 | ELECTRICAL SENSOR FOR REAL-TIME FEEDBACK CONTROL OF PLASMA NITRIDATION |
| FREESCALE SEMICONDUCTOR, INC. | 7799678 | METHOD FOR FORMING A THROUGH SILICON VIA LAYOUT |
| FREESCALE SEMICONDUCTOR, INC. | 7800135 | POWER SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING A POWER SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7800141 | ELECTRONIC DEVICE INCLUDING A SEMICONDUCTOR FIN AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7800164 | NANOCRYSTAL NON-VOLATILE MEMORY CELL AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7800350 | APPARATUS FOR OPTIMIZING DIODE CONDUCTION TIME DURING A DEADTIME INTERVAL |
| FREESCALE SEMICONDUCTOR, INC. | 7800959 | MEMORY HAVING SELF-TIMED BIT LINE BOOST CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7800974 | ADJUSTABLE PIPELINE IN A MEMORY CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7802241 | METHOD FOR ESTIMATING PROCESSOR ENERGY USAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7802359 | ELECTRONIC ASSEMBLY MANUFACTURING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7802471 | LIQUID LEVEL SENSING DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7803662 | WARPAGE CONTROL USING A PACKAGE CARRIER ASSEMBLY |
| FREESCALE SEMICONDUCTOR, INC. | 7803670 | TWISTED DUAL-SUBSTRATE ORIENTATION (DSO) SUBSTRATES |
| FREESCALE SEMICONDUCTOR, INC. | 7803685 | SILICIDED BASE STRUCTURE FOR HIGH FREQUENCY TRANSISTORS |
| FREESCALE SEMICONDUCTOR, INC. | 7803714 | SEMICONDUCTOR THROUGH SILICON VIAS OF VARIABLE SIZE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7804258 | CIRCUIT FOR PROVIDING AN APPROXIMATELY CONSTANT RESISTANCE AND/OR CURRENT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7804283 | MODE TRANSITIONING IN A DC/DC CONVERTER USING A CONSTANT DUTY CYCLE DIFFERENCE |
| FREESCALE SEMICONDUCTOR, INC. | 7804701 | METHOD OF PROGRAMMING A MEMORY HAVING ELECTRICALLY PROGRAMMABLE FUSES |
| FREESCALE SEMICONDUCTOR, INC. | 7805581 | MULTI-MODE DATA PROCESSING DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7805590 | COPROCESSOR RECEIVING TARGET ADDRESS TO PROCESS A FUNCTION AND TO SEND DATA TRANSFER INSTRUCTIONS TO MAIN PROCESSOR FOR EXECUTION TO PRESERVE CACHE COHERENCE |
| FREESCALE SEMICONDUCTOR, INC. | 7807511 | METHOD OF PACKAGING A DEVICE HAVING A MULTI-CONTACT ELASTOMER CONNECTOR CONTACT AREA AND DEVICE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7807572 | MICROPAD FORMATION FOR A SEMICONDUCTOR |
| FREESCALE SEMICONDUCTOR, INC. | 7808117 | INTEGRATED CIRCUIT HAVING PADS AND INPUT/OUTPUT (I/O) CELLS |
| FREESCALE SEMICONDUCTOR, INC. | 7808258 | TEST INTERPOSER HAVING ACTIVE CIRCUIT COMPONENT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7808279 | LOW POWER, SELF-GATED, PULSE TRIGGERED CLOCK GATING CELL |
| FREESCALE SEMICONDUCTOR, INC. | 7808286 | CIRCUITRY IN A DRIVER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7809980 | ERROR DETECTOR IN A CACHE MEMORY USING CONFIGURABLE WAY REDUNDANCY |
| FREESCALE SEMICONDUCTOR, INC. | 7811382 | METHOD FOR FORMING A SEMICONDUCTOR STRUCTURE HAVING A STRAINED SILICON LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7811851 | PHASE CHANGE MEMORY STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | 7811886 | SPLIT-GATE THIN FILM STORAGE NVM CELL WITH REDUCED LOAD-UP/TRAP-UP EFFECTS |

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| FREESCALE SEMICONDUCTOR, INC. | 7811889 | FINFET MEMORY CELL HAVING A FLOATING GATE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7811891 | METHOD TO CONTROL THE GATE SIDEWALL PROFILE BY GRADED MATERIAL COMPOSITION |
| FREESCALE SEMICONDUCTOR, INC. | 7811932 | 3-D SEMICONDUCTOR DIE STRUCTURE WITH CONTAINING FEATURE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7812448 | ELECTRONIC DEVICE INCLUDING A CONDUCTIVE STUD OVER A BONDING PAD REGION AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7813908 | CLOCK CONTROL MODULE SIMULATOR AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7816211 | METHOD OF MAKING A SEMICONDUCTOR DEVICE HAVING HIGH VOLTAGE TRANSISTORS, NON-VOLATILE MEMORY TRANSISTORS, AND LOGIC TRANSISTORS |
| FREESCALE SEMICONDUCTOR, INC. | 7816221 | DIELECTRIC LEDGE FOR HIGH FREQUENCY DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7816948 | VOLTAGE TRANSLATOR |
| FREESCALE SEMICONDUCTOR, INC. | 7817387 | MIGFET CIRCUIT WITH ESD PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 7818720 | METHOD AND APPARATUS FOR OPTIMIZING BOOLEAN EXPRESSION EVALUATION |
| FREESCALE SEMICONDUCTOR, INC. | 7820485 | METHOD OF FORMING A PACKAGE WITH EXPOSED COMPONENT SURFACES |
| FREESCALE SEMICONDUCTOR, INC. | 7820491 | LIGHT ERASABLE MEMORY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7820519 | PROCESS OF FORMING AN ELECTRONIC DEVICE INCLUDING A CONDUCTIVE STRUCTURE EXTENDING THROUGH A BURIED INSULATING LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7820520 | SEMICONDUCTOR DEVICE WITH CAPACITOR AND/OR INDUCTOR AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 7820538 | METHOD OF FABRICATING A MOS DEVICE WITH NON-SIO2 GATE DIELECTRIC |
| FREESCALE SEMICONDUCTOR, INC. | 7820539 | METHOD FOR SEPARATELY OPTIMIZING SPACER WIDTH FOR TWO TRANSISTOR GROUPS USING A RECESS SPACER ETCH (RSE) INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | 7821055 | STRESSED SEMICONDUCTOR DEVICE AND METHOD FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 7821067 | ELECTRONIC DEVICES INCLUDING A SEMICONDUCTOR LAYER AND A PROCESS FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7821102 | POWER TRANSISTOR FEATURING A DOUBLE-SIDED FEED DESIGN AND METHOD OF MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7821103 | COUNTER-DOPED VARACTOR STRUCTURE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7821104 | PACKAGE DEVICE HAVING CRACK ARREST FEATURE AND METHOD OF FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 7821117 | SEMICONDUCTOR PACKAGE AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7821240 | VOLTAGE REGULATOR WITH PASS TRANSISTORS CARRYING DIFFERENT RATIOS OF THE TOTAL LOAD CURRENT AND METHOD OF OPERATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7821787 | SYSTEM AND METHOD FOR COOLING USING IMPINGING JET CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 7822131 | REDUCING A PEAK-TO-AVERAGE RATIO OF A SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 7823033 | DATA PROCESSING WITH RECONFIGURABLE REGISTERS |
| FREESCALE SEMICONDUCTOR, INC. | 7824988 | METHOD OF FORMING AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7825610 | LED DRIVER WITH DYNAMIC POWER MANAGEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 7825720 | CIRCUIT FOR A LOW POWER MODE |
| FREESCALE SEMICONDUCTOR, INC. | 7825726 | DIGITAL PULSE WIDTH MODULATION FOR HALF BRIDGE AMPLIFIERS |

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| FREESCALE SEMICONDUCTOR, INC. | 7827336 | TECHNIQUE FOR INTERCONNECTING INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 7829366 | MICROELECTROMECHANICAL SYSTEMS COMPONENT AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7829447 | SEMICONDUCTOR STRUCTURE PATTERN FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7829997 | NOVEL INTERCONNECT FOR CHIP LEVEL POWER DISTRIBUTION |
| FREESCALE SEMICONDUCTOR, INC. | 7831818 | EXCEPTION-BASED TIMER CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 7833852 | SOURCE/DRAIN STRESSORS FORMED USING IN-SITU EPITAXIAL GROWTH |
| FREESCALE SEMICONDUCTOR, INC. | 7833858 | SUPERJUNCTION TRENCH DEVICE FORMATION METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 7834417 | ANTIFUSE ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | 7834428 | APPARATUS AND METHOD FOR REDUCING NOISE IN MIXED-SIGNAL CIRCUITS AND DIGITAL CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 7834431 | LEADFRAME FOR PACKAGED ELECTRONIC DEVICE WITH ENHANCED MOLD LOCKING CAPABILITY |
| FREESCALE SEMICONDUCTOR, INC. | 7834466 | SEMICONDUCTOR DIE WITH DIE PAD PATTERN |
| FREESCALE SEMICONDUCTOR, INC. | 7834601 | CIRCUIT AND METHOD FOR REDUCING OUTPUT NOISE OF REGULATOR |
| FREESCALE SEMICONDUCTOR, INC. | 7834657 | INVERTER CIRCUIT WITH COMPENSATION FOR THRESHOLD VOLTAGE VARIATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 7834689 | MOS OPERATIONAL AMPLIFIER WITH CURRENT MIRRORING GAIN AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7834787 | TECHNIQUES FOR DELAY COMPENSATION OF CONTINUOUS-TIME SIGMADELTA MODULATORS |
| FREESCALE SEMICONDUCTOR, INC. | 7835124 | SHORT CIRCUIT AND OVER-VOLTAGE PROTECTION FOR A DATA BUS |
| FREESCALE SEMICONDUCTOR, INC. | 7835434 | ADAPTIVE RADIO FREQUENCY (RF) FILTER |
| FREESCALE SEMICONDUCTOR, INC. | 7836283 | DATA ACQUISITION MESSAGING USING SPECIAL PURPOSE REGISTERS |
| FREESCALE SEMICONDUCTOR, INC. | 7836369 | DEVICE AND METHOD FOR CONFIGURING INPUT/OUTPUT PADS |
| FREESCALE SEMICONDUCTOR, INC. | 7837762 | METHOD OF DISTANCING A BUBBLE AND BUBBLE DISPLACEMENT APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 7838345 | ELECTRONIC DEVICE INCLUDING SEMICONDUCTOR FINS AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7838363 | METHOD OF FORMING A SPLIT GATE NON-VOLATILE MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | 7838383 | LINEARITY CAPACITOR STRUCTURE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7838389 | ENCLOSED VOID CAVITY FOR LOW DIELECTRIC CONSTANT INSULATOR |
| FREESCALE SEMICONDUCTOR, INC. | 7838420 | METHOD FOR FORMING A PACKAGED SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7838922 | ELECTRONIC DEVICE INCLUDING TRENCHES AND DISCONTINUOUS STORAGE ELEMENTS AND PROCESSES OF FORMING AND USING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7839189 | VOLTAGE DETECTOR DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7839207 | INTEGRATED CIRCUIT AND A METHOD FOR RECOVERING FROM A LOW-POWER PERIOD |
| FREESCALE SEMICONDUCTOR, INC. | 7840189 | FREQUENCY GENERATION IN A WIRELESS COMMUNICATION UNIT |
| FREESCALE SEMICONDUCTOR, INC. | 7842546 | INTEGRATED CIRCUIT MODULE AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7842573 | VIRTUAL GROUND MEMORY ARRAY AND METHOD THEREFOR |
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7842587 III-V MOSFET FABRICATION AND DEVICE

FREESCALE SEMICONDUCTOR, INC.

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7843011 | ELECTRONIC DEVICE INCLUDING INSULATING LAYERS HAVING DIFFERENT STRAINS AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7843033 | SHIELDED INTEGRATED CIRCUIT PAD STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7843218 | DATA LATCH WITH STRUCTURAL HOLD |
| FREESCALE SEMICONDUCTOR, INC. | 7843231 | TEMPERATURE-COMPENSATED VOLTAGE COMPARATOR |
| FREESCALE SEMICONDUCTOR, INC. | 7843242 | PHASE-SHIFTED PULSE WIDTH MODULATION SIGNAL GENERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7843730 | NON-VOLATILE MEMORY WITH REDUCED CHARGE FLUENCE |
| FREESCALE SEMICONDUCTOR, INC. | 7844048 | TONE EVENT DETECTOR AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7844937 | METHOD AND APPARATUS FOR MAKING A SEMICONDUCTOR DEVICE USING HARDWARE DESCRIPTION HAVING MERGED FUNCTIONAL AND TEST LOGIC BLOCKS |
| FREESCALE SEMICONDUCTOR, INC. | 7846803 | MULTIPLE MILLISECOND ANNEALS FOR SEMICONDUCTOR DEVICE FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 7846815 | EUTECTIC FLOW CONTAINMENT IN A SEMICONDUCTOR FABRICATION PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 7847177 | DIGITAL COMPLEX TONE GENERATOR AND CORRESPONDING METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 7847524 | HIGH VOLTAGE PROTECTION FOR A THIN OXIDE CMOS DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7849247 | INTERRUPT ACKNOWLEDGMENT IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7851340 | SEMICONDUCTOR FIN INTEGRATION USING A SACRIFICIAL FIN |
| FREESCALE SEMICONDUCTOR, INC. | 7851834 | CASCODE DEVICES AND CURRENT MIRRORS |
| FREESCALE SEMICONDUCTOR, INC. | 7851857 | DUAL CURRENT PATH LDMOSFET WITH GRADED PBL FOR ULTRA HIGH VOLTAGE SMART POWER APPLICATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 7851889 | MOSFET DEVICE INCLUDING A SOURCE WITH ALTERNATING P-TYPE AND N-TYPE REGIONS |
| FREESCALE SEMICONDUCTOR, INC. | 7852249 | SIGMA-DELTA MODULATOR WITH DIGITALLY FILTERED DELAY COMPENSATION |
| FREESCALE SEMICONDUCTOR, INC. | 7852253 | DIGITALLY ADJUSTABLE QUANTIZATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7852692 | MEMORY OPERATION TESTING |
| FREESCALE SEMICONDUCTOR, INC. | 7855517 | CURRENT DRIVER CIRCUIT AND METHOD OF OPERATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7855562 | DUAL SENSOR SYSTEM HAVING FAULT DETECTION CAPABILITY |
| FREESCALE SEMICONDUCTOR, INC. | 7855581 | REAL TIME CLOCK MONITORING METHOD AND SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7858482 | METHOD OF FORMING A SEMICONDUCTOR DEVICE USING STRESS MEMORIZATION |
| FREESCALE SEMICONDUCTOR, INC. | 7858487 | METHOD AND APPARATUS FOR INDICATING DIRECTIONALITY IN INTEGRATED CIRCUIT MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | 7858505 | METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE TYPES OF SCHOTTKY JUNCTIONS |
| FREESCALE SEMICONDUCTOR, INC. | 7859068 | INTEGRATED CIRCUIT ENCAPSULATION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7859299 | CIRCUIT FOR CONTROLLING DATA COMMUNICATION WITH SYNCHRONOUS STORAGE CIRCUITRY AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7859919 | MEMORY DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7861200 | SETUP AND HOLD TIME CHARACTERIZATION DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7863876 | A BUILT-IN SELF CALIBRATION (BISC) TECHNIQUE FOR REGULATION CIRCUITS USED IN NON-VOLATILE MEMORY |

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| FREESCALE SEMICONDUCTOR, INC. | 7863938 | ADDRESS DECODER AND METHOD FOR SETTING AN ADDRESS |
| FREESCALE SEMICONDUCTOR, INC. | 7863963 | LEVEL SHIFTER FOR CHANGE OF BOTH HIGH AND LOW VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7864617 | MEMORY WITH REDUCED POWER SUPPLY VOLTAGE FOR A WRITE OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7865691 | A VIRTUAL ADDRESS CACHE AND METHOD FOR SHARING DATA USING A UNIQUE TASK IDENTIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 7865704 | SELECTIVE INSTRUCTION BREAKPOINT GENERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7865797 | MEMORY DEVICE WITH ADJUSTABLE READ REFERENCE BASED ON ECC AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7867858 | HYBRID TRANSISTOR BASED POWER GATING SWITCH CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7868389 | ELECTRONIC DEVICE COMPRISING A GATE ELECTRODE INCLUDING A METAL- CONTAINING LAYER HAVING ONE OR MORE IMPURITIES |
| FREESCALE SEMICONDUCTOR, INC. | 7868393 | SPACE EFFICIENT INTEGRATED CIRCUIT WITH PASSIVE DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7868449 | SEMICONDUCTOR SUBSTRATE AND METHOD OF CONNECTING SEMICONDUCTOR DIE TO SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 7868729 | STACKED DEVICE ASSEMBLY WITH INTEGRATED COIL AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7868795 | DATA CONVERSION CIRCUITRY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7868796 | DATA CONVERSION CIRCUITRY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7868877 | TOUCH PANEL DETECTION CIRCUITRY AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7869225 | SHIELDING STRUCTURES FOR SIGNAL PATHS IN ELECTRONIC DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7869558 | METHOD AND APPARATUS FOR CALIBRATING A COUNTING CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7869609 | BOUNDED SIGNAL MIXER AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7869784 | RADIO FREQUENCY CIRCUIT WITH INTEGRATED ON-CHIP RADIO FREQUENCY INDUCTIVE SIGNAL COUPLER |
| FREESCALE SEMICONDUCTOR, INC. | 7870400 | SYSTEM HAVING A MEMORY VOLTAGE CONTROLLER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7871854 | METHOD OF MAKING A VERTICAL PHOTODETECTOR |
| FREESCALE SEMICONDUCTOR, INC. | 7871886 | NANOCRYSTAL MEMORY WITH DIFFERENTIAL ENERGY BANDS AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7872311 | METHOD AND APPARATUS FOR MOBILITY ENHANCEMENT IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7872460 | METHOD FOR DETECTING OUTPUT SHORT CIRCUIT IN SWITCHING REGULATOR |
| FREESCALE SEMICONDUCTOR, INC. | 7872489 | RADIATION INDUCED FAULT ANALYSIS |
| FREESCALE SEMICONDUCTOR, INC. | 7872494 | MEMORY CONTROLLER CALIBRATION |
| FREESCALE SEMICONDUCTOR, INC. | 7873819 | BRANCH TARGET BUFFER ADDRESSING IN A DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 7876254 | DATA CONVERSION CIRCUITRY HAVING SUCCESSIVE APPROXIMATION CIRCUITRY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7877015 | OPTICAL TO RADIO FREQUENCY DETECTOR |
| FREESCALE SEMICONDUCTOR, INC. | 7879663 | TRENCH FORMATION IN A SEMICONDUCTOR MATERIAL |
| FREESCALE SEMICONDUCTOR, INC. | 7880457 | DUAL-LOOP DC-TO-DC CONVERTER APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 7880516 | METHOD FOR NOISE REDUCTION IN A PHASE LOCKED LOOP AND A DEVICE HAVING NOISE REDUCTION CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 7880550 | VOLTAGE TRANSLATION USING FEEDBACK TO ADJUST OUTPUT VOLTAGE RANGE |
| FREESCALE SEMICONDUCTOR, INC. | 7880650 | METHOD AND APPARATUS FOR TESTING DATA CONVERTER |
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| FREESCALE SEMICONDUCTOR, INC. | 7880653 | SWITCHED-CAPACITOR CIRCUITS, INTEGRATION SYSTEMS, AND METHODS OF OPERATION THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7880654 | CONTINUOUS-TIME SIGMA-DELTA MODULATOR WITH MULTIPLE FEEDBACK PATHS HAVING INDEPENDENT DELAYS |
| FREESCALE SEMICONDUCTOR, INC. | 7881813 | SYSTEM AND METHOD FOR SHARING RESET AND BACKGROUND COMMUNICATION ON A SINGLE MCU PIN |
| FREESCALE SEMICONDUCTOR, INC. | 7885174 | COMMON SIGNALING MODE FOR USE WITH MULTIPLE WIRELESS FORMATS |
| FREESCALE SEMICONDUCTOR, INC. | 7886609 | PRESSURE SENSOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7887235 | MULTIPLE SENSOR THERMAL MANAGEMENT FOR ELECTRONIC DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7887928 | COATED LEAD FRAME |
| FREESCALE SEMICONDUCTOR, INC. | 7888186 | METHOD FOR ASSEMBLING STACKABLE SEMICONDUCTOR PACKAGES |
| FREESCALE SEMICONDUCTOR, INC. | 7889523 | VARIABLE LOAD, VARIABLE OUTPUT CHARGE-BASED VOLTAGE MULTIPLIERS |
| FREESCALE SEMICONDUCTOR, INC. | 7892070 | PROCESS OF USING A POLISHING APPARATUS INCLUDING A PLATEN WINDOW AND A POLISHING PAD |
| FREESCALE SEMICONDUCTOR, INC. | 7892882 | METHODS AND APPARATUS FOR A SEMICONDUCTOR DEVICE PACKAGE WITH IMPROVED THERMAL PERFORMANCE |
| FREESCALE SEMICONDUCTOR, INC. | 7892907 | CMOS LATCH-UP IMMUNITY |
| FREESCALE SEMICONDUCTOR, INC. | 7892950 | METHODOLOGY FOR PROCESSING A PANEL DURING SEMICONDUCTOR DEVICE FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 7893491 | SEMICONDUCTOR SUPERJUNCTION STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7893696 | PULSE CIRCUIT USING A TRANSMISSION LINE |
| FREESCALE SEMICONDUCTOR, INC. | 7893741 | MULTIPLE-STAGE, SIGNAL EDGE ALIGNMENT APPARATUS AND METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 7894440 | PROGRAMMABLE HASH-TUPLE GENERATION WITH PARALLEL RULE IMPLEMENTATION INDEPENDENCE |
| FREESCALE SEMICONDUCTOR, INC. | 7895422 | SELECTIVE POSTPONEMENT OF BRANCH TARGET BUFFER (BTB) ALLOCATION |
| FREESCALE SEMICONDUCTOR, INC. | 7895427 | METHOD AND SYSTEM OF EXECUTING A SOFTWARE APPLICATION IN HIGHLY CONSTRAINED MEMORY SITUATION |
| FREESCALE SEMICONDUCTOR, INC. | 7898059 | SEMICONDUCTOR DEVICE COMPRISING PASSIVE COMPONENTS |
| FREESCALE SEMICONDUCTOR, INC. | 7898301 | ZERO INPUT CURRENT DRAIN COMPARATOR WITH HIGH ACCURACY TRIP POINT ABOVE SUPPLY VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7898323 | AMPLIFYING CIRCUIT WITH OFFSET COMPENSATION |
| FREESCALE SEMICONDUCTOR, INC. | 7898353 | CLOCK CONDITIONING CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7900183 | VENDOR INDEPENDENT METHOD TO MERGE COVERAGE RESULTS FOR DIFFERENT DESIGNS |
| FREESCALE SEMICONDUCTOR, INC. | 7900521 | EXPOSED PAD BACKSIDE PRESSURE SENSOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7901852 | METROLOGY OF BILAYER PHOTORESIST PROCESSES |
| FREESCALE SEMICONDUCTOR, INC. | 7902021 | METHOD FOR SEPARATELY OPTIMIZING SPACER WIDTH FOR TWO OR MORE TRANSISTOR CLASSES USING A RECESS SPACER INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | 7902022 | SELF-ALIGNED IN-LAID SPLIT GATE MEMORY AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 7902892 | METHOD OF CONTROL SLOPE REGULATION AND CONTROL SLOPE REGULATION APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 7902915 | METHOD AND CIRCUIT FOR CHARGING AND DISCHARGING A CIRCUIT NODE |
| FREESCALE SEMICONDUCTOR, INC. | 7903007 | METHOD AND APPARATUS FOR CONVERTING SIGNALS |
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| FREESCALE SEMICONDUCTOR, INC. | 7903483 | INTEGRATED CIRCUIT HAVING MEMORY WITH CONFIGURABLE READ/WRITE OPERATIONS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7903778 | A LOW POWER, HIGH RESOLUTION TIMING GENERATOR FOR ULTRA-WIDE BANDWIDTH COMMUNICATION SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 7904869 | METHOD OF AREA COMPACTION FOR INTEGRATED CIRCUIT LAYOUT DESIGN |
| FREESCALE SEMICONDUCTOR, INC. | 7907022 | PHASE-LOCKED LOOP AND METHOD FOR OPERATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7907072 | DIGITAL-TO-ANALOG CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 7907789 | REDUCTION OF BLOCK EFFECTS IN SPATIALLY RE-SAMPLED IMAGE INFORMATION FOR BLOCK-BASED IMAGE CODING |
| FREESCALE SEMICONDUCTOR, INC. | 7910441 | MULTI-GATE SEMICONDUCTOR DEVICE AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7910442 | PROCESS FOR MAKING A SEMICONDUCTOR DEVICE USING PARTIAL ETCHING |
| FREESCALE SEMICONDUCTOR, INC. | 7910482 | METHOD OF FORMING A FINFET AND STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7910991 | DUAL GATE LATERAL DIFFUSED MOS TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 7911002 | SEMICONDUCTOR DEVICE WITH SELECTIVELY MODULATED GATE WORK FUNCTION |
| FREESCALE SEMICONDUCTOR, INC. | 7911013 | SPACE AND PROCESS EFFICIENT MRAM |
| FREESCALE SEMICONDUCTOR, INC. | 7911750 | RESISTOR TRIGGERED ELECTROSTATIC DISCHARGE PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 7912119 | PER-SURVIVOR BASED ADAPTIVE EQUALIZER |
| FREESCALE SEMICONDUCTOR, INC. | 7912437 | RADIO FREQUENCY RECEIVER HAVING DYNAMIC BANDWIDTH CONTROL AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7915704 | SCHOTTKY DIODE |
| FREESCALE SEMICONDUCTOR, INC. | 7916053 | ANALOG-TO-DIGITAL CONVERSION MODULE ADAPTED FOR IRREGULAR SAMPLING SEQUENCES |
| FREESCALE SEMICONDUCTOR, INC. | 7916736 | SYSTEM AND METHOD FOR TRANSLUCENT BRIDGING |
| FREESCALE SEMICONDUCTOR, INC. | 7916796 | REGION CLUSTERING BASED ERROR CONCEALMENT FOR VIDEO DATA |
| FREESCALE SEMICONDUCTOR, INC. | 7917831 | OPTIMIZATION OF STORAGE DEVICE ACCESSES IN RAID SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 7917875 | CLOCK TREE ADJUSTABLE BUFFER |
| FREESCALE SEMICONDUCTOR, INC. | 7919006 | METHOD OF ANTI-STICTION DIMPLE FORMATION UNDER MEMS |
| FREESCALE SEMICONDUCTOR, INC. | 7919382 | VARACTOR STRUCTURE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7919388 | SEMICONDUCTOR DEVICES HAVING REDUCED GATE-DRAIN CAPACITANCE AND METHODS FOR THE FABRICATION THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7920987 | DEVICE UNDER TEST DE-EMBEDDING |
| FREESCALE SEMICONDUCTOR, INC. | 7923328 | SPLIT GATE NON-VOLATILE MEMORY CELL WITH IMPROVED ENDURANCE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7923369 | THROUGH-VIA AND METHOD OF FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 7923769 | SPLIT GATE NON-VOLATILE MEMORY CELL WITH IMPROVED ENDURANCE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7924061 | APPARATUS FOR DETECTING CLOCK FAILURE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7924108 | OSCILLATOR AMPLIFIER WITH INPUT CLOCK DETECTION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7924131 | ELECTRICAL COMPONENT HAVING AN INDUCTOR AND A METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7924925 | FLEXIBLE MACROBLOCK ORDERING WITH REDUCED DATA TRAFFIC AND |

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| FREESCALE SEMICONDUCTOR, INC. | 7925862 | COPROCESSOR FORWARDING LOAD AND STORE INSTRUCTIONS WITH DISPLACEMENT TO MAIN PROCESSOR FOR CACHE COHERENT EXECTUTION WHEN PROGRAM COUNTER VALUE FALLS WITHIN PREDETERMINED RANGES |
| FREESCALE SEMICONDUCTOR, INC. | 7927927 | SEMICONDUCTOR PACKAGE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7927934 | SOI SEMICONDUCTOR DEVICE WITH BODY CONTACT AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7927955 | ADJUSTABLE BIPOLAR TRANSISTORS FORMED USING A CMOS PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 7927956 | METHOD FOR MAKING A SEMICONDUCTOR STRUCTURE USING SILICON GERMANIUM |
| FREESCALE SEMICONDUCTOR, INC. | 7927989 | METHOD FOR FORMING A TRANSISTOR HAVING GATE DIELECTRIC PROTECTION AND STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 7928502 | TRANSISTOR DEVICES WITH NANO-CRYSTAL GATE STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | 7928706 | VOLTAGE REGULATOR DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7928753 | DEV ICE AND METHOD FOR EVALUATING ELECTROSTATIC DISCHARGE PROTECTION CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 7928788 | DOUBLE-BALANCED SINUSOIDAL MIXING PHASE INTERPOLATOR CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7929266 | ELECTRONIC DEVICE OPERABLE TO PROTECT A POWER TRANSISTOR WHEN USED IN CONJUNCTION WITH A TRANSFORMER |
| FREESCALE SEMICONDUCTOR, INC. | 7929650 | ACG FOR NARROWBAND RECEIVERS |
| FREESCALE SEMICONDUCTOR, INC. | 7930444 | DEVICE AND METHOD FOR CONTROLLING MULTIPLE DMA TASKS |
| FREESCALE SEMICONDUCTOR, INC. | 7930522 | METHOD FOR SPECULATIVE EXECUTION OF INSTRUCTIONS AND A DEVICE HAVING SPECULATIVE EXECUTION CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 7931190 | CIRCUIT AND METHOD FOR CORRELATED INPUTS TO A POPULATION COUNT CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7932145 | METHOD OF FORMING A BIPOLAR TRANSISTOR AND SEMICONDUCTOR COMPONENT THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7932175 | A METHOD TO FORM A VIA |
| FREESCALE SEMICONDUCTOR, INC. | 7932189 | ELECTRONIC DEVICE INCLUDING A LAYER OF DISCONTINUOUS STORAGE ELEMENTS AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7932731 | DEVICE AND METHOD FOR TESTING A NOISE IMMUNITY CHARACTERISTIC OF ANALOG CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 7933372 | SUCCESSIVE INTERFERENCE CANCELLATION BASED ON THE NUMBER OF RETRANSMISSIONS |
| FREESCALE SEMICONDUCTOR, INC. | 7935547 | METHOD OF PATTERNING A LAYER USING A PELLICLE |
| FREESCALE SEMICONDUCTOR, INC. | 7935571 | THROUGH SUBSTRATE VIAS FOR BACK-SIDE INTERCONNECTIONS ON VERY THIN SEMICONDUCTOR WAFERS |
| FREESCALE SEMICONDUCTOR, INC. | 7935607 | INTEGRATED PASSIVE DEVICE WITH A HIGH RESISTIVITY SUBSTRATE AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7935620 | LOW LEAKAGE SCHOTTKY CONTACT DEVICES AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7935631 | METHOD AND APPARATUS FOR FORMING A NOBLE METAL LAYER, NOTABLY ON INLAID METAL FEATURES |
| FREESCALE SEMICONDUCTOR, INC. | 7936200 | APPARATUS AND METHOD FOR PROVIDING A CLOCK SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 7936793 | METHODS AND APPARATUS FOR SYNCHRONIZING DATA TRANSFERRED ACROSS A MULTI-PIN ASYNCHRONOUS SERIAL INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | 7936921 | EFFICIENT FIXED-POINT REAL-TIME THRESHOLDING FOR SIGNAL PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 7937064 | WIRELESS TRANSCEIVER AND METHOD OF OPERATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7937573 | METRIC FOR SELECTIVE BRANCH TARGET BUFFER (BTB) ALLOCATION |
| FREESCALE SEMICONDUCTOR, INC. | 7938016 | MULTIPLE LAYER STRAIN GAUGE |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7939412 | ELECTRONIC DEVICE INCLUDING A FIN-TYPE TRANSISTOR STRUCTURE AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7939482 | CLEANING SOLUTION FOR A SEMICONDUCTOR WAFER |
| FREESCALE SEMICONDUCTOR, INC. | 7939880 | SPLIT GATE NON-VOLATILE MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | 7940059 | METHOD FOR TESTING H-BRIDGE |
| FREESCALE SEMICONDUCTOR, INC. | 7940084 | DEVICE AND METHOD FOR SHARING CHARGE |
| FREESCALE SEMICONDUCTOR, INC. | 7940092 | GATE DRIVER CIRCUIT FOR H BRIDGE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7940332 | SIGNAL DETECTION DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7940513 | SWITCH ARRANGEMENT, INTEGRATED CIRCUIT, ACTIVATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7940545 | LOW POWER READ SCHEME FOR READ ONLY MEMORY (ROM) |
| FREESCALE SEMICONDUCTOR, INC. | 7940599 | DUAL PORT MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7941110 | RF CIRCUIT WITH CONTROL UNIT TO REDUCE SIGNAL POWER UNDER APPROPRIATE CONDITIONS |
| FREESCALE SEMICONDUCTOR, INC. | 7941594 | SDRAM SHARING USING A CONTROL SURROGATE |
| FREESCALE SEMICONDUCTOR, INC. | 7941646 | COMPLETION CONTINUE ON THREAD SWITCH MECHANISM FOR A MICROPROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 7941716 | METHOD FOR RACE PREVENTION AND A DEVICE HAVING RACE PREVENTION CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 7941718 | ELECTRONIC DEVICE TESTING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7941721 | SYSTEM AND A METHOD FOR TESTING CONNECTIVITY BETWEEN A FIRST DEVICE AND A SECOND DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7943525 | MICROELECTROMECHANICAL DEVICE WITH ISOLATED MICROSTRUCTURES AND METHOD OF PRODUCING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 7943988 | POWER MOSFET WITH A GATE STRUCTURE OF DIFFERENT MATERIAL |
| FREESCALE SEMICONDUCTOR, INC. | 7944969 | METHOD AND SYSTEM FOR SAMPLING VIDEO DATA |
| FREESCALE SEMICONDUCTOR, INC. | 7945418 | STREAM BASED STIMULUS DEFINITION AND DELIVERY VIA INTERWORKING |
| FREESCALE SEMICONDUCTOR, INC. | 7948244 | CAPACITIVE SENSORS AND METHODS FOR REDUCING NOISE THEREIN |
| FREESCALE SEMICONDUCTOR, INC. | 7948301 | CHARGE PUMP WITH CHARGE FEEDBACK AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7948302 | REGULATOR HAVING INTERLEAVED LATCHES |
| FREESCALE SEMICONDUCTOR, INC. | 7948607 | IMMERSION LITHOGRAPHY APPARATUS AND METHOD OF PERFORMING IMMERSION LITHOGRAPHY |
| FREESCALE SEMICONDUCTOR, INC. | 7948803 | A NON-VOLATILE MEMORY DEVICE AND PROGRAMMABLE VOLTAGE REFERENCE FOR A NON-VOLATILE MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7949073 | DUAL-MODE SYSTEM AND METHOD FOR RECEIVING WIRELESS SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 7950144 | METHOD FOR CONTROLLING WARPAGE IN REDISTRIBUTED CHIP PACKAGING PANELS |
| FREESCALE SEMICONDUCTOR, INC. | 7951695 | METHOD FOR REDUCING PLASMA DISCHARGE DAMAGE DURING PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 7952401 | STANDBY CONTROL CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7952937 | A WORLDWIDE DRIVER FOR A NON-VOLATILE MEMORY DEVICE, A NON-VOLATILE MEMORY DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7955877 | A METHOD FOR SIMULATING LONG-TERM PERFORMANCE OF A NON-VOLATILE MEMORY BY EXPOSING THE NON-VOLATILE MEMORY TO HEAVY-ION RADIATION |

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7955929 | SEMICONDUCTOR DEVICE AND METHOD OF FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7955953 | METHOD OF FORMING STACKED DIE PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 7955973 | METHOD AND APPARATUS FOR IMPROVEMENTS IN CHIP MANUFACTURE AND DESIGN |
| FREESCALE SEMICONDUCTOR, INC. | 7956400 | MIM CAPACITOR INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | 7956471 | MOLD AND SUBSTRATE FOR USE WITH MOLD |
| FREESCALE SEMICONDUCTOR, INC. | 7956594 | DEVICE AND METHOD FOR COMPENSATING FOR VOLTAGE DROPS |
| FREESCALE SEMICONDUCTOR, INC. | 7956662 | FLIP-FLOP CIRCUIT WITH INTERNAL LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | 7956679 | DIFFERENTIAL AMPLIFIER WITH OFFSET VOLTAGE TRIMMING |
| FREESCALE SEMICONDUCTOR, INC. | 7956781 | ANALOGUE-TO-DIGITAL CONVERTER APPARATUS AND METHOD OF REUSING AN ANALOGUE-TO-DIGITAL CONVERTER CICRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7957190 | MEMORY HAVING P-TYPE SPLIT GATE MEMORY CELLS AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7957218 | MEMORY CONTROLLER WITH SKEW CONTROL AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7957707 | SYSTEMS, APPARATUS AND METHODS FOR PERFORMING DIGITAL PRE- DISTORTION BASED ON LOOKUP TABLE GAIN VALUES |
| FREESCALE SEMICONDUCTOR, INC. | 7957716 | BASEBAND FILTERS FOR USE IN WIRELESS COMMUNICATION DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 7958173 | POPULATION COUNT APPROXIMATION CIRCUIT AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7958281 | METHOD AND APPARATUS FOR TRANSMITTING DATA IN A FLEXRAY NODE |
| FREESCALE SEMICONDUCTOR, INC. | 7958401 | DEBUG TRACE MESSAGING WITH ONE OR MORE CHARACTERISTIC INDICATORS |
| FREESCALE SEMICONDUCTOR, INC. | 7960243 | METHOD OF FORMING A SEMICONDUCTOR DEVICE FEATURING A GATE STRESSOR AND SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7960267 | METHOD FOR MAKING A STRESSED NON-VOLATILE MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7960814 | STRESS RELIEF OF A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7960983 | CIRCUIT FOR DETECTING BONDING DEFECT IN MULTI-BONDING WIRE |
| FREESCALE SEMICONDUCTOR, INC. | 7961063 | BALUN SIGNAL TRANSFORMER AND METHOD OF FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 7962718 | METHODS FOR PERFORMING EXTENDED TABLE LOOKUPS |
| FREESCALE SEMICONDUCTOR, INC. | 7962805 | SYSTEM AND METHOD FOR PREVENTING A RACE CONDITION |
| FREESCALE SEMICONDUCTOR, INC. | 7962868 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE USING OPTICAL PROXIMITY CORRECTION FOR THE OPTICAL LITHOGRAPHY |
| FREESCALE SEMICONDUCTOR, INC. | 7964502 | MULTILAYERED THROUGH VIA |
| FREESCALE SEMICONDUCTOR, INC. | 7965117 | CHARGE PUMP FOR PHASE LOCKED LOOP |
| FREESCALE SEMICONDUCTOR, INC. | 7965119 | DEVICE AND METHOD FOR HADLING METASTABLE SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 7965125 | CURRENT DRIVE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7965129 | TEMPERATURE COMPENSATED CURRENT REFERENCE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7965130 | LOW POWER CHARGE PUMP AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7966529 | SYSTEM AND METHOD FOR TESTING MEMORY BLOCKS IN AN SOC DESIGN |
| FREESCALE SEMICONDUCTOR, INC. | 7968394 | TRANSISTOR WITH IMMERSED CONTACTS AND METHODS OF FORMING |

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| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7969026 | FLEXIBLE CARRIER FOR HIGH VOLUME ELECTRONIC PACKAGE FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 7969164 | METHOD AND APPARATUS FOR MINI MODULE EMI SHIELDING EVALUATION |
| FREESCALE SEMICONDUCTOR, INC. | 7969167 | CAPACITANCE-TO-VOLTAGE INTERFACE CIRCUIT WITH SHARED CAPACITOR BANK FOR OFFSETTING AND ANALOG-TO-DIGITAL CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | 7969179 | METHOD AND APPARATUS FOR INCREASING SECURITY IN A SYSTEM USING AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7969181 | DEVICE AND METHOD FOR ADJUSTING AN IMPEDANCE OF AN OUTPUT DRIVER OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7969196 | CIRCUITS AND METHODS FOR BUFFERING AND COMMUNICATING DATA SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 7969339 | ELECTRONIC DEVICE AND INTEGRATED CIRCUIT COMPRISING A DELTA- SIGMA CONVERTER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7970087 | EYE CENTER DETERMINATION SYSTEM AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7970128 | SYSTEMS AND METHODS FOR EFFICIENT GENERATION OF HASH VALUES OF VARYING BIT WIDTHS |
| FREESCALE SEMICONDUCTOR, INC. | 7971082 | METHOD AND SYSTEM FOR ESTIMATING POWER CONSUMPTION OF INTEGRATED CIRCUIT DESIGN |
| FREESCALE SEMICONDUCTOR, INC. | 7971105 | DEVICE AND METHOD FOR DETECTING AND CORRECTING TIMING ERRORS |
| FREESCALE SEMICONDUCTOR, INC. | 7972913 | METHOD FOR FORMING A SCHOTTKY DIODE |
| FREESCALE SEMICONDUCTOR, INC. | 7972922 | METHOD OF FORMING A SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 7973392 | ELECTRONIC DEVICE AND METHOD FOR MANUFACTURING STRUCTURE FOR ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7973545 | TIME RESOLVED RADIATION ASSISTED DEVICE ALTERATION |
| FREESCALE SEMICONDUCTOR, INC. | 7973570 | SAMPLE-AND-HOLD (S/H) CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | | POWER SWITCH CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7975120 | DYNAMIC ALLOCATION OF MESSAGE BUFFERS |
| FREESCALE SEMICONDUCTOR, INC. | 7975183 | DYNAMIC DEBUGGING OF PLATFORM TRANSACTIONS VIA CONTEXT AWARE TRANSACTIONAL DEBUG MARKING |
| FREESCALE SEMICONDUCTOR, INC. | 7975307 | SECURING PROPRIETARY FUNCTIONS FROM SCAN ACCESS |
| FREESCALE SEMICONDUCTOR, INC. | 7977241 | METHOD FOR FABRICATING HIGHLY RELIABLE INTERCONNECTS |
| FREESCALE SEMICONDUCTOR, INC. | 7977785 | ELECTRONIC DEVICE AND METHOD OF PACKAGING AN ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 7977948 | SENSOR DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 7977983 | A DEVICE HAVING SYNCHRONIZING CAPABILITIES AND A METHOD FOR SYNCHRONIZING |
| FREESCALE SEMICONDUCTOR, INC. | 7978757 | CONFIGURABLE RECEIVER AND A METHOD FOR CONFIGURING A RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 7978793 | METHOD FOR GENERATING SOFT DECISION SIGNAL FROM HARD DECISION SIGNAL IN A RECEIVER SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7978796 | RECOVERING SYMBOLS IN A COMMUNICATION RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 7981730 | INTEGRATED CONFORMAL SHIELDING METHOD AND PROCESS USING REDISTRIBUTED CHIP PACKAGING |
| FREESCALE SEMICONDUCTOR, INC. | 7981808 | METHOD OF FORMING A GATE DIELECTRIC BY IN-SITU PLASMA |
| FREESCALE SEMICONDUCTOR, INC. | 7982247 | TRANSISTOR WITH GAIN VARIATION COMPENSATION |
| FREESCALE SEMICONDUCTOR, INC. | 7982282 | HIGH EFFICIENCY AMPLIFIER WITH REDUCED PARASITIC CAPACITANCE |
| FREESCALE SEMICONDUCTOR, INC. | 7982521 | DEVICE AND SYSTEM FOR REDUCING NOISE INDUCED ERRORS |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 7982542 | POWER TRANSISTOR FEEDBACK CIRCUIT WITH NOISE AND OFFSET COMPENSATION |
| FREESCALE SEMICONDUCTOR, INC. | 7982800 | VIDEO DE-INTERLACER USING MOTION RESIDUE COMPENSATION |
| FREESCALE SEMICONDUCTOR, INC. | 7983371 | SYSTEM AND METHOD FOR USING PROGRAMMABLE FREQUENCY OFFSETS IN A DATA NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 7984210 | METHOD FOR TRANSMITTING A DATUM FROM A TIME-DEPENDENT DATA STORAGE MEANS |
| FREESCALE SEMICONDUCTOR, INC. | 7984229 | PIPELINED TAG AND INFORMATION ARRAY ACCESS WITH SPECULATIVE RETRIEVAL OF TAG THAT CORRESPONDS TO INFORMATION ACCESS |
| FREESCALE SEMICONDUCTOR, INC. | 7984336 | METHOD AND SYSTEM FOR STORING DATA FROM A PLURALITY OF PROCESSORS |
| FREESCALE SEMICONDUCTOR, INC. | 7984655 | ENTRAPMENT DETECTION AND PREVENTION DEVICE FOR OPENING/CLOSING MECHANISM |
| FREESCALE SEMICONDUCTOR, INC. | 7985122 | METHOD OF POLISHING A LAYER USING A POLISHING PAD |
| FREESCALE SEMICONDUCTOR, INC. | 7985649 | METHOD OF MAKING A SEMICONDUCTOR STRUCTURE USEFUL IN MAKING A SPLIT GATE NON-VOLATILE MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | 7985655 | THROUGH-VIA AND METHOD OF FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 7985659 | SEMICONDUCTOR DEVICE WITH A CONTROLLED CAVITY AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7985672 | SOLDER BALL ATTACHMENT RING AND METHOD OF USE |
| FREESCALE SEMICONDUCTOR, INC. | 7986006 | SINGLE TRANSISTOR MEMORY CELL WITH REDUCED RECOMBINATION RATES |
| FREESCALE SEMICONDUCTOR, INC. | 7986166 | CLOCK BUFFER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 7986172 | SWITCHING CIRCUIT WITH GATE DRIVER HAVING PRECHARGE PERIOD AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7986189 | AMPLIFIER WITH FEEDBACK |
| FREESCALE SEMICONDUCTOR, INC. | 7986252 | SYSTEM AND METHOD FOR REMOVING GLITCHES FROM A BIT STREAM |
| FREESCALE SEMICONDUCTOR, INC. | 7987322 | SNOOP REQUEST MANAGEMENT IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7989347 | PROCESS FOR FILLING RECESSED FEATURES IN A DIELECTRIC SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 7989951 | DIE ASSEMBLIES |
| FREESCALE SEMICONDUCTOR, INC. | 7989965 | UNDERFILL DISPENSING SYSTEM FOR INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 7990795 | DYNAMIC RANDOM ACCESS MEMORY (DRAM) REFRESH |
| FREESCALE SEMICONDUCTOR, INC. | 7991921 | SYSTEM AND METHOD FOR REDUCING POWER CONSUMPTION OF MEMORY IN AN I/O CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | 7993971 | FORMING A 3-D SEMICONDUCTOR DIE STRUCTURE WITH AN INTERMETALLIC FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 7994069 | SEMICONDUCTOR WAFER WITH LOW-K DIELECTRIC LAYER AND PROCESS FOR FABRICATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 7994766 | DIFFERENTIAL CURRENT SENSOR DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 7995607 | ARBITER FOR A SERIAL BUS SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 7998822 | SEMICONDUCTOR FABRICATION PROCESS INCLUDING SILICIDE STRINGER REMOVAL PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 7998852 | RF DEVICE AND METHOD WITH TRENCH UNDER BOND PAD FEATURE |
| FREESCALE SEMICONDUCTOR, INC. | 7999581 | A SYSTEM AND A METHOD FOR PROVIDING AN OUTPUT CLOCK SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 7999601 | CHARGE PUMP AND CONTROL SCHEME |
| EDEECCALE CELUCONDUCTOR TO | 50005 00 | CONTRACTOR TO CE DATE OF THE CENTER AND THE PROPERTY OF THE CENTER AND THE CENTER |

7999709 CONTINUOUS-TIME IMAGE-REJECT FILTER WITH DISCRETE-TIME-FEEDBACK

FREESCALE SEMICONDUCTOR, INC.

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8000408 | LOOP DELAY AND GAIN CONTROL METHODS IN CLOSED-LOOP TRANSMITTERS AND WIRELESS DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 8000821 | AUDIO COMMUNICATION UNIT AND INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8001309 | METHOD AND SYSTEM OF GROUPING INTERRUPTS FROM A TIME-DEPENDENT DATA STORAGE MEANS |
| FREESCALE SEMICONDUCTOR, INC. | 8001430 | DEVICE AND METHOD FOR CONTROLLING AN EXECUTION OF A DMA TASK |
| FREESCALE SEMICONDUCTOR, INC. | 8001591 | DISTRIBUTED RESOURCE ACCESS PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 8001602 | DATA SCAN MECHANISM |
| FREESCALE SEMICONDUCTOR, INC. | 8003517 | A METHOD FOR FORMING INTERCONNECTS FOR 3-D APPLICATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 8003539 | INTEGRATED ASSIST FEATURES FOR EPITAXIAL GROWTH |
| FREESCALE SEMICONDUCTOR, INC. | 8004068 | SHIELDED MULTI-LAYER PACKAGE STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | 8004069 | IMPROVEMENTS IN OR RELATING TO LEAD FRAME BASED SEMICONDUCTOR PACKAGE AND A METHOD OF MANUFACTURING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8004080 | EDGE MOUNTED INTEGRATED CIRCUITS WITH HEAT SINK |
| FREESCALE SEMICONDUCTOR, INC. | 8004207 | LED DRIVER WITH PRECHARGE AND TRACK/HOLD |
| FREESCALE SEMICONDUCTOR, INC. | 8004319 | PROGRAMMABLE CLOCK DIVIDER |
| FREESCALE SEMICONDUCTOR, INC. | 8004367 | VCO CONTROL AND METHODS THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8004907 | SRAM WITH READ AND WRITE ASSIST |
| FREESCALE SEMICONDUCTOR, INC. | 8006015 | DEVICE AND METHOD FOR MANAGING ACCESS REQUESTS |
| FREESCALE SEMICONDUCTOR, INC. | 8006113 | SYSTEM AND METHOD FOR CONTROLLING VOLTAGE LEVEL AND CLOCK FREQUENCY SUPPLIED TO A SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8006141 | METHOD FOR SPEEDING UP SERIAL DATA TOLERANCE TESTING |
| FREESCALE SEMICONDUCTOR, INC. | 8008786 | DYNAMIC PAD SIZE TO REDUCE SOLDER FATIGUE |
| FREESCALE SEMICONDUCTOR, INC. | 8008934 | BURN-IN SYSTEM FOR ELECTRONIC DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 8008935 | TESTER AND A METHOD FOR TESTING AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8008964 | VARIABLE INPUT VOLTAGE CHARGE PUMP |
| FREESCALE SEMICONDUCTOR, INC. | 8009397 | METHOD AND CIRCUIT FOR EFUSE PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 8009489 | MEMORY WITH READ CYCLE WRITE BACK |
| FREESCALE SEMICONDUCTOR, INC. | 8009658 | METHOD FOR SHARING BANDWIDTH USING REDUCED DUTY CYCLE SIGNALS AND MEDIA ACCESS CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 8009673 | A METHOD AND DEVICE FOR PROCESSING FRAMES |
| FREESCALE SEMICONDUCTOR, INC. | 8009744 | TWISTED PAIR COMMUNICATION SYSTEM, APPARATUS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8010074 | MIXER CIRCUITS FOR SECOND ORDER INTERCEPT POINT CALIBRATION |
| FREESCALE SEMICONDUCTOR, INC. | 8010077 | DC OFFSET CALIBRATION IN A DIRECT CONVERSION RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 8010854 | METHOD AND CIRCUIT FOR BROWNOUT DETECTION IN A MEMORY SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8012799 | METHOD OF ASSEMBLING SEMICONDUCTOR DEVICE WITH HEAT SPREADER |
| FREESCALE SEMICONDUCTOR, INC. | 8014457 | METHOD OF PROVIDING A DATA SIGNAL FOR CHANNEL ESTIMATION AND CIRCUIT THEREOF |

| <u>Owner</u> | Patent # | Description |
|-------------------------------|----------|---|
| FREESCALE SEMICONDUCTOR, INC. | 8014682 | FREE-SPACE OPTICAL COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8014737 | POWER CONTROL SYSTEM FOR A WIRELESS COMMUNICATION UNIT |
| FREESCALE SEMICONDUCTOR, INC. | 8015470 | APPARATUS AND METHOD FOR DECODING BURSTS OF CODED INFORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 8016183 | ADJUSTABLE CLAMP SYSTEM AND METHOD FOR WIRE BONDING DIE ASSEMBLY |
| FREESCALE SEMICONDUCTOR, INC. | 8017469 | DUAL HIGH-K OXIDES WITH SIGE CHANNEL |
| FREESCALE SEMICONDUCTOR, INC. | 8017474 | PROCESS OF FORMING AN ELECTRONIC DEVICE INCLUDING A RESISTOR-CAPACITOR FILTER |
| FREESCALE SEMICONDUCTOR, INC. | 8017497 | METHOD FOR MANUFACTURING SEMICONDUCTOR |
| FREESCALE SEMICONDUCTOR, INC. | 8018018 | A TEMPERATURE SENSING DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8018197 | VOLTAGE REFERENCE DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 8018200 | CONTROL APARATUS AND METHOD OF REGULATING POWER |
| FREESCALE SEMICONDUCTOR, INC. | 8018247 | APPARATUS FOR REDUCING POWER CONSUMPTION USING SELECTIVE POWER GATING |
| FREESCALE SEMICONDUCTOR, INC. | 8018259 | PHASE-LOCKED LOOP HAVING A FEEDBACK CLOCK DETECTOR CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8020014 | METHOD FOR POWER REDUCTION AND A DEVICE HAVING POWER REDUCTION CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 8020017 | MANAGEMENT OF POWER DOMAINS IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8020067 | APPARATUS AND METHOD FOR DETECTING AN END POINT OF AN INFORMATION FRAME |
| FREESCALE SEMICONDUCTOR, INC. | 8020443 | TRANSDUCER WITH DECOUPLED SENSING IN MUTUALLY ORTHOGONAL DIRECTIONS |
| FREESCALE SEMICONDUCTOR, INC. | 8021926 | SEMICONDUCTOR DEVICE WITH LOW RESISTANCE BACK-SIDE COUPLING |
| FREESCALE SEMICONDUCTOR, INC. | 8021957 | PROCESS OF FORMING AN ELECTRONIC DEVICE INCLUDING INSULATING LAYERS HAVING DIFFERENT STRAINS |
| FREESCALE SEMICONDUCTOR, INC. | 8021970 | METHOD OF ANNEALING A DIELECTRIC LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 8022505 | SEMICONDUCTOR DEVICE STRUCTURE AND INTEGRATED CIRCUIT THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8022507 | VARACTOR DIODES |
| FREESCALE SEMICONDUCTOR, INC. | 8022850 | MULTIPLE-BIT, DIGITALTO-ANALOG CONVERTERS AND CONVERSION METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 8023457 | FEEDBACK REDUCTION FOR MIMO PRECODED SYSTEM BY EXPLOITING CHANNEL CORRELATION |
| FREESCALE SEMICONDUCTOR, INC. | 8024620 | DYNAMIC ADDRESS-TYPE SELECTION CONTROL IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8026700 | DC TO DC CONVERTER HAVING SWITCH CONTROL AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 8026760 | GAIN ENHANCED SWITCHED CAPACITOR CIRCUIT AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 8028178 | ADAPTIVE FEEDBACK AND POWER CONTROL FOR USB DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 8030153 | HIGH VOLTAGE TMOS SEMICONDUCTOR DEVICE WITH LOW GATE CHARGE STRUCTURE AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 8030173 | SILICON NITRIDE HARDSTOP ENCAPSULATION LAYER FOR STI REGION |
| FREESCALE SEMICONDUCTOR, INC. | 8030220 | PLASMA TREATMENT OF A SEMICONDUCTOR SURFACE FOR ENHANCED NUCLEATION OF A METAL-CONTAINING LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 8030763 | SEMICONDUCTOR PACKAGE WITH REDUCED INDUCTIVE COUPLING BETWEEN ADJACENT BONDWIRE ARRAYS |
| FREESCALE SEMICONDUCTOR, INC. | 8030953 | DEVICE AND METHOD FOR TESTING INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 8030983 | COMMON MODE TRACKING RECEIVER |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8030986 | POWER TRANSISTOR WITH TURN OFF CONTROL AND METHOD FOR OPERATING |
| FREESCALE SEMICONDUCTOR, INC. | 8031549 | INTEGRATED CIRCUIT HAVING BOOSTED ARRAY VOLTAGE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8032030 | MULTIPLE CORE SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8035156 | SPLIT-GATE NON-VOLATILE MEMORY CELL AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 8035314 | METHOD AND DEVICE FOR LED CHANNEL MANAGEMENT IN LED DRIVER |
| FREESCALE SEMICONDUCTOR, INC. | 8035315 | LED DRIVER WITH FEEDBACK CALIBRATION |
| FREESCALE SEMICONDUCTOR, INC. | 8035448 | DIFFERENTIAL AMPLIFIER THAT COMPENSATES FOR PROCESS VARIATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 8035943 | PROTECTION CIRCUIT APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 8036260 | SYSTEM AND METHOD FOR EQUALIZING AN INCOMING SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 8036312 | SYSTEM AND METHOD FOR DETERMINING SIGNAL PHASE |
| FREESCALE SEMICONDUCTOR, INC. | 8039312 | METHOD FOR FORMING A CAPPED MICRO-ELECTRO-MECHANICAL SYSTEM (MEMS) DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8039339 | SEPARATE LAYER FORMATION IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8039341 | SELECTIVE UNIAXIAL STRESS MODIFICATION FOR USE WITH STRAINED SILICON ON INSULATOR INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8039386 | METHOD FOR FORMING A THROUGH SILICON VIA (TSV) |
| FREESCALE SEMICONDUCTOR, INC. | 8040079 | PEAK DETECTION WITH DIGITAL CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | 8040143 | CAPACITANCE SENSING WITH MISMATCH COMPENSATION |
| FREESCALE SEMICONDUCTOR, INC. | 8040643 | POWER SUPPLY SWITCHING APPARATUS WITH SEVERE OVERLOAD DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | 8040700 | CHARGE PUMP FOR USE WITH A SYNCHRONOUS LOAD |
| FREESCALE SEMICONDUCTOR, INC. | 8040746 | EFFICIENT WORD LINES, BIT LINE AND PRECHARGE TRACKING IN SELF-TIMED MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8041132 | SYSTEM AND METHOD FOR LOAD BALANCING A VIDEO SIGNAL IN A MULTI-CORE PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 8041899 | SYSTEM AND METHOD FOR FETCHING INFORMATION TO A CACHE MODULE USING A WRITE BACK ALLOCATE ALGORITHM |
| FREESCALE SEMICONDUCTOR, INC. | 8041901 | PERFORMANCE MONITORING DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 8042002 | METHOD AND APPARATUS FOR HANDLING SHARED HARDWARE AND SOFTWARE DEBUG RESOURCE EVENTS IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8042071 | CIRCUIT AND METHOD FOR AVOIDING SOFT ERRORS IN STORAGE DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 8043888 | PHASE CHANGE MEMORY CELL WITH HEATER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8043951 | METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE OBTAINABLE THEREWITH |
| FREESCALE SEMICONDUCTOR, INC. | 8044494 | STACKABLE MOLDED PACKAGES AND METHODS OF MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8044837 | ANALOGUE TO DIGITAL CONVERTERS |
| FREESCALE SEMICONDUCTOR, INC. | 8045943 | HIGH PERFORMANCE CMOS RADIO FREQUENCY RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 8046567 | MULTI-THREADED PROCESSOR ARCHITECTURE |
| FREESCALE SEMICONDUCTOR, INC. | 8048738 | METHOD FOR FORMING A SPLIT GATE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8049299 | ANTIFUSES WITH CURVED BREAKDOWN REGIONS |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8049313 | HEAT SPREADER FOR SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 8049439 | LED DRIVER WITH DYNAMIC HEADROOM CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 8049549 | DELTA PHI GENERATOR WITH START-UP CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8049550 | METHOD FOR POWER REDUCTION AND A DEVICE HAVING POWER REDUCTION CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 8050048 | LEAD FRAME WITH SOLDER FLOW CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 8050179 | METHOD AND SYSTEM FOR ACKNOWLEDGING FRAMES IN A COMMMUNICATION NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 8050371 | METHOD AND SYSTEM FOR COMPENSATING FOR THE EFFECT OF PHASE DRIFT IN A DATA SAMPLING CLOCK |
| FREESCALE SEMICONDUCTOR, INC. | 8050904 | SYSTEM AND METHOD FOR CIRCUIT SYMBOLIC TIMING ANALYSIS OF CIRCUIT DESIGNS |
| FREESCALE SEMICONDUCTOR, INC. | 8051226 | CIRCULAR BUFFER SUPPORT IN A SINGLE INSTRUCTION MULTIPLE DATA (SIMD) DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 8053866 | VARACTOR STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | 8056415 | SEMICONDUCTOR DEVICE WITH REDUCED SENSITIVITY TO PACKAGE STRESS |
| FREESCALE SEMICONDUCTOR, INC. | 8058143 | SUBSTRATE BONDING WITH METAL GERMANIUM SILICON MATERIAL |
| FREESCALE SEMICONDUCTOR, INC. | 8059380 | PACKAGE LEVEL ESD PROTECTION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8059482 | MEMORY USING MULTIPLE SUPPLY VOLTAGES |
| FREESCALE SEMICONDUCTOR, INC. | 8060043 | ADAPTIVE IIP2 CALIBRATION |
| FREESCALE SEMICONDUCTOR, INC. | 8060324 | DEVICE AND A METHOD FOR ESTIMATING TRANSISTOR PARAMETER VARIATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 8060654 | NETWORK AND METHOD FOR SETTING A TIME-BASE OF A NODE IN THE NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 8060724 | PROVISION OF EXTENDED ADDRESSING MODES IN A SINGLE INSTRUCTION MULTIPLE DATA (SIMD) DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 8060770 | METHOD AND SYSTEM FOR CLOCK SKEW REDUCTION IN CLOCK TREES |
| FREESCALE SEMICONDUCTOR, INC. | 8061185 | METHOD FOR TESTING A SLURRY USED TO FORM A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8062424 | METHOD AND APPARATUS FOR MOLDING SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 8062953 | SEMICONDUCTOR DEVICES WITH EXTENDED ACTIVE REGIONS |
| FREESCALE SEMICONDUCTOR, INC. | 8062975 | THROUGH SUBSTRATE VIAS |
| FREESCALE SEMICONDUCTOR, INC. | 8063402 | INTEGRATED CIRCUIT HAVING A FILLER STANDARD CELL |
| FREESCALE SEMICONDUCTOR, INC. | 8063624 | HIGH SIDE HIGH VOLTAGE SWITCH WITH OVER CURRENT AND OVER VOLTAGE PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 8063678 | CHARGE PUMP FOR PHASE LOCKED LOOP |
| FREESCALE SEMICONDUCTOR, INC. | 8063685 | PUSLED FLIP-FLOP CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8063710 | SELF-CALIBRATING OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | 8063810 | UNFOLDING VCO-BASED QUANTIZATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8064329 | CONTROL AND DATA INFORMATION COMMUNICATION IN A WIRELESS SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8065646 | METHOD AND A COMPUTER READABLE MEDIUM FOR PERFORMING STATIC TIMING ANALYSIS OF A DESIGN OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8068574 | SYSTEMS, APPARATUS, AND METHODS FOR PERFORMING DIGITAL PRE- DISTORTION WITH FEEDBACK SIGNAL ADJUSTMENT |

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| FREESCALE SEMICONDUCTOR, INC. | 8068795 | RF MULTIBAND TRANSMITTER WITH BALUN |
| FREESCALE SEMICONDUCTOR, INC. | 8070357 | DEVICE AND METHOD FOR EVALUATING A TEMPERATURE |
| FREESCALE SEMICONDUCTOR, INC. | 8071459 | METHOD OF SEALING AN AIR GAP IN A LAYER OF A SEMICONDUCTOR STRUCTURE AND SEMICONDUCTOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 8071461 | LOW LOSS SUBSTRATE FOR INTEGRATED PASSIVE DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 8072062 | CIRCUIT DEVICE WITH AT LEAST PARTIAL PACKAGING AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 8073078 | SPLIT CHANNEL RECEIVER WITH VERY LOW SECOND ORDER INTERMODULATION |
| FREESCALE SEMICONDUCTOR, INC. | 8074195 | SYSTEM AND METHOD FOR EVALUATING A DYNAMIC POWER CONSUMPTION OF A BLOCK |
| FREESCALE SEMICONDUCTOR, INC. | 8076189 | METHOD OF FORMING A SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8076979 | LOCK DETECTION CIRCUIT FOR PHASE LOCKED LOOP |
| FREESCALE SEMICONDUCTOR, INC. | 8076981 | SELF-CALIBRATING OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | 8077063 | METHOD AND SYSTEM FOR DETERMINING BIT STREAM ZONE STATISTICS |
| FREESCALE SEMICONDUCTOR, INC. | 8077521 | BITLINE CURRENT GENERATOR FOR A NON-VOLATILE MEMORY ARRAY AND A NON-VOLATILE MEMORY ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | 8077533 | MEMORY AND METHOD FOR SENSING DATA IN A MEMORY USING COMPLEMENTARY SENSING SCHEME |
| FREESCALE SEMICONDUCTOR, INC. | 8077698 | METHOD AND DEVICE FOR FRAME AND SLOT SYNCHRONIZATION |
| FREESCALE SEMICONDUCTOR, INC. | 8077775 | SYSTEMS AND METHOD OF ADAPTIVE RATE CONTROL FOR A VIDEO ENCODER |
| FREESCALE SEMICONDUCTOR, INC. | 8077803 | QUARTER DUTY CYCLE PULSE GENERATOR FOR INTERLEAVED SWITCHING MIXER |
| FREESCALE SEMICONDUCTOR, INC. | 8077816 | FAST PREDICTIVE AUTOMATIC GAIN CONTROL FOR DYNAMIC RANGE REDUCTION IN WIRELESS COMMUNICATION RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 8077839 | HANDHELD DEVICE FOR DIALING OF PHONE NUMBERS EXTRACTED FROM A VOICEMAIL |
| FREESCALE SEMICONDUCTOR, INC. | 8078353 | SELF MONITORING BRAKING SYSTEM FOR VEHICLES |
| FREESCALE SEMICONDUCTOR, INC. | 8078781 | DEVICE HAVING PRIORITY UPGRADE MECHANISM CAPABILITIES AND A METHOD FOR UPDATING PRIORITIES |
| FREESCALE SEMICONDUCTOR, INC. | 8078845 | DEVICE AND METHOD FOR PROCESSING INSTRUCTIONS BASED ON MASKED REGISTER GROUP SIZE INFORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 8080439 | METHOD OF MAKING A VERTICAL PHASE CHANGE MEMORY (PCM) AND A PCM DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8080444 | METHOD FOR FORMING A PACKAGED SEMICONDUCTOR DEVICE HAVING A GROUND PLANE |
| FREESCALE SEMICONDUCTOR, INC. | 8080448 | SEMICONDUCTOR DEVICE WITH NESTED ROWS OF CONTACTS |
| FREESCALE SEMICONDUCTOR, INC. | 8081026 | METHOD FOR SUPPLYING AN OUTPUT SUPPLY VOLTAGE TO A POWER GATED CIRCUIT AND AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8082789 | MATCHED MULTIPLIER CIRCUIT HAVING REDUCED PHASE SHIFT FOR USE IN MEMS SENSING APPLICATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 8084786 | SILICIDED BASE STRUCTURE FOR HIGH FREQUENCY TRANSISTORS |
| FREESCALE SEMICONDUCTOR, INC. | 8085200 | SYSTEM AND METHOD FOR ESTABLISHING A WPAN WITH PRECISE LOCATIONING CAPABILITY |
| FREESCALE SEMICONDUCTOR, INC. | 8085700 | SYSTEM NODE AND METHOD FOR PROVIDING MEDIA ARBITRATION |
| FREESCALE SEMICONDUCTOR, INC. | 8085868 | PHASE MODULATING AND COMBINING CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8085954 | MICROPHONE AMPLIFICATION ARRANGEMENT AND INTEGRATED CIRCUIT THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8086234 | BROADCAST HANDOFF BETWEEN COMMUNICATION NETWORKS |

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| FREESCALE SEMICONDUCTOR, INC. | 8088657 | INTEGRATED CIRCUIT USING FINFETS AND HAVING A STATIC RANDOM ACCESS MEMORY (SRAM) |
| FREESCALE SEMICONDUCTOR, INC. | 8089259 | INTEGRATED CIRCUIT AND A METHOD FOR RECOVERING FROM A LOW-POWER PERIOD |
| FREESCALE SEMICONDUCTOR, INC. | 8089978 | METHOD FOR MANAGING UNDER-RUN AND A DEVICE HAVING UNDER-RUN MANAGEMENT CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 8090892 | ORDERED QUEUE AND METHODS THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8090984 | ERROR DETECTION AND COMMUNICATION OF AN ERROR LOCATION IN MULTI-PROCESSOR DATA PROCESSING SYSTEM HAVING PROCESSORS OPERATING IN LOCKSTEP |
| FREESCALE SEMICONDUCTOR, INC. | 8091257 | STEAM IRON WITH ACCELERATION AND TILT DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | 8093084 | SEMICONDUCTOR DEVICE WITH PHOTONICS |
| FREESCALE SEMICONDUCTOR, INC. | 8093102 | PROCESS OF FORMING AN ELECTRONIC DEVICE INCLUDING A PLURALITY OF SINGULATED DIE |
| FREESCALE SEMICONDUCTOR, INC. | 8093700 | PACKAGING MILLIMETER WAVE MODULES |
| FREESCALE SEMICONDUCTOR, INC. | 8093880 | PROGRAMMABLE VOLTAGE REFERENCE WITH A VOLTAGE REFERENCE CIRCUIT HAVING A SELF-CASCODE METAL-OXIDE SEMICONDUCTOR FIELD-EFFECT TRANSISTOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 8093929 | PROGRAMMABLE DIGITAL CLOCK SIGNAL FREQUENCY DIVIDER MODULE AND MODULAR DIVIDER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8093933 | METHOD FOR FAST TRACKING AND JITTER IMPROVEMENT IN ASYNCHRONOUS SAMPLE RATE CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | 8094755 | RAMPING IN MULTIMODE TRANSMITTERS USING PRIMED FILTERS |
| FREESCALE SEMICONDUCTOR, INC. | 8094769 | PHASE-LOCKED LOOP SYSTEM WITH A PHASE ERROR SPREADING CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8095769 | METHOD FOR ADDRESS COMPARISON AND A DEVICE HAVING ADDRESS COMPARISON CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 8095809 | SYSTEM AND METHOD FOR REDUCING POWER CONSUMPTION |
| FREESCALE SEMICONDUCTOR, INC. | 8095831 | PROGRAMMABLE ERROR ACTIONS FOR A CACHE IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8095836 | TIME-BASED TECHNIQUES FOR DETECTING AN IMMINENT READ FAILURE IN A MEMORY ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | 8096179 | SENSOR DEVICE WITH REDUCED PARASITIC-INDUCED ERROR |
| FREESCALE SEMICONDUCTOR, INC. | 8096182 | CAPACITIVE SENSOR WITH STRESS RELIEF THAT COMPENSATES FOR PACKAGE STRESS |
| FREESCALE SEMICONDUCTOR, INC. | 8097494 | METHOD OF MAKING AN INTEGRATED CIRCUIT PACKAGE WITH SHIELDING VIA RING SRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 8097873 | PHASE CHANGE MEMORY STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | 8098744 | REDUCING A PEAK-TO-AVERAGE RATIO OF A SIGNAL USING FILTERING |
| FREESCALE SEMICONDUCTOR, INC. | 8099067 | DATA SIGNAL SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8099560 | SYNCHRONIZATION MECHANISM FOR USE WITH A SNOOP QUEUE |
| FREESCALE SEMICONDUCTOR, INC. | 8099580 | TRANSLATION LOOK-ASIDE BUFFER WITH A TAG MEMORY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8099657 | ERROR CORRECTING VITERBI DECODER |
| FREESCALE SEMICONDUCTOR, INC. | 8099729 | METHOD AND DEVICE FOR CREATING AND USING PRE-INTERNALIZED PROGRAM FILES |
| FREESCALE SEMICONDUCTOR, INC. | 8102399 | METHOD AND DEVICE FOR PROCESSING IMAGE DATA STORED IN A FRAME BUFFER |
| FREESCALE SEMICONDUCTOR, INC. | 8103833 | A CACHE MEMORY AND A METHOD FOR SERVICING ACCESS REQUESTS |
| FREESCALE SEMICONDUCTOR, INC. | 8105890 | METHOD OF FORMING A SEMICONDUCTOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 8105925 | METHOD FOR FORMING AN INSULATED GATE FIELD EFFECT DEVICE |

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| FREESCALE SEMICONDUCTOR, INC. | 8105933 | LOCALIZED ALLOYING FOR IMPROVED BOND RELIABILITY |
| FREESCALE SEMICONDUCTOR, INC. | 8106604 | LED DRIVER WITH DYNAMIC POWER MANAGEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 8111825 | ENCRYPTION APPARATUS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8111945 | A SYSTEM AND METHOD FOR PROVIDING A BLENDED PICTURE |
| FREESCALE SEMICONDUCTOR, INC. | 8112645 | SYSTEM AND METHOD FOR POWER MANAGEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 8114739 | SEMICONDUCTOR DEVICE WITH OXYGEN-DIFFUSION BARRIER LAYER AND METHOD FOR FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8115288 | LEAD FRAME FOR SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8115414 | LED DRIVER WITH SEGMENTED DYNAMIC HEADROOM CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 8115469 | DRIVER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8115499 | DEVICE WITH PROXIMITY DETECTION CAPABILITY |
| FREESCALE SEMICONDUCTOR, INC. | 8115516 | CIRCUIT ARRANGEMENT FOR FILTERING UNWANTED SIGNALS FROM A CLOCK SIGNAL, PROCESSING SYSTEM AND METHOD OF FILTERING UNWANTED SIGNALS FROM A CLOCK SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 8115544 | AMPLIFIER CIRCUIT AND INTEGRATED CIRCUIT THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8115863 | VIDEO DE-INTERLACER USING PIXEL TRAJECTORY |
| FREESCALE SEMICONDUCTOR, INC. | 8116153 | READ ONLY MEMORY AND METHOD OF READING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8116318 | A METHOD FOR SCHEDULING ATM CELLS AND A DEVICE HAVING ATM CELL SCHEDULING CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 8116397 | SYSTEM AND METHOD FOR SYMBOL BOUNDARY DETECTION IN ORTHOGONAL FREQUENCY DIVISON MULTIPLEXING BASED DATA COMMUNICATION |
| FREESCALE SEMICONDUCTOR, INC. | 8116687 | DYNAMIC FREQUENCY SELECTION IN WIRELESS DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 8117383 | HARDWARE ACCELERATOR BASED METHOD AND DEVICE FOR STRING SEARCHING |
| FREESCALE SEMICONDUCTOR, INC. | 8117399 | PROCESSING OF COHERENT AND INCOHERENT ACCESSES AT A UNIFORM CACHE |
| FREESCALE SEMICONDUCTOR, INC. | 8117400 | SYSTEM AND METHOD FOR FETCHING AN INFORMATION UNIT |
| FREESCALE SEMICONDUCTOR, INC. | 8117483 | METHOD TO CALIBRATE START VALUES FOR WRITE LEVELING IN A MEMORY SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8117618 | FORWARD PROGRESS MECHANISM FOR A MULTITHREADED PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 8117642 | COMPUTING DEVICE WITH ENTRY AUTHENTICATION INTO TRUSTED EXECUTION ENVIRONMENT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8119334 | METHOD OF MAKING A SEMICONDUCTOR DEVICE USING NEGATIVE PHOTORESIST |
| FREESCALE SEMICONDUCTOR, INC. | 8119431 | METHOD OF FORMING A MICRO-ELECTROMECHANICAL SYSTEM (MEMS) HAVING A GAP STOP |
| FREESCALE SEMICONDUCTOR, INC. | 8120404 | FLIP-FLOP CIRCUIT WITH INTERNAL LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | 8120412 | VOLTAGE BOOSTING SYSTEM WITH SLEW RATE CONTROL AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 8120660 | IMAGE DATA UP SAMPLING |
| FREESCALE SEMICONDUCTOR, INC. | 8120975 | MEMORY HAVING NEGATIVE VOLTAGE WRITE ASSIST CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8121228 | DETECTING A DATA FRAME |
| FREESCALE SEMICONDUCTOR, INC. | 8121761 | ACCELERATION SENSOR ARRANGEMENT, SAFING ARRANGEMENT FOR AN |

ACTIVATION SYSTEM, ACTIVATION SYSTEM

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| FREESCALE SEMICONDUCTOR, INC. | 8122437 | METHOD AND APPARATUS TO TRACE AND CORRELATE DATA TRACE AND INSTRUCTION TRACE FOR OUT-OF-ORDER PROCESSORS |
| FREESCALE SEMICONDUCTOR, INC. | 8125032 | MODIFIED HYBRID ORIENTATION TECHNOLOGY |
| FREESCALE SEMICONDUCTOR, INC. | 8125231 | CAPACITANCE-TO-VOLTAGE INTERFACE CIRCUIT, AND RELATED OPERATING METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 8126101 | METHOD AND APPARATUS FOR VARYING A DYNAMIC RANGE |
| FREESCALE SEMICONDUCTOR, INC. | 8126422 | RECEIVER HAVING VOLTAGE-TO-CURRENT AND CURRENT-TO-VOLTAGE CONVERTERS |
| FREESCALE SEMICONDUCTOR, INC. | 8127258 | DATA PROCESSING DEVICE DESIGN TOOL AND METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 8129226 | POWER LEAD-ON-CHIP BALL GRID ARRAY PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 8130014 | NETWORK AND METHOD FOR SETTING A TIME-BASE OF A NODE IN THE NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 8130018 | LATCH MODULE AND FREQUENCY DIVIDER |
| FREESCALE SEMICONDUCTOR, INC. | 8131241 | LINEAR VOLTAGE CONTROLLED VARIABLE ATTENUATOR WITH LINEAR DB/V GAIN SLOPE |
| FREESCALE SEMICONDUCTOR, INC. | 8131316 | CELLULAR MODEM PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 8131914 | AN ELECTRONIC DEVICE HAVING A MEMORY ELEMENT AND METHOD OF OPERATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8131947 | CACHE SNOOP LIMITING WITHIN A MULTIPLE MASTER DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8131948 | SNOOP REQUEST ARBITRATION IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8131951 | UTILIZATION OF A STORE BUFFER FOR ERROR RECOVERY ON A STORE ALLOCATION CACHE MISS |
| FREESCALE SEMICONDUCTOR, INC. | 8134219 | SCHOTTKY DIODES |
| FREESCALE SEMICONDUCTOR, INC. | 8134222 | MOS CAPACITOR STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | 8134241 | ELECTRONIC ELEMENTS AND DEVICES WITH TRENCH UNDER BOND PAD FEATURE |
| FREESCALE SEMICONDUCTOR, INC. | 8134384 | METHOD FOR TESTING NOISE IMMUNITY OF AN INTEGRATED CIRCUIT AND A DEVICE HAVING NOISE IMMUNITY TESTING CAPABILITES |
| FREESCALE SEMICONDUCTOR, INC. | 8134941 | POWER SAVING IN SIGNAL PROCESSING IN RECEIVERS |
| FREESCALE SEMICONDUCTOR, INC. | 8135094 | RECEIVER I/Q GROUP DELAY MISMATCH CORRECTION |
| FREESCALE SEMICONDUCTOR, INC. | 8135966 | A METHOD AND DEVICE FOR POWER MANAGEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 8136001 | TECHNIQUE FOR INITIALIZING DATA AND INSTRUCTIONS FOR CORE FUNCTIONAL PATTERN GENERATION IN MULTI-CORE PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 8138007 | MEMS DEVICE WITH STRESS ISOLATION AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 8138062 | ELECTRICAL COUPLING OF WAFER STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | 8138073 | METHOD FOR FORMING A SCHOTTKY DIODE HAVING A METAL- SEMICONDUCTOR SCHOTTKY CONTACT |
| FREESCALE SEMICONDUCTOR, INC. | 8138584 | METHOD OF FORMING A SEMICONDUCTOR PACKAGE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 8139540 | ARRANGEMENT AND METHOD FOR DUAL MODE OPERATION IN A COMMUNICATION SYSTEM TERMINAL |
| FREESCALE SEMICONDUCTOR, INC. | 8139599 | SYSTEM AND METHOD FOR OPERATING A COMMUNICATIONS SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8139683 | A RECEIVER AND A METHOD FOR CHANNEL ESTIMATION |
| FREESCALE SEMICONDUCTOR, INC. | 8139760 | ESTIMATING DELAY OR AN ECHO PATH IN A COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8140110 | CONTROLLING INPUT AND OUTPUT IN A MULTI-MODE WIRELESS PROCESSING |

SYSTEM

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8143074 | SEMICONDUCTOR PROCESSING SYSTEM AND METHOD OF PROCESSING A SEMICONDUCTOR WAFER |
| FREESCALE SEMICONDUCTOR, INC. | 8143126 | METHOD FOR FORMING A VERTICAL MOS TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 8143921 | LATCHED COMPARATOR AND METHODS THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8143929 | FLIP-FLOP HAVING SHARED FEEDBACK AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 8145158 | BIAS CIRCUIT FOR A RADIO FREQUENCY POWER-AMPLIFIER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8145985 | ERROR DETECTION SCHEMES FOR A UNIFIED CACHE IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8146039 | OPTIMAL DISTANCE BASED BUFFER TREE FOR DATA PATH AND CLOCK |
| FREESCALE SEMICONDUCTOR, INC. | 8148206 | PACKAGE FOR HIGH POWER INTEGRATED CIRCUITS AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 8148793 | THREE DIMENSIONAL INTEGRATED PASSIVE DEVICE AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 8149564 | MEMS CAPACITIVE DEVICE AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8150350 | ADAPTIVE IIP2 CALIBRATION |
| FREESCALE SEMICONDUCTOR, INC. | 8150360 | DC OFFSET CALIBRATION IN A DIRECT CONVERSION RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 8151075 | MULTIPLE ACCESS TYPE MEMORY AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 8155189 | SYSTEM AND METHOD OF CODING MODE DECISION FOR VIDEO ENCODING |
| FREESCALE SEMICONDUCTOR, INC. | 8156265 | DATA PROCESSOR COUPLED TO A SEQUENCER CIRCUIT THAT PROVIDES EFFICIENT SCALABLE QUEUING AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 8156273 | METHOD AND SYSTEM FOR CONTROLLING TRANSMISSION AND EXECUTION OF COMMANDS IN AN INTEGRATED CIRCUIT DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8156357 | VOLTAGE-BASED MEMORY SIZE SCALING IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8156411 | ERROR CORRECTION OF AN ENCODED MESSAGE |
| FREESCALE SEMICONDUCTOR, INC. | 8156805 | MEMS INERTIAL SENSOR WITH FREQUENCY CONTROL AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 8158484 | METHOD OF FORMING AN INVERTED T SHAPED CHANNEL STRUCTURE FOR AN INVERTED T CHANNEL FIELD EFFECT TRANSISTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8158492 | MEMS MICROPHONE WITH CAVITY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8160518 | MULTI-MODE TRANSCEIVER HAVING TUNABLE HARMONIC TERMINATION CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8161449 | IMPROVING TEST PATTERN COVERAGE THROUGH PARALLEL DISCARD, FLOW CONTROL, AND QUALITY METRICS |
| FREESCALE SEMICONDUCTOR, INC. | 8163609 | NANOCRYSTAL MEMORY WITH DIFFERENTIAL ENERGY BANDS AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 8163615 | SPLIT-GATE NON-VOLATILE MEMORY CELL HAVING IMPROVED OVERLAP TOLERANCE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8164321 | CURRENT INJECTOR CIRCUIT FOR SUPPLYING A LOAD TRANSIENT IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8164378 | DEVICE AND TECHNIQUE FOR TRANSISTOR WELL BIASING |
| FREESCALE SEMICONDUCTOR, INC. | 8165214 | CIRCUIT AND METHOD FOR GENERATING FIXED POINT VECTOR DOT PRODUCT AND MATRIX VECTOR VALUES |
| FREESCALE SEMICONDUCTOR, INC. | 8165243 | METHOD AND SYSTEM FOR GENERATING WAVELETS |
| FREESCALE SEMICONDUCTOR, INC. | 8165255 | MULTIRATE RESAMPLING AND FILTERING SYSTEM AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 8168464 | MICROELECTRONIC ASSEMBLY WITH AN EMBEDDED WAVEGUIDE ADAPTER AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8168468 | CONDUCTIVE BRIDGE RANDOM ACCESS MEMORY DEVICE AND METHOD OF MAKING THE SAME |

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8169245 | DUTY TRANSITION CONTROL IN PULSE WIDTH MODULATION SIGNALING |
| FREESCALE SEMICONDUCTOR, INC. | 8169257 | SYSTEM AND METHOD FOR COMMUNICATING BETWEEN MULTIPLE VOLTAGE TIERS |
| FREESCALE SEMICONDUCTOR, INC. | 8169978 | TECHNIQUES FOR FREQUENCY-DOMAIN JOINT DETECTION IN WIRELESS COMMUNICATIONS SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 8170166 | METHODS AND SYSTEMS FOR COMBINING TIMING SIGNALS FOR TRANSMISSION OVER A SERIAL INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | 8170509 | INCIDENT AND REFLECTED SIGNAL PHASE DIFFERENCE DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | 8171187 | SYSTEM AND METHOD FOR ARBITRATING BETWEEN MEMORY ACCESS REQUESTS |
| FREESCALE SEMICONDUCTOR, INC. | 8171336 | METHOD FOR PROTECTING A SECURED REAL TIME CLOCK MODULE AND A DEVICE HAVING PROTECTION CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 8171384 | DEVICE HAVING TURBO DECODING CAPABILITIES AND A METHOD FOR TURBO DECODING |
| FREESCALE SEMICONDUCTOR, INC. | 8173505 | METHOD OF MAKING A SPLIT GATE MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | 8174251 | SERIES REGULATOR WITH OVER CURRENT PROTECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8174279 | SOCKET CONNECTOR FOR CONNECTION LEAD OF SEMICONDUCTOR DEVICE UNDER TEST WITH TESTER |
| FREESCALE SEMICONDUCTOR, INC. | 8175213 | SYSTEM AND METHOD FOR SETTING COUNTER THRESHOLD VALUE |
| FREESCALE SEMICONDUCTOR, INC. | 8175276 | ENCRYPTION APPARATUS WITH DIVERSE KEY RETENTION SCHEMES |
| FREESCALE SEMICONDUCTOR, INC. | 8175548 | METHOD AND DEVICE FOR TRANSMITTING A SEQUENCE OF TRANSMISSION BURSTS |
| FREESCALE SEMICONDUCTOR, INC. | 8175560 | METHOD AND SYSTEM FOR TUNING AN ANTENNA |
| FREESCALE SEMICONDUCTOR, INC. | 8176227 | METHOD AND SYSTEM FOR HIGH-SPEED DETECTION HANDSHAKE IN UNIVERSAL SERIAL BUS BASED DATA COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8176340 | METHOD AND SYSTEM FOR INITIAILIZING AN INTERFACE BETWEEN TWO CIRCUITS OF A COMMUNICATION DEVICE WHILE A PROCESSOR OF THE FIRST CIRCUIT IS INACTIVE AND WAKING UP THE PROCESSOR THEREAFTER |
| FREESCALE SEMICONDUCTOR, INC. | 8177426 | SUB-THRESHOLD CMOS TEMPERATURE DETECTOR |
| FREESCALE SEMICONDUCTOR, INC. | 8178401 | METHOD FOR FABRICATING DUAL-METAL GATE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8178406 | SPLIT GATE DEVICE AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 8178942 | ELECTRICALLY ALTERABLE CIRCUIT FOR USE IN AN INTEGRATED CIRCUIT DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8178950 | MULTILAYERED THROUGH A VIA |
| FREESCALE SEMICONDUCTOR, INC. | 8179051 | SERIAL CONFIGURATION FOR DYNAMIC POWER CONTROL IN LED DISPLAYS |
| FREESCALE SEMICONDUCTOR, INC. | 8179108 | REGULATOR HAVING PHASE COMPENSATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8179187 | SUBSTRATE NOISE PASSIVE CANCELLATION METHOD FOR BUCK CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 8180007 | METHOD FOR CLOCK AND DATA RECOVERY |
| FREESCALE SEMICONDUCTOR, INC. | 8180969 | CACHE USING PSEUDO LEAST RECENTLY USED (PLRU) CACHE REPLACEMENT WITH LOCKING |
| FREESCALE SEMICONDUCTOR, INC. | 8181049 | METHOD FOR CONTROLLING A FREQUENCY OF A CLOCK SIGNAL TO CONTROL POWER CONSUMPTION AND A DEVICE HAVING POWER CONSUMPTION CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 8181051 | ELECTRONIC APPARATUS AND METHOD OF CONSERVING ENERGY |
| FREESCALE SEMICONDUCTOR, INC. | 8181098 | ERROR CORRECTING VITERBI DECODER |
| FREESCALE SEMICONDUCTOR, INC. | 8183639 | DUAL PORT STATIC RANDOM ACCESS MEMORY CELL LAYOUT |
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| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8184027 | SEMICONDUCTOR DEVICE AND DIFFERENTIAL AMPLIFIER CIRCUIT THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8184750 | TECHNIQUES FOR INCREASING DECODING RELIABILITY IN AN ADAPTIVE MINIMUM MEAN SQUARED ERROR WITH SUCCESSIVE INTERFERENCE CANCELLATION (MMSE/SIC) DECODER |
| FREESCALE SEMICONDUCTOR, INC. | 8184812 | SECURE COMPUTING DEVICE WITH MONOTONIC COUNTER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8185798 | TECHNIQUES FOR REDUCING JOINT DETECTION COMPLEXITY IN A CHANNEL-CODED MULTIPLE-INPUT MULTIPLE-OUTPUT COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8186220 | ACCELEROMETER WITH OVER-TRAVEL STOP STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 8186221 | VERTICALLY INTEGRATED MEMS ACCELERATION TRANSDUCER |
| FREESCALE SEMICONDUCTOR, INC. | 8187978 | METHOD OF FORMING OPENINGS IN A SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8188539 | FIELD-EFFECT SEMICONDUCTOR DEVICE AND METHOD OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8188543 | ELECTRONIC DEVICE INCLUDING A CONDUCTIVE STRUCTURE EXTENDING THROUGH A BURIED INSULATING LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 8189408 | MEMORY DEVICE HAVING SHIFTING CAPABILITY AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 8189717 | LOW IF RADIO RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 8191085 | METHOD AND APPARATUS FOR LOADING OR STORING MULTIPLE REGISTERS IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8193560 | VOLTAGE LIMITING DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 8193572 | ELECTRONIC DEVICE INCLUDING TRENCHES AND DISCONTINUOUS STORAGE ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | 8193585 | SEMICONDUCTOR DEVICE WITH INCREASED SNAPBACK VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | 8193591 | TRANSISTOR AND METHOD WITH DUAL LAYER PASSIVATION |
| FREESCALE SEMICONDUCTOR, INC. | 8193828 | BUFFER APPARATUS, INTEGRATED CIRCUIT AND METHOD OF REDUCING A PORTION OF AN OSCILLATION OF AN OUTPUT SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 8193868 | SWITCHED CAPACITOR CIRCUIT FOR A VOLTAGE CONTROLLED OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | 8194528 | PACKET BASED DATA CELL DELINEATION |
| FREESCALE SEMICONDUCTOR, INC. | 8198143 | MOLD AND SUBSTRATE FOR USE WITH MOLD |
| FREESCALE SEMICONDUCTOR, INC. | 8198703 | ZENER DIODE WITH REDUCED SUBSTRATE CURRENT |
| FREESCALE SEMICONDUCTOR, INC. | 8198705 | ULTRA-THIN DIE AND METHOD OF FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8198737 | METHOD OF FORMING WIRE BONDS IN SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 8198916 | DIGITAL SIGNAL VOLTAGE LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | 8198933 | MIXER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8198937 | SWITCHED-CAPACITOR AMPLIFIER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8199547 | ERROR DETECTION IN A CONTENT ADDRESSABLE MEMORY (CAM) |
| FREESCALE SEMICONDUCTOR, INC. | 8200733 | DEVICE HAVING INTERLEAVING CAPABILITIES AND A METHOD FOR APPLYING AN INTERLEAVING FUNCTION |
| FREESCALE SEMICONDUCTOR, INC. | 8200908 | METHOD FOR DEBUGGER INITIATED COHERENCY TRANSACTIONS USING A SHARED COHERENCY MANAGER |
| FREESCALE SEMICONDUCTOR, INC. | 8201025 | DEBUG MESSAGING WITH SELECTIVE TIMESTAMP CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 8202778 | PATTERNING A GATE STACK OF A NON-VOLATILE MEMORY (NVM) WITH SIMULTANEOUS ETCH IN NON-NVM AREA |
| FREESCALE SEMICONDUCTOR, INC. | 8202798 | IMPROVEMENTS FOR REDUCING ELECTROMIGRATION EFFECT IN AN |

INTEGRATED CIRCUIT

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8203822 | DIGITAL SQUIB DRIVER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8204035 | NETWORK NODE |
| FREESCALE SEMICONDUCTOR, INC. | 8204129 | SIMPLIFIED DEBLOCK FILTERING FOR REDUCED MEMORY ACCESS AND COMPUTATIONAL COMPLEXITY |
| FREESCALE SEMICONDUCTOR, INC. | 8204166 | CLOCK CIRCUIT WITH CLOCK TRANSFER CAPABILITY AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 8204458 | TRANSMITTING DEVICE AND METHOD OF TUNING THE TRANSMITTING DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8205068 | BRANCH TARGET BUFFER ALLOCATION |
| FREESCALE SEMICONDUCTOR, INC. | 8209558 | SYSTEM AND METHOD FOR CONTROLLING VOLTAGE AND FREQUENCY IN A MULTIPLE VOLTAGE ENVIRONMENT |
| FREESCALE SEMICONDUCTOR, INC. | 8211844 | METHOD FOR CLEANING A SEMICONDUCTOR STRUCTURE AND CHEMISTRY THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 8212159 | CAPACITIVE TOUCHPAD METHOD USING MCU GPIO AND SIGNAL PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 8212292 | HIGH GAIN TUNABLE BIPOLAR TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 8212321 | SEMICONDUCTOR DEVICE WITH FEEDBACK CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 8213343 | COMMUNICATING CONVERSATIONAL DATA BETWEEN SIGNALS BETWEEN TERMINALS OVER A RADIO LINK |
| FREESCALE SEMICONDUCTOR, INC. | 8214674 | INTEGRATED CIRCUIT HAVING A MICROCONTROLLER UNIT AND METHODS OF OPERATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8214722 | METHOD AND SYSTEM FO SIGNAL ERROR DETERMINATION AND CORRECTION IN A FLEXRAY COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8215177 | APPARATUS AND METHOD FOR APPLYING STRESS-INDUCED OFFSET COMPENSATION IN SENSOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 8216882 | MEMS SENSOR DEVICE WITH MULTI-STIMULUS SENSING AND METHOD OF FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8216886 | METHOD FOR MAKING SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 8216918 | METHOD OF FORMING A PACKAGED SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8217448 | SEMICONDUCTOR DEVICE AND METHOD OF FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8217511 | REDISTRIBUTED CHIP PACKAGING WITH THERMAL CONTACT TO DEVICE BACKSIDE |
| FREESCALE SEMICONDUCTOR, INC. | 8217605 | MOTOR CONTROLLER FOR DETERMINING A POSITION OF A ROTOR OF AN AC MOTOR, AC MOTOR SYSTEM, AND METHOD OF DETERMINING A POSITION OF A ROTOR OF AN AC MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | 8217673 | METHOD AND CIRCUIT FOR TESTING INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8219092 | USER EQUIPMENT FREQUENCY ALLOCATION METHODS AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 8219761 | MULTI-PORT HIGH-LEVEL CACHE UNIT AND A METHOD FOR RETRIEVING INFORMATION FROM A MULTI-PORT HIGH-LEVEL CACHE UNIT |
| FREESCALE SEMICONDUCTOR, INC. | 8220330 | VERTICALLY INTEGRATED MEMS SENSOR DEVICE WITH MULTI-STIMULUS SENSING |
| FREESCALE SEMICONDUCTOR, INC. | 8222943 | MASTER-SLAVE FLIP-FLOP WITH TIMING ERROR CORRECTION |
| FREESCALE SEMICONDUCTOR, INC. | 8223572 | EFFICIENT WORD LINES, BIT LINE AND PRECHARGE TRACKING IN SELF-TIMED MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8223910 | METHOD AND DEVICE FOR FRAME SYNCHRONIZATION |
| FREESCALE SEMICONDUCTOR, INC. | 8225123 | METHOD AND SYSTEM FOR INTEGRATED CIRCUIT POWER SUPPLY MANAGEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 8227861 | MULTI-GATE SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 8228080 | DEVICE AND METHOD FOR CURRENT ESTIMATION |
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| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8228098 | PULSE WIDTH MODULATION FREQUENCY CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | 8228100 | DATA PROCESSING SYSTEM HAVING BROWN-OUT DETECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8228109 | TRANSMISSION GATE CIRCUITRY FOR HIGH VOLTAGE TERMINAL |
| FREESCALE SEMICONDUCTOR, INC. | 8228117 | QUIET POWER UP AND POWER DOWN OF CLOSED LOOP DIGITAL PWM MODULATORS |
| FREESCALE SEMICONDUCTOR, INC. | 8229502 | MOBILE COMMUNICATIONS DEVICE, CONTROLLER, AND METHOD FOR CONTROLLING A MOBILE COMMUNICATIONS DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8233524 | RADIO TRANSMITTER IQ IMBALANCE MEASUREMENT AND CORRECTION METHODS AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 8234452 | DEVICE AND METHOD FOR FETCHING INSTRUCTIONS |
| FREESCALE SEMICONDUCTOR, INC. | 8234618 | TRACE RECONSTRUCTION FOR SILICON VALIDATION OF ASYNCHRONOUS SYSTEMS-ON-CHIP |
| FREESCALE SEMICONDUCTOR, INC. | 8236609 | PACKAGING AN INTEGRATED CIRCUIT DIE WITH BACKSIDE METALLIZATION |
| FREESCALE SEMICONDUCTOR, INC. | 8236638 | SHALLOW TRENCH ISOLATION FOR SOI STRUCTURES COMBINING SIDEWALL SPACER AND BOTTOM LINER |
| FREESCALE SEMICONDUCTOR, INC. | 8237293 | SEMICONDUCTOR PACKAGE WITH PROTECTIVE TAPE |
| FREESCALE SEMICONDUCTOR, INC. | 8237424 | REGULATED VOLTAGE SYSTEM AND METHOD OF PROTECTION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8237700 | SYNCHRONIZED PHASE-SHIFTED PULSE WIDTH MODULATION SIGNAL GENERATION |
| FREESCALE SEMICONDUCTOR, INC. | 8238333 | METHOD FOR TRANSMITTING DATA AND A DEVICE HAVING DATA TRANSMISSION CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 8238674 | METHOD FOR ENCODING AND DECODING IMAGES |
| FREESCALE SEMICONDUCTOR, INC. | 8238849 | METHOD AND SYSTEM OF ADAPTIVE PREDISTORTION OF A WIRELESS TRANSMITTER |
| FREESCALE SEMICONDUCTOR, INC. | 8238860 | TUNING A SECOND ORDER INTERCEPT POINT OF A MIXER IN A RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 8239587 | DEVICE HAVING DATA SHARING CAPABILITIES AND A METHOD FOR SHARING DATA |
| FREESCALE SEMICONDUCTOR, INC. | 8239625 | PARITY GENERATOR FOR REDUNDANT ARRAY OF INDEPENDENT DISCS TYPE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 8239745 | PARITY DATA ENCODER FOR SERIAL COMMUNICATION |
| FREESCALE SEMICONDUCTOR, INC. | 8239799 | DESIGN PLACEMENT METHOD AND DEVICE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8239807 | METHOD OF MAKING ROUTABLE LAYOUT PATTERN USING CONGESTION TABLE |
| FREESCALE SEMICONDUCTOR, INC. | 8242564 | SEMICONDUCTOR DEVICE WITH PHOTONICS |
| FREESCALE SEMICONDUCTOR, INC. | 8242566 | STACKED ESD PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 8242613 | BOND PAD FOR SEMICONDUCTOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | 8242763 | DC TO DC CONVERTER HAVING ABILITY OF SWITCHING BETWEEN CONTINUOUS AND DISCONTINUOUS MODES AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 8242815 | MICROCONTROLLER UNIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8243405 | CIRCUIT, INTEGRATED CIRCUIT AND METHOD FOR DISSIPATING HEAT FROM AN INDUCTIVE LOAD |
| FREESCALE SEMICONDUCTOR, INC. | 8243855 | CALIBRATED QUADRATURE GENERATION FOR MULTI-GHZ RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 8244381 | MICROPROCESSOR, SYSTEM FOR CONTROLLING A DEVICE AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 8245068 | POWER SUPPLY MONITORING METHOD AND SYSTEM |

8245562 CIRCUIT AND METHOD FOR PRESSURE SENSOR TESTING

FREESCALE SEMICONDUCTOR, INC.

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8247850 | DUAL INTERLAYER DIELECTRIC STRESSOR INTEGRATION WITH A SACRIFICIAL UNDERLAYER FILM STACK |
| FREESCALE SEMICONDUCTOR, INC. | 8247869 | LDMOS TRANSISTORS WITH A SPLIT GATE |
| FREESCALE SEMICONDUCTOR, INC. | 8248130 | DUTY CYCLE CORRECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8248133 | PROGRAMMABLE DELAY TIMER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8248288 | ANALOG TO DIGITAL CONVERTER WITH AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 8248743 | DEVICE HAVING FAILURE RECOVERY CAPABILITIES AND A METHOD FOR FAILURE RECOVERY |
| FREESCALE SEMICONDUCTOR, INC. | 8250319 | OPERATING AN EMULATED ELECTRICALLY ERASABLE (EEE) MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 8251776 | METHOD AND APPARATUS FOR CONDITIONING A CMP PAD |
| FREESCALE SEMICONDUCTOR, INC. | 8252631 | METHOD AND APPARATUS FOR INTEGRATED CIRCUIT PACKAGES USING MATERIALS WITH LOW MELTING POINT |
| FREESCALE SEMICONDUCTOR, INC. | 8252656 | ZENER TRIGGERED ESD PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 8253453 | BROWN-OUT DETECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8253458 | DIGITAL PHASE LOCKED LOOP WITH REDUCED SWITCHING NOISE |
| FREESCALE SEMICONDUCTOR, INC. | 8253479 | OUTPUT DRIVER CIRCUITS FOR VOLTAGE REGULATORS |
| FREESCALE SEMICONDUCTOR, INC. | 8253495 | WIRELESS COMMUNICATION DEVICE AND SEMICONDUCTOR PACKAGE DEVICE HAVING A POWER AMPLIFIER THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8254161 | DEVICE THAT CAN BE RENDERED USELESS AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 8254186 | CIRCUIT FOR VERIFYING THE WRITE ENABLE OF A ONE TIME PROGRAMMABLE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 8255616 | NON-VOLATILE MEMORY DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8255723 | DEVICE HAVING MULTIPLE INSTRUCTION EXECUTION MODULES AND A MANAGEMENT METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 8255748 | SOFT ERROR AND TRANSIENT ERROR DETECTION DEVICE AND METHODS THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8255861 | EFFICIENT REPLAYING OF AUTOGRADED COVERAGE REGRESSIONS AND PERFORMANCE VERIFICATION WITH DIRECTED TESTCASES |
| FREESCALE SEMICONDUCTOR, INC. | 8258035 | METHOD TO IMPROVE SOURCE/DRAIN PARASITICS IN VERTICAL DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 8259427 | POWER TRANSISTOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8260151 | OPTICAL COMMUNICATION INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | 8261011 | ONE-TIME PROGRAMMABLE MEMORY DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 8261047 | QUALIFICATION OF CONDITIONAL DEBUG INSTRUCTIONS BASED ON ADDRESS |
| FREESCALE SEMICONDUCTOR, INC. | 8263463 | NONVOLATILE SPLIT GATE MEMORY CELL HAVING OXIDE GROWTH |
| FREESCALE SEMICONDUCTOR, INC. | 8264060 | METHOD OF SEALING AN AIR GAP IN A LAYER OF A SEMICONDUCTOR STRUCTURE AND SEMICONDUCTOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 8264082 | SEMICONDUCTOR DEVICES WITH LOW RESISTANCE BACK-SIDE COUPLING |
| FREESCALE SEMICONDUCTOR, INC. | 8264295 | SWITCHED VARACTOR CIRCUIT FOR VOLTAGE CONTROLLED OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | 8264393 | CURRENT REDUCTION IN A SINGLE STAGE CYCLIC ANALOG TO DIGITAL CONVERTER WITH VARIABLE RESOLUTION |
| FREESCALE SEMICONDUCTOR, INC. | 8264896 | INTEGRATED CIRCUIT HAVING AN ARRAY SUPPLY VOLTAGE CONTROL CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8265216 | TECHNIQUES FOR ASYNCHRONOUS DATA RECOVERY |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8265573 | WIRELESS SUBCRIBER COMMUNICATION UNIT AND METHOD OF POWER CONTROL WITH BACK-OFF THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8266414 | METHOD FOR EXECUTING AN INSTRUCTION LOOP AND A DEVICE HAVING INSTRUCTION LOOP EXECUTION CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 8266498 | IMPLEMENTATION OF MULTIPLE ERROR DETECTION SCHEMES FOR A CACHE |
| FREESCALE SEMICONDUCTOR, INC. | 8270343 | BROADCASTING OF TEXTUAL AND MULTIMEDIA INFORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 8271569 | TECHNIQUES FOR PERFORMING DISCRETE FOURIER TRANSFORMS ON RADIX-2 PLATFORMS |
| FREESCALE SEMICONDUCTOR, INC. | 8271719 | NON-VOLATILE MEMORY CONTROLLER DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8274146 | HIGH FREQUENCY INTERCONNECT PAD STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 8274303 | SCHMITT TRIGGER WITH TEST CIRCUIT AND METHOD FOR TESTING |
| FREESCALE SEMICONDUCTOR, INC. | 8274415 | SIGMA-DELTA MODULATOR APPARATUS AND METHOD OF GENERATING A MODULATED OUTPUT SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 8275977 | DEBUG SIGNALING IN A MULTIPLE PROCESSOR DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8276199 | METHOD AND DEVICE FOR SECURE TEST PORT AUTHENTICATION |
| FREESCALE SEMICONDUCTOR, INC. | 8278710 | GUARD RING INTEGRATED LDMOS |
| FREESCALE SEMICONDUCTOR, INC. | 8278902 | DC TO DC SWITCHING POWER CONVERTER CONTROLLER USING SPREAD SPECTRUM PWM |
| FREESCALE SEMICONDUCTOR, INC. | 8278932 | METHOD AND DETECTOR FOR DETERMINING A STATE OF A SWITCH |
| FREESCALE SEMICONDUCTOR, INC. | 8278960 | METHOD AND CIRCUIT FOR MEASURING QUIESCENT CURRENT |
| FREESCALE SEMICONDUCTOR, INC. | 8278977 | REFRESH OPERATION DURING LOW POWER MODE CONFIGURATION |
| FREESCALE SEMICONDUCTOR, INC. | 8278988 | METHOD AND APPARATUS FOR GENERATING A MODULATED WAVEFORM SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 8279144 | LED DRIVER WITH FRAME-BASED DYNAMIC POWER MANAGEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 8279566 | MULTI-VOLTAGE ELECTROSTATIC DISCHARGE PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 8279877 | A METHOD FOR PROCESSING ATM CELLS AND A DEVICE HAVING ATM CELL PROCESSING CAPABILITES |
| FREESCALE SEMICONDUCTOR, INC. | 8281080 | METHOD AND APPARATUS FOR MODIFYING AN INFORMATION UNIT USING AN ATOMIC OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 8281188 | DATA PROCESSING SYSTEM WITH PERIPHAL CONFIGURATION INFORMATION ERROR DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | 8283207 | METHODS OF FORMING THROUGH-SUBSTRATE CONDUCTOR FILLED VIAS, AND ELECTRONIC ASSEMBLIES FORMED USING SUCH METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 8283244 | METHOD FOR FORMING ONE TRANSISTOR DRAM CELL STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 8283748 | LOW LOSS SUBSTRATE FOR INTEGRATED PASSIVE DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 8283762 | LEAD FRAME BASED SEMICONDUCTOR PACKAGE AND A METHOD OF MANUFACTURING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8283764 | MICROELECTRONIC ASSEMBLY WITH AN EMBEDDED WAVEGUIDE ADAPTER AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8283780 | SURFACE MOUNT SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8283898 | BATTERY CHARGING CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8284534 | OVERCURRENT PROTECTION CIRCUIT, INTEGRATED CIRCUIT, APPARATUS AND COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | 8284593 | MULTI-PORT MEMORY HAVING A VARIABLE NUMBER OF USED WRITE PORTS |
| FREESCALE SEMICONDUCTOR, INC. | 8284860 | ERROR SIGNAL PROCESSING SYSTEMS FOR GENERATING A DIGITAL ERROR |

SIGNAL FROM AN ANALOG ERROR SIGNAL

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8285908 | BUS BRIDGE AND METHOD FOR INTERFACING OUT-OF-ORDER BUS AND MULTIPLE ORDERED BUSES |
| FREESCALE SEMICONDUCTOR, INC. | 8286011 | METHOD OF WAKING PROCESSOR FROM SLEEP MODE |
| FREESCALE SEMICONDUCTOR, INC. | 8286032 | TRACE MESSAGING DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 8286040 | DEVICE AND METHOD FOR TESTING A CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8286043 | SYSTEM, COMPUTER PROGRAM PRODUCT AND METHOD FOR TESTING A LOGIC CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8288814 | VIA DEFINITION FOR SEMICONDUCTOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | 8288847 | DUAL DIE SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 8289001 | BATTERY CHARGING CIRCUIT AND BATTERY CHARGER |
| FREESCALE SEMICONDUCTOR, INC. | 8289060 | PULSE STATE RETENTION POWER GATING FLIP-FLOP |
| FREESCALE SEMICONDUCTOR, INC. | 8289094 | VOLTAGE CONTROLLED OSCILLATOR (VCO) CIRCUIT WITH INTEGRATED COMPENSATION OF THERMALLY CAUSED FREQUENCY DRIFT |
| FREESCALE SEMICONDUCTOR, INC. | 8289773 | NON-VOLATILE MEMORY (NVM) ERASE OPERATION WITH BROWNOUT RECOVERY TECHNIQUE |
| FREESCALE SEMICONDUCTOR, INC. | 8290080 | TECHNIQUES FOR TRANSMITTING DATA IN A WIRELESS COMMUNICATION SYSTEM USING QUASI-ORTHOGONAL SPACE-TIME CODE |
| FREESCALE SEMICONDUCTOR, INC. | 8290141 | TECHNIQUES FOR COMFORT NOISE GENERATION IN A COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8290473 | REMOTELY MODIFYING DATA IN MEMORY IN A MOBILE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8290736 | CALIBRATION STANDARDS AND METHODS OF THEIR FABRICATION AND USE |
| FREESCALE SEMICONDUCTOR, INC. | 8291257 | APPARATUS AND METHOD TO COMPENSATE FOR INJECTION LOCKING |
| FREESCALE SEMICONDUCTOR, INC. | 8291305 | ERROR DETECTION SCHEMES FOR A CACHE IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8291368 | METHOD FOR REDUCING SURFACE AREA OF PAD LIMITED SEMICONDUCTOR DIE LAYOUT |
| FREESCALE SEMICONDUCTOR, INC. | 8291417 | TRACE BUFFER WITH A PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 8293588 | METHOD OF PROVIDING AN ELECTRONIC DEVICE INCLUDING DIES, A DIELECTRIC LAYER, AND AN ENCAPSULATING LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 8293608 | INTERMEDIATE PRODUCT FOR A MULTICHANNEL FET AND PROCESS FOR OBTAINING AN INTERMEDIATE PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | 8294239 | EFFECTIVE EFUSE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 8294483 | TESTING OF MULTIPLE INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 8295474 | ECHO CANCELLER WITH HEAVY DOUBLE-TALK ESTIMATION |
| FREESCALE SEMICONDUCTOR, INC. | 8296548 | DEVICE AND METHOD FOR FINDING EXTREME VALUES IN A DATA BLOCK |
| FREESCALE SEMICONDUCTOR, INC. | 8296621 | INTEGRATED CIRCUIT COMPRISING ERROR CORRECTION LOGIC, AND A METHOD OF ERROR CORRECTION |
| FREESCALE SEMICONDUCTOR, INC. | 8300464 | METHOD AND CIRCUIT FOR CALIBRATING DATA CAPTURE IN A MEMORY CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | 8300802 | ADAPTIVE FILTER FOR USE IN ECHO REDUCTION |
| FREESCALE SEMICONDUCTOR, INC. | 8302065 | DEVICE AND METHOD FOR TESTING A DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8304271 | INTEGRATED CIRCUIT HAVING A BULK ACOUSTIC WAVE DEVICE AND A TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 8304275 | MEMS DEVICE ASSEMBLY AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8304331 | ANGLED ION IMPLANTATION IN A SEMICONDUCTOR DEVICE |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8305007 | ANALOG-TO-DIGITAL CONVERTER WITH NON-UNIFORM ACCURACY |
| FREESCALE SEMICONDUCTOR, INC. | 8305068 | VOLTAGE REFERENCE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8306000 | METHOD OF OPTIMISING THE RANK OF A MMSE CHANNEL EQUALISER |
| FREESCALE SEMICONDUCTOR, INC. | 8306011 | METHOD AND DEVICE FOR MANAGING MULTI-FRAMES |
| FREESCALE SEMICONDUCTOR, INC. | 8306172 | ELECTRONIC DEVICE, INTEGRATED CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8307147 | INTERCONNECT AND A METHOD FOR DESIGNING AN INTERCONNECT |
| FREESCALE SEMICONDUCTOR, INC. | 8307196 | DATA PROCESSING SYSTEM HAVING BIT EXACT INSTRUCTIONS AND METHODS THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8307227 | DATA COMMUNICATION SYSTEM AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 8307714 | DUAL PORT PRESSURE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | 8309410 | POWER MOSFET WITH A GATE STRUCTURE OF DIFFERENT MATERIAL |
| FREESCALE SEMICONDUCTOR, INC. | 8309419 | CMOS INTEGRATION WITH METAL GATE AND DOPED HIGH-K OXIDES |
| FREESCALE SEMICONDUCTOR, INC. | 8310042 | HEATSINK MOLDLOCKS |
| FREESCALE SEMICONDUCTOR, INC. | 8310300 | CHARGE PUMP HAVING RAMP RATE CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 8310362 | METHOD AND APPARATUS TO RECEIVE LOCATION INFORMATION IN A DIVERSITY ENABLED RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 8310436 | POWER SUPPLY CONTROLLER FOR MULTIPLE LIGHTING COMPONENTS |
| FREESCALE SEMICONDUCTOR, INC. | 8310877 | READ CONDITIONS FOR A NON-VOLATILE MEMORY (NVM) |
| FREESCALE SEMICONDUCTOR, INC. | 8311025 | METHOD, DATA STRUCTURE AND COMPUTER SYSTEM FOR PACKING A WORLDWIDE INTEROPERABILITY FOR MICROWAVE ACCESS (WiMAX) FRAME |
| FREESCALE SEMICONDUCTOR, INC. | 8311074 | LOW POWER, HIGH RESOLUTION TIMING GENERATOR FOR ULTRA-WIDE BANDWIDTH COMMUNICATION SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 8311494 | TEST UNIT FOR TESTING THE FREQUENCY CHARACTERISTIC OF A TRANSMITTER |
| FREESCALE SEMICONDUCTOR, INC. | 8311495 | INCIDENT AND REFLECTED SIGNAL PHASE DIFFERENCE DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | 8312253 | DATA PROCESSOR DEVICE HAVING TRACE CAPABILITIES AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 8312331 | MEMORY TESTING WITH SNOOP CAPABILITIES IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8313947 | METHOD FOR TESTING A CONTACT STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 8314026 | ANCHORED CONDUCTIVE VIA AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 8314448 | TRANSISTORS WITH IMMERSED CONTACTS |
| FREESCALE SEMICONDUCTOR, INC. | 8315026 | SEMICONDUCTOR DEVICE AND APPARATUS INCLUDING SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8315117 | INTEGRATED CIRCUIT MEMORY HAVING ASSISTED ACCESS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8316186 | METHOD AND APPARATUS FOR MANAGING CACHE RELIABILITY BASED ON AN ASSOCIATED ERROR RATE |
| FREESCALE SEMICONDUCTOR, INC. | 8316718 | MEMS PRESSURE SENSOR DEVICE AND METHOD OF FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8318545 | METHOD OF MAKING A MOUNTED GALLIUM NITRIDE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8318549 | MOLDED SEMICONDUCTOR PACKAGE HAVING A FILLER MATERIAL |
| FREESCALE SEMICONDUCTOR, INC. | 8318576 | DECOUPLING CAPACITORS RECESSED IN SHALLOW TRENCH ISOLATION |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8318577 | METHOD OF MAKING A SEMICONDUCTOR DEVICE AS A CAPACITOR |
| FREESCALE SEMICONDUCTOR, INC. | 8319283 | LATERALLY DIFFUSED METAL OXIDE SEMICONDUCTOR (LDMOS) DEVICE WITH MULTIPLE GATES AND DOPED REGIONS |
| FREESCALE SEMICONDUCTOR, INC. | 8319310 | FIELD EFFECT TRANSISTOR GATE PROCESS AND STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 8319504 | TUNER CHARACTERIZATION METHODS AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 8319548 | INTEGRATED CIRCUIT HAVING LOW POWER MODE VOLTAGE REGULATOR |
| FREESCALE SEMICONDUCTOR, INC. | 8319550 | SWITCHED-CAPACITOR PROGRAMMABLE-GAIN AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 8319608 | APPARATUS AND METHOD FOR CONTROLLING ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8320201 | METHOD OF READING MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | 8320258 | METHOD AND DEVICE FOR RECOGNIZING A SYNCHRONIZATION MESSAGE FROM A WIRELESS TELECOMMUNICATION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8320460 | DYADIC SPATIAL RE-SAMPLING FILTERS FOR INTER-LAYER TEXTURE PREDICTIONS IN SCALABLE IMAGE PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 8321170 | OFFSET ERROR AUTOMATIC CALIBRATION INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8321603 | RECHARGEABLE DEVICE AND METHOD FOR DETERMINING UNIVERSAL SERIAL BUS PORT TYPE |
| FREESCALE SEMICONDUCTOR, INC. | 8321649 | MEMORY CONTROLLER ADDRESS AND DATA PIN MULTIPLEXING |
| FREESCALE SEMICONDUCTOR, INC. | 8324064 | METHODS FOR FORMING VARACTOR DIODES |
| FREESCALE SEMICONDUCTOR, INC. | 8324104 | SURFACE TREATMENT IN SEMICONDUCTOR MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | 8324882 | PHASE LOCKED LOOP DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 8324977 | OSCILLATOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8325280 | DYNAMIC COMPENSATION OF DISPLAY BACKLIGHT BY ADAPTIVELY ADJUSTING A SCALING FACTOR BASED ON MOTION |
| FREESCALE SEMICONDUCTOR, INC. | 8327082 | SNOOP REQUEST ARBITRATION IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8327092 | MEMORY DEVICE CONFIGURABLE AS INTERLEAVED OR NON-INTERLEAVED MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 8327532 | METHOD AND SYSTEM FOR RELEASING A MICROELECTRONIC ASSEMBLY FROM A CARRIER SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 8329509 | PACKAGING PROCESS TO CREATE WETTABLE LEAD FLANK DURING BOARD ASSEMBLY |
| FREESCALE SEMICONDUCTOR, INC. | 8329514 | METHODS FOR FORMING ANTIFUSES WITH CURVED BREAKDOWN REGIONS |
| FREESCALE SEMICONDUCTOR, INC. | 8329543 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING NANOCRYSTALS |
| FREESCALE SEMICONDUCTOR, INC. | 8329544 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING NANOCRYSTALS |
| FREESCALE SEMICONDUCTOR, INC. | 8329579 | THROUGH SUBSTRATE VIAS |
| FREESCALE SEMICONDUCTOR, INC. | 8330220 | LDMOS WITH ENHANCED SAFE OPERATING AREA (SOA) AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8330231 | A TRANSISTOR HAVING GATE DIELECTRIC PROTECTION AND STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 8330239 | SHIELDING FOR A MICRO ELECTRO-MECHANICAL DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8330502 | SYSTEMS AND METHODS FOR DETECTING INTERFERENCE IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8330506 | FREQUENCY MULTIPLIER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8330526 | LOW VOLTAGE DETECTOR |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8332620 | SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR EXECUTING A HIGH LEVEL PROGRAMMING LANGUAGE CONDITIONAL STATEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 8332641 | AUTHENTICATED DEBUG ACCESS FOR FIELD RETURNS |
| FREESCALE SEMICONDUCTOR, INC. | 8334575 | SEMICONDUCTOR DEVICE AND ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8335881 | METHOD AND APPARATUS FOR HANDLING AN INTERRUPT DURING TESTING OF A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8338236 | VENTED SUBSTRATE FOR SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8338828 | SEMICONDUCTOR PACKAGE AND METHOD OF TESTING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8338872 | ELECTRONIC DEVICE WITH CAPCITIVELY COUPLED FLOATING BURIED LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 8339105 | POWER MANAGEMENT ARRANGEMENT FOR A MOBILE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8339117 | START-UP CIRCUIT ELEMENT FOR A CONTROLLED ELECTRICAL SUPPLY |
| FREESCALE SEMICONDUCTOR, INC. | 8339152 | TEST STRUCTURE ACTIVATED BY PROBE NEEDLE |
| FREESCALE SEMICONDUCTOR, INC. | 8339177 | MULTIPLE FUNCTION POWER DOMAIN LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | 8339302 | ANALOG-TO-DIGITAL CONVERTER HAVING A COMPARATOR FOR A MULTI- STAGE SAMPLING CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8339474 | GAIN CONTROLLED THRESHOLD IN DENOISING FILTER IMAGE SIGNAL PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 8339838 | IN-LINE REGISTER FILE BITCELL |
| FREESCALE SEMICONDUCTOR, INC. | 8340021 | WIRELESS COMMUNICATION UNIT |
| FREESCALE SEMICONDUCTOR, INC. | 8340622 | ARRANGEMENT OF RADIOFREQUENCY INTEGRATED CIRCUIT AND METHOD FOR MANUFACTURING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 8340952 | POWER ESTIMATION METHOD AND DEVICE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8341301 | DEVICE AND METHOD FOR TESTING A DIRECT MEMORY ACCESS CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | 8341322 | DEVICE AND METHOD FOR SCHEDULING TRANSACTIONS OVER A DEEP PIPELINED COMPONENT |
| FREESCALE SEMICONDUCTOR, INC. | 8341372 | EMULATED ELECTRICALLY ERASABLE (EEE) MEMORY AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 8341443 | SYSTEM AND METHOD FOR SECURE REAL TIME CLOCKS |
| FREESCALE SEMICONDUCTOR, INC. | 8343842 | METHOD FOR REDUCING PLASMA DISCHARGE DAMAGE DURING PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 8344443 | SINGLE POLY NVM DEVICES AND ARRAYS |
| FREESCALE SEMICONDUCTOR, INC. | 8344472 | SEMICONDUCTOR DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 8344481 | BIPOLAR TRANSISTORS WITH HUMP REGIONS |
| FREESCALE SEMICONDUCTOR, INC. | 8344503 | 3-D CIRCUITS WITH INTEGRATED PASSIVE DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 8344713 | LDO LINEAR REGULATOR WITH IMPROVED TRANSIENT RESPONSE |
| FREESCALE SEMICONDUCTOR, INC. | 8344779 | COMPARATOR CIRCUIT WITH HYSTERESIS, TEST CIRCUIT, AND METHOD FOR TESTING |
| FREESCALE SEMICONDUCTOR, INC. | 8344798 | CORRELATED-DOUBLE-SAMPLING SWITCHED-CAPACITOR GAIN STAGES, SYSTEMS IMPLEMENTING THE GAIN STAGES, AND METHODS OF THEIR OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 8345155 | INTEGRATED CIRCUIT COMPRISING DEFLICKER UNIT FOR FILTERING IMAGE DATA, AND A METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8345469 | STATIC RANDOM ACCESS MEMORY (SRAM) HAVING BIT CELLS ACCESSIBLE BY SEPARATE READ AND WRITE PATHS |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8345485 | ERASE RAMP PULSE WIDTH CONTROL FOR NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 8349666 | FUSED BUSS FOR PLATING FEATURES ON A SEMICONDUCTOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | 8350592 | SINGLE SUPPLY DIGITAL VOLTAGE LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | 8350631 | RELAXATION OSCILLATOR WITH LOW POWER CONSUMPTION |
| FREESCALE SEMICONDUCTOR, INC. | 8350921 | VIDEO PROCESSING SYSTEM, INTEGRATED CIRCUIT, SYSTEM FOR DISPLAYING VIDEO, SYSTEM FOR GENERATING VIDEO, METHOD FOR CONFIGURING A VIDEO PROCESSING SYSTEM, AND COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | 8351168 | OPEN CIRCUIT DETECTOR AND METHOD THEREFORE |
| FREESCALE SEMICONDUCTOR, INC. | 8351276 | SOFT PROGRAM OF A NON-VOLATILE MEMORY BLOCK |
| FREESCALE SEMICONDUCTOR, INC. | 8351291 | ELECTRICALLY PROGRAMMABLE FUSE MODULE IN SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8352428 | NETWORK FILE UPDATE MECHANISM WITH INTEGRITY ASSURANCE |
| FREESCALE SEMICONDUCTOR, INC. | 8352813 | TRANSITION FAULT TESTING FOR A NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 8354325 | METHOD FOR FORMING A TOROIDAL INDUCTOR IN A SEMICONDUCTOR SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 8354739 | THIN SEMICONDUCTOR PACKAGE AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8354866 | PLL START-UP CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8354879 | POWER SWITCH FOR DECREASED RAMP RATE |
| FREESCALE SEMICONDUCTOR, INC. | 8355294 | SYNCHRONOUS DATA PROCESSING SYSTEM FOR RELIABLE TRANSFER OF DATA IRRESPECTIVE OF PROPAGATION DELAYS AND PROCESS, VOLTAGE AND TEMPERATURE (PVT) VARIATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 8355435 | TRANSMISSION OF PACKET DATA |
| FREESCALE SEMICONDUCTOR, INC. | 8356239 | SELECTIVE CACHE WAY MIRRORING |
| FREESCALE SEMICONDUCTOR, INC. | 8358589 | BUFFER MODULE, RECEIVER, DEVICE AND BUFFERING METHOD USING WINDOWS |
| FREESCALE SEMICONDUCTOR, INC. | 8359346 | HASH FUNCTION FOR HARDWARE IMPLEMENTATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 8359927 | MOLDED DIFFERENTIAL PRT PRESSURE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | 8362814 | DATA PROCESSING SYSTEM HAVING BROWN-OUT DETECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8362833 | AMPLIFIER CIRCUITRY, INTEGRATED CIRCUIT AND COMMUNICATION UNIT |
| FREESCALE SEMICONDUCTOR, INC. | 8363491 | PROGRAMMING A NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 8363504 | DEVICE AND METHOD FOR STATE RETENTION POWER GATING |
| FREESCALE SEMICONDUCTOR, INC. | 8363766 | DEVICE AND METHOD OF SYNCHRONIZING SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 8364896 | METHOD AND APPARATUS FOR CONFIGURING A UNIFIED CACHE BASED ON AN ASSOCIATED ERROR RATE |
| FREESCALE SEMICONDUCTOR, INC. | 8364934 | MICROPROCESSOR AND METHOD FOR REGISTER ADDRESSING THEREIN |
| FREESCALE SEMICONDUCTOR, INC. | 8365036 | SOFT ERROR CORRECTION IN A MEMORY ARRAY AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 8368172 | FUSED BUSS FOR PLATING FEATURES ON A SEMICONDUCTOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | 8368360 | METHOD AND APPARATUS FOR REGULATING A FIELD CURRENT FOR AN ALTERNATOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8368383 | METHOD FOR TESTING A VARIABLE DIGITAL DELAY LINE AND A DEVICE HAVING VARIABLE DIGITAL DELAY LINE TESTING CAPABILITIES |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8368657 | TOUCH SENSOR PANEL USING REGIONAL AND LOCAL ELECTRODES TO INCREASE NUMBER OF SENSE LOCATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 8369053 | DISCHARGE PROTECTION APPARATUS AND METHOD OF PROTECTING AN ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8369804 | WIRELESS COMMUNICATION UNIT, SEMICONDUCTOR DEVICE AND POWER CONTROL METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8369844 | DEVICE AND METHOD FOR TRANSMITTING DATA IN A WIDEBAND WIRELESS NETWORK AND COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | 8372699 | METHOD FOR FORMING A SPLIT-GATE MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | 8373221 | NANOCLUSTER CHARGE STORAGE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8373435 | METHOD AND APPARATUS FOR HANDLING AN OUTPUT MISMATCH |
| FREESCALE SEMICONDUCTOR, INC. | 8373460 | DUAL LOOP PHASE LOCKED LOOP WITH LOW VOLTAGE-CONTROLLED OSCILLATOR GAIN |
| FREESCALE SEMICONDUCTOR, INC. | 8373643 | FREQUENCY SYNTHESIS AND SYNCHRONIZATION FOR LED DRIVERS |
| FREESCALE SEMICONDUCTOR, INC. | 8373953 | DISTRIBUTION OF ELECTROSTATIC DISCHARGE (ESD) CIRCUITRY WITHIN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8377793 | METHOD FOR MANUFACTURING A NON-VOLATILE MEMORY, NON-VOLATILE MEMORY DEVICE, AND AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8378433 | SEMICONDUCTOR DEVICE WITH A CONTROLLED CAVITY AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 8378435 | PRESSURE SENSOR AND METHOD OF ASSEMBLING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8378648 | LINEAR REGULATOR WITH AUTOMATIC EXTERNAL PASS DEVICE DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | 8378725 | ADAPTIVE BANDWIDTH PHASE-LOCKED LOOP |
| FREESCALE SEMICONDUCTOR, INC. | 8378728 | LEVEL SHIFTING FLIP-FLOP |
| FREESCALE SEMICONDUCTOR, INC. | 8378735 | DIE TEMPERATURE SENSOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8378865 | METHOD OF TESTING DIGITAL-TO-ANALOG AND ANALOG-TO-DIGITAL CONVERTERS |
| FREESCALE SEMICONDUCTOR, INC. | 8379466 | INTEGRATED CIRCUIT HAVING AN EMBEDDED MEMORY AND METHOD FOR TESTING THE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 8379468 | WORD LINE FAULT DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | 8379627 | WIRELESS COMMUNICATION DEVICE, INTEGRATED CIRCUIT AND METHOD OF TIMING SYNCHRONISATION |
| FREESCALE SEMICONDUCTOR, INC. | 8379671 | TECHNIQUES FOR EXTRACTING A CONTROL CHANNEL FROM A RECEIVED SIGNAL IN A WIRELESS COMMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8379846 | ENCRYPTION APPARATUS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8379861 | INTEGRATED CIRCUIT AND A METHOD FOR SECURE TESTING |
| FREESCALE SEMICONDUCTOR, INC. | 8380768 | RANDOM NUMBER GENERATOR |
| FREESCALE SEMICONDUCTOR, INC. | 8380779 | TECHNIQUE FOR DETERMINING IF A LOGICAL SUM OF A FIRST OPERAND AND A SECOND OPERAND IS THE SAME AS A THIRD OPERAND |
| FREESCALE SEMICONDUCTOR, INC. | 8380918 | NON-VOLATILE STORAGE ALTERATION TRACKING |
| FREESCALE SEMICONDUCTOR, INC. | 8381009 | DEVICE AND METHOD FOR POWER MANAGEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 8382153 | CHILD CAR SEAT FOR A LAND VEHICLE |
| FREESCALE SEMICONDUCTOR, INC. | 8384168 | SENSOR DEVICE WITH SEALING STRUCTURE |
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FREESCALE SEMICONDUCTOR, INC. 8384184 LATERALLY DIFFUSED METAL OXIDE SEMICONDUCTOR DEVICE

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| FREESCALE SEMICONDUCTOR, INC. | 8384193 | BIPOLAR TRANSISTOR WITH TWO DIFFERENT EMITTER PORTIONS HAVING SAME TYPE DOPANT OF DIFFERENT CONCENTRATIONS FOR IMPORVED GAIN |
| FREESCALE SEMICONDUCTOR, INC. | 8384313 | SYSTEM AND METHOD TO IMPROVE SWITCHING IN POWER SWITCHING APPLICATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 8384437 | METHOD AND APPARATUS FOR GATING A CLOCK SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 8384575 | CONFIGURABLE CONTINUOUS TIME SIGMA DELTA ANALOG-TO-DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 8384579 | SYSTEMS AND METHODS FOR DATA CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | 8385084 | SHIELDING STRUCTURES FOR SIGNAL PATHS IN ELECTRONIC DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 8386552 | FOURIER TRANSFORM PROCESSING AND TWIDDLE FACTOR GENERATION |
| FREESCALE SEMICONDUCTOR, INC. | 8386747 | PROCESSOR AND METHOD FOR DYNAMIC AND SELECTIVE ALTERATION OF ADDRESS TRANSLATION |
| FREESCALE SEMICONDUCTOR, INC. | 8387464 | LATERALLY INTEGRATED MEMS SENSOR DEVICE WITH MULTI-STIMULUS SENSING |
| FREESCALE SEMICONDUCTOR, INC. | 8389365 | NON-VOLATILE MEMORY AND LOGIC CIRCUIT PROCESS INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | 8389366 | RESURF SEMICONDUCTOR DEVICE CHARGE BALANCING |
| FREESCALE SEMICONDUCTOR, INC. | 8390026 | ELECTRONIC DEVICE INCLUDING A HETEROJUNCTION REGION |
| FREESCALE SEMICONDUCTOR, INC. | 8390071 | ESD PROTECTION WITH INCREASED CURRENT CAPABILITY |
| FREESCALE SEMICONDUCTOR, INC. | 8390091 | SEMICONDUCTOR STRUCTURE, AN INTEGRATED CIRCUIT INCLUDING A SEMICONDUCTOR STRUCTURE AND A METHOD FOR MANUFACTURING A SEMICONDUCTOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 8390092 | AREA-EFFICIENT HIGH VOLTAGE BIPOLAR-BASED ESD PROTECTION TARGETING NARROW DESIGN WINDOWS |
| FREESCALE SEMICONDUCTOR, INC. | 8390347 | SINGLE PERIOD PHASE TO DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 8390354 | DELAY CONFIGURABLE DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 8390369 | ELECTRONIC CIRCUIT AND METHOD FOR OPERATING A MODULE IN A FUNCTIONAL MODE AND IN AN IDLE MODE |
| FREESCALE SEMICONDUCTOR, INC. | 8391415 | ELECTRONIC DEVICE, INTEGRATED CIRCUIT AND METHOD FOR SELECTING OF AN OPTIMAL SAMPLING CLOCK PHASE |
| FREESCALE SEMICONDUCTOR, INC. | 8394713 | METHOD OF IMPROVING ADHESION OF BOND PAD OVER PAD METALLIZATION WITH A NEIGHBORING PASSIVATION LAYER BY DEPOSITING A PALLADIUM LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 8395872 | CURRENT DRIVER CIRCUIT AND METHOD OF OPERATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8397006 | ARBITRATION SCHEME FOR ACCESSING A SHARED RESOURCE |
| FREESCALE SEMICONDUCTOR, INC. | 8397081 | DEVICE AND METHOD FOR SECURING SOFTWARE |
| FREESCALE SEMICONDUCTOR, INC. | 8397571 | OUTPUT CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8398304 | MULTIPLE SENSOR THERMAL MANAGEMENT FOR ELECTRONIC DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 8399310 | NON-VOLATILE MEMORY AND LOGIC CIRCUIT PROCESS INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | 8400213 | COMPLEMENTARY BAND-GAP VOLTAGE REFERENCE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8400339 | CORRELATED-LEVEL-SHIFTING AND CORRELATED-DOUBLE-SAMPLING SWITCHED-CAPACITOR GAIN STAGES, SYSTEMS IMPLEMENTING THE GAIN STAGES, AND METHODS OF THEIR OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 8400819 | INTEGRATED CIRCUIT HAVING VARIABLE MEMORY ARRAY POWER SUPPLY VOLTAGE |
| | 8400859 | |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8400995 | SYSTEM AND METHOD FOR DESCRAMBLING DATA |
| FREESCALE SEMICONDUCTOR, INC. | 8401019 | METHOD, INTEGRATED CIRCUIT, AND COMMUNICATION UNIT FOR SCHEDULING A PROCESSING OF PACKET STREAM CHANNELS |
| FREESCALE SEMICONDUCTOR, INC. | 8401140 | PHASE/FREQUENCY DETECTOR FOR A PHASE-LOCKED LOOP THAT SAMPLES ON BOTH RISING AND FALLING EDGES OF A REFERENCE SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 8402258 | DEBUG MESSAGE GENERATION USING A SELECTED ADDRESS TYPE |
| FREESCALE SEMICONDUCTOR, INC. | 8402288 | APPARATUS AND METHOD FOR CONTROLLING VOLTAGE AND FREQUENCY USING MULTIPLE REFERENCE CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 8402327 | MEMORY SYSTEM WITH ERROR CORRECTION AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 8404594 | REVERSE ALD |
| FREESCALE SEMICONDUCTOR, INC. | 8405423 | FLEXIBLE BUS DRIVER |
| FREESCALE SEMICONDUCTOR, INC. | 8406113 | PEAK-TO-AVERAGE REDUCTION OF SC-FDMA SIGNALS WITH FREQUENCY MASK |
| FREESCALE SEMICONDUCTOR, INC. | 8406702 | CLOCK SIGNAL GENERATING ARRANGEMENT FOR A COMMUNICATION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8407457 | SYSTEM AND METHOD FOR MONITORING DEBUG EVENTS |
| FREESCALE SEMICONDUCTOR, INC. | 8407509 | METHOD FOR COMPENSATING FOR VARIATIONS IN DATA TIMING |
| FREESCALE SEMICONDUCTOR, INC. | 8407890 | METHOD OF MANUFACTURING AN ELECTRONIC DEVICE MODULE WITH INTEGRATED ANTENNA STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 8410580 | DEVICE HAVING CONDUCTIVE SUBSTRATE VIA WITH CATCH-PAD ETCH-STOP |
| FREESCALE SEMICONDUCTOR, INC. | 8410763 | CONTROLLER FOR BUCK AND BOOST CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 8412132 | TECHNIQUES FOR ADAPTIVE PREDISTORTION DIRECT CURRENT OFFSET CORRECTION IN A TRANSMITTER |
| FREESCALE SEMICONDUCTOR, INC. | 8413033 | DEVICE AND METHOD FOR CALCULATING BACKWARD STATE METRICS OF A TRELLIS |
| FREESCALE SEMICONDUCTOR, INC. | 8413153 | METHOD AND SYSTEMS FOR SHARING COMMON JOB INFORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 8413509 | SPRING MEMBER FOR USE IN A MICROELECTROMECHANICAL SYSTEMS SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | 8415203 | METHOD OF FORMING A SEMICONDUCTOR PACKAGE INCLUDING TWO DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 8415217 | PATTERNING A GATE STACK OF A NON-VOLATILE MEMORY (NVM) WITH FORMATION OF A CAPACITOR |
| FREESCALE SEMICONDUCTOR, INC. | 8415255 | PORE SEALING AND CLEANING POROUS LOW DIELECTRIC CONSTANT STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | 8415779 | LEAD FRAME FOR SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 8415940 | TEMPERATURE COMPENSATION CIRCUIT AND METHOD FOR GENERATING A VOLTAGE REFERENCE WITH A WELL-DEFINED TEMPERATURE BEHAVIOR |
| FREESCALE SEMICONDUCTOR, INC. | 8416216 | METHOD AND SYSTEM FOR TOUCH SENSOR INTERACE FAULT DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | 8416969 | AMPLIFIER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8417842 | VIRTUAL MEMORY DIRECT ACCESS (DMA) CHANNEL TECHNIQUE WITH MULTIPLE ENGINES FOR DMA CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | 8417924 | DATA PROCESSING DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 8420480 | PATTERNING A GATE STACK OF A NON-VOLATILE MEMORY (NVM) WITH FORMATION OF A GATE EDGE DIODE |
| FREESCALE SEMICONDUCTOR, INC. | 8421587 | DIAGNOSIS FOR MIXED SIGNAL DEVICE FOR USE IN A DISTRIBUTED SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8423721 | CACHE COHERENCY PROTOCOL IN A DATA PROCESSING SYSTEM |
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| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8426263 | PATTERNING A GATE STACK OF A NON-VOLATILE MEMORY (NVM) WITH FORMATION OF A METAL-OXIDE-SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET) |
| FREESCALE SEMICONDUCTOR, INC. | 8426310 | METHOD OF FORMING A SHARED CONTACT IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8427877 | DIGITAL METHOD TO OBTAIN THE I-V CURVES OF NVM BITCELLS |
| FREESCALE SEMICONDUCTOR, INC. | 8429321 | REQUEST CONTROLLER, PROCESSING UNIT, METHOD FOR CONTROLLING REQUESTS AND COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | 8430562 | DEVICE AND METHOD FOR EVALUATING A TEMPERATURE |
| FREESCALE SEMICONDUCTOR, INC. | 8431471 | METHOD FOR INTEGRATING A NON-VOLATILE MEMORY (NVM) |
| FREESCALE SEMICONDUCTOR, INC. | 8431970 | INTEGRATED CIRCUITS WITH EDGE-ADJACENT DEVICES HAVING REACTANCE VALUES |
| FREESCALE SEMICONDUCTOR, INC. | 8432189 | DIGITAL VOLTAGE LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | 8432200 | SELF-TRACKING ADAPTIVE BANDWIDTH PHASE-LOCKED LOOP |
| FREESCALE SEMICONDUCTOR, INC. | 8432201 | PHASE-LOCKED LOOP (PLL) CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8432209 | METHOD FOR POWER REDUCTION AND A DEVICE HAVING POWER REDUCTION CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 8432214 | PROGRAMMABLE TEMPERATURE SENSING CIRCUIT FOR AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8432309 | AUTOMOTIVE RADAR SYSTEM AND METHOD FOR USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8432654 | MULTI-VOLTAGE ELECTROSTATIC DISCHARGE PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 8432752 | ADAPTIVE WRITE PROCEDURES FOR NON-VOLATILE MEMORY USING VERIFY READ |
| FREESCALE SEMICONDUCTOR, INC. | 8432960 | DIGITAL ADAPTIVE CHANNEL EQUALIZER |
| FREESCALE SEMICONDUCTOR, INC. | 8433263 | WIRELESS COMMUNICATION UNIT, INTEGRATED CIRCUIT AND METHOD OF POWER CONTROL OF A POWER AMPLIFIER THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8433967 | METHOD AND SYSTEM FOR DETECTING RETRANSMISSION THRESHOLD CONDITION IN SELECTIVE REPEAT ARQ COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8435874 | METHOD OF FORMING OPENINGS IN A SEMICONDUCTOR DEVICE AND A SEMICONDUCTOR DEVICE FABRICATED BY THE METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 8435898 | A FIRST INTER-LAYER DIELECTRIC STACK FOR NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 8436582 | BATTERY CELL EQUALIZER SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8436597 | VOLTAGE REGULATOR WITH AN EMITTER FOLLOWER DIFFERENTIAL AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 8438327 | RECOVERY SCHEME FOR AN EMULATED MEMORY SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8438419 | FAULT MANAGEMENT FOR A COMMUNICATION BUS |
| FREESCALE SEMICONDUCTOR, INC. | 8438442 | METHOD AND APPARATUS FOR TESTING A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8438547 | ADDRESS TRANSLATION TRACE MESSAGE GENERATION FOR DEBUG |
| FREESCALE SEMICONDUCTOR, INC. | 8438572 | TASK SCHEDULING METHOD AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 8440507 | LEAD FRAME SULFUR REMOVAL |
| FREESCALE SEMICONDUCTOR, INC. | 8440539 | ISOLATION TRENCH PROCESSING FOR STRAIN CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 8441324 | VOLTAGE-CONTROLLED OSCILLATOR AND RADAR SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8441525 | METHOD FOR SYNCHRONIZING REMOTE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8442456 | WIRELESS COMMUNICATION UNIT, INTEGRATED CIRCUIT AND METHOD OF POWER CONTROL THEREIN |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8443224 | APPARATUS AND METHOD FOR DECOUPLING ASYNCHRONOUS CLOCK DOMAINS |
| FREESCALE SEMICONDUCTOR, INC. | 8443326 | SCAN CHAIN RE-ORDERING IN ELECTRONIC CIRCUIT DESIGN BASED ON REGION CONGESTION IN LAYOUT PLAN |
| FREESCALE SEMICONDUCTOR, INC. | 8445939 | METHOD OF FORMING A SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8446176 | RECONFIGURABLE ENGINEERING CHANGE ORDER BASE CELL |
| FREESCALE SEMICONDUCTOR, INC. | 8446228 | OSCILLATOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8447004 | ESTIMATION AND COMPENSATION OF CLOCK VARIATION IN RECEIVED SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 8447245 | RADIO FREQUENCY TRANSMITTER HAVING AN AMPLIFIER WITH POWER SUPPLY MODULATION |
| FREESCALE SEMICONDUCTOR, INC. | 8447897 | BANDWIDTH CONTROL FOR A DIRECT MEMORY ACCESS UNIT WITHIN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8448114 | METHOD FOR DUAL EDGE CLOCK AND BUFFER TREE SYNTHESIS |
| FREESCALE SEMICONDUCTOR, INC. | 8448513 | ROTARY DISK GYROSCOPE |
| FREESCALE SEMICONDUCTOR, INC. | 8450841 | BONDED WIRE SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8451936 | METHOD AND SYSTEM FOR PERFORMING DISTANCE MEASURING AND DIRECTION FINDING USING ULTRAWIDE BANDWIDTH TRANSMISSIONS |
| FREESCALE SEMICONDUCTOR, INC. | 8452553 | DEVICE AND METHOD FOR TESTING A CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8452999 | DATA PROCESSOR PERFORMANCE PREDICTION |
| FREESCALE SEMICONDUCTOR, INC. | 8453135 | COMPUTATION REUSE FOR LOOPS WITH IRREGULAR ACCESSES |
| FREESCALE SEMICONDUCTOR, INC. | 8455286 | METHOD OF MAKING A MICRO-ELECTRO-MECHANICAL-SYSTEMS (MEMS) DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8455306 | METHODS OF FORMING VOLTAGE LIMITING DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 8456023 | SEMICONDUCTOR WAFER PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 8456337 | SYSTEM TO INTERFACE ANALOG-TO-DIGITAL CONVERTERS TO INPUTS WITH ARBITRARY COMMON-MODES |
| FREESCALE SEMICONDUCTOR, INC. | 8456529 | DEVICE AND METHOD FOR EVALUATING CONNECTIVITY BETWEEN A VIDEO DRIVER AND A DISPLAY |
| FREESCALE SEMICONDUCTOR, INC. | 8456783 | INTEGRATED CIRCUIT, ELECTRONIC DEVICE AND ESD PROTECTION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8456784 | OVERVOLTAGE PROTECTION CIRCUIT FOR AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8456935 | MEMORY AND METHOD FOR SENSING DATA IN A MEMORY USING COMPLEMENTARY SENSING SCHEME |
| FREESCALE SEMICONDUCTOR, INC. | 8457301 | MULTI-FREQUENCY TONE DETECTOR |
| FREESCALE SEMICONDUCTOR, INC. | 8458364 | A METHOD FOR RECEIVING AND PROCESSING FRAMES AND A DEVICE HAVING FRAME RECEIVING AND PROCESSING CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 8458407 | DEVICE AND METHOD FOR GENERATING CACHE USER INITIATED PRE-FETCH REQUESTS |
| FREESCALE SEMICONDUCTOR, INC. | 8458447 | BRANCH TARGET BUFFER ADDRESSING IN A DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 8458541 | SYSTEM AND METHOD FOR DEBUGGING SCAN CHAINS |
| FREESCALE SEMICONDUCTOR, INC. | 8458543 | SCAN BASED TEST ARCHITECTURE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 8460972 | METHOD OF FORMING SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 8460996 | SEMICONDUCTOR DEVICES WITH DIFFERENT DIELECTRIC THICKNESSES |
| FREESCALE SEMICONDUCTOR, INC. | 8461012 | DEVICE WITH GROUND PLANE FOR HIGH FREQUENCY SIGNAL TRANSMISSION AND METHOD THEREFOR |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8461626 | HETERO-STRUCTURE FIELD EFFECT TRANSISTOR, INTEGRATED CIRCUIT INCLUDING A HETERO-STRUCTURE FIELD EFFECT TRANSISTOR AND METHOD FOR MANUFACTURING A HETERO-STRUCTURE FIELD EFFECT TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 8461656 | DEVICE STRUCTURES FOR IN-PLANE AND OUT-OF-PLANE SENSING MICRO- ELECTRO-MECHANICAL SYSTEMS (MEMS) |
| FREESCALE SEMICONDUCTOR, INC. | 8461657 | METHODS FOR FORMING A MICRO ELECTRO-MECHANICAL DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8461865 | LOGIC BUILT-IN SELF-TEST SYSTEM AND METHOD FOR APPLYING A LOGIC BUILT-IN SELF-TEST TO A DEVICE UNDER TEST |
| FREESCALE SEMICONDUCTOR, INC. | 8461913 | INTEGRATED CIRCUIT AND A METHOD FOR SELECTING A VOLTAGE IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8461938 | DIRECTIONAL COUPLERS FOR USE IN ELECTRONIC DEVICES, AND METHODS OF USE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 8462141 | UNIFIED MEMORY ARCHITECTURE AND DISPLAY CONTROLLER TO PREVENT DATA FEED UNDER-RUN |
| FREESCALE SEMICONDUCTOR, INC. | 8462578 | CHARGE PUMP CIRCUIT WITH FAST START-UP |
| FREESCALE SEMICONDUCTOR, INC. | 8462597 | DECOUPLING TECHNIQUE FOR OPTICAL DISK DRIVE OPTICAL PICKUP UNITS |
| FREESCALE SEMICONDUCTOR, INC. | 8462818 | METHOD FOR PROCESSING CDMA SIGNALS AND A DEVICE HAVING CDMA SIGNAL CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 8463193 | CALIBRATION APPARATUS AND METHOD OF CALIBRATING A COMMUNICATIONS TERMINAL |
| FREESCALE SEMICONDUCTOR, INC. | 8463196 | METHOD AND DECODER FOR DECODING A WIRELESS TRANSMISSION FROM A PREDEFINED USER |
| FREESCALE SEMICONDUCTOR, INC. | 8463207 | WIRELESS COMMUNICATION UNIT, INTEGRATED CIRCUIT AND METHOD OF POWER CONTROL OF A POWER AMPLIFIER THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8463226 | AMPLIFIERS AND RELATED RECEIVER SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 8464069 | SECURE DATA ACCESS METHODS AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 8464098 | MICROCONTROLLER DEVICE, MICROCONTROLLER DEBUGGING DEVICE, METHOD OF DEBUGGING A MICROCONTROLLER DEVICE, MICROCONTROLLER KIT |
| FREESCALE SEMICONDUCTOR, INC. | 8464117 | SYSTEM FOR TESTING INTEGRATED CIRCUIT WITH ASYNCHRONOUS CLOCK DOMAINS |
| FREESCALE SEMICONDUCTOR, INC. | 8466539 | MRAM DEVICE AND METHOD OF ASSEMBLING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8467338 | SCHEDULING WIRELESS COMMUNICATION |
| FREESCALE SEMICONDUCTOR, INC. | 8467748 | WIRELESS COMMUNICATION UNIT, INTEGRATED CIRCUIT COMPRISING A VOLTAGE CONTROLLED OSCILLATOR AND METHOD OF OPERATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8468024 | GENERATING A FRAME OF AUDIO DATA |
| FREESCALE SEMICONDUCTOR, INC. | 8468887 | RESONANT ACCELEROMETER WITH LOW SENSITIVITY TO PACKAGE STRESS |
| FREESCALE SEMICONDUCTOR, INC. | 8471749 | COMPARATOR |
| FREESCALE SEMICONDUCTOR, INC. | 8473000 | COMMUNICATION DEVICE, INTEGRATED CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8473644 | ACCESS MANAGEMENT TECHNIQUE WITH OPERATION TRANSLATION CAPABILITY |
| FREESCALE SEMICONDUCTOR, INC. | 8473710 | MULTIPLE PARTITIONED EMULATED ELECTRICALLY ERASABLE (EEE) MEMORY AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 8476087 | METHODS FOR FABRICATING SENSOR DEVICE PACKAGE USING A SEALING STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 8476768 | SYSTEM ON A CHIP WITH INTERLEAVED SETS OF PADS |
| FREESCALE SEMICONDUCTOR, INC. | 8476917 | QUIESCENT CURRENT (IDDQ) INDICATION AND TESTING APPARATUS AND METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 8476962 | SYSTEM HAVING MULTIPLE VOLTAGE TIERS AND METHOD THEREFOR |

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8476963 | EXPONENTIAL CHARGE PUMP |
| FREESCALE SEMICONDUCTOR, INC. | 8477052 | METHOD AND APPARATUS FOR SELF-TEST OF SUCCESSIVE APPROXIMATION REGISTER (SAR) A/D CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 8478219 | HETERODYNE RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 8479130 | METHOD OF DESIGNING INTEGRATED CIRCUIT THAT ACCOUNTS FOR DEVICE AGING |
| FREESCALE SEMICONDUCTOR, INC. | 8481369 | METHOD OF MAKING SEMICONDUCTOR PACKAGE WITH IMPROVED STANDOFF |
| FREESCALE SEMICONDUCTOR, INC. | 8481873 | CAPACITIVE TOUCH SENSOR DEVICE CONFIGURATION SYSTEMS AND METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 8482099 | POLY-RESISTOR, AND LINEAR AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 8482266 | VOLTAGE REGULATION CIRCUITRY AND RELATED OPERATING METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 8483384 | ENHANCED TONE DETECTOR INCLUDING ADAPTIVE MULTI-BANDPASS FILTER FOR TONE DETECTION AND ENHANCEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 8483720 | SMART/ACTIVE RFID TAG FOR USE IN A WPAN |
| FREESCALE SEMICONDUCTOR, INC. | 8484453 | DATA PROCESSING SYSTEM HAVING AN OPERATING SYSTEM ADAPTER AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 8484523 | SEQUENTIAL DIGITAL CIRCUITRY WITH TEST SCAN |
| FREESCALE SEMICONDUCTOR, INC. | 8486540 | LEAD FRAME SHEET |
| FREESCALE SEMICONDUCTOR, INC. | 8486839 | METHODS AND APPARATUS TO IMPROVE RELIABILITY OF ISOLATED VIAS |
| FREESCALE SEMICONDUCTOR, INC. | 8487387 | MEMS SENSOR DEVICE WITH MULTI-STIMULUS SENSING |
| FREESCALE SEMICONDUCTOR, INC. | 8487398 | CAPACITOR DEVICE USING AN ISOLATED WELL AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8487656 | DYNAMIC LOGIC CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8487657 | DYNAMIC LOGIC CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8487677 | PHASE LOCKED LOOP WITH ADAPTIVE BIASING |
| FREESCALE SEMICONDUCTOR, INC. | 8487683 | CIRCUIT FOR GENERATING MULTI-PHASE NON-OVERLAPPING CLOCK SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 8487803 | PIPELINED ANALOG-TO-DIGITAL CONVERTER HAVING REDUCED POWER CONSUMPTION |
| FREESCALE SEMICONDUCTOR, INC. | 8487805 | SUCCESSIVE APPROXIMATION ANALOG-TO-DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 8487884 | TOUCH SCREEN DETECTION AND DIAGNOSTICS |
| FREESCALE SEMICONDUCTOR, INC. | 8489404 | METHOD FOR DETECTING AUDIO SIGNAL TRANSIENT AND TIME-SCALE MODIFICATION BASED ON SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8489906 | DATA PROCESSOR HAVING MULTIPLE LOW POWER MODES |
| FREESCALE SEMICONDUCTOR, INC. | 8490046 | Merging Line and Condition Coverage Data |
| FREESCALE SEMICONDUCTOR, INC. | 8493003 | SERIAL CASCADE OF MINIMIUM TAIL VOLTAGES OF SUBSETS OF LED STRINGS FOR DYNAMIC POWER CONTROL IN LED DISPLAYS |
| FREESCALE SEMICONDUCTOR, INC. | 8493034 | CHARGE CONTROL CIRCUIT AND BATTERY CHARGER INCLUDING A CHARGE CONTROL CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8493121 | RECONFIGURABLE FLIP-FLOP |
| FREESCALE SEMICONDUCTOR, INC. | 8493122 | VOLTAGE CLAMPING CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8494102 | METHODS AND APPARATUS FOR ORTHOGONAL MODULATED SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 8495436 | SYSTEM AND METHOD FOR MEMORY TESTING IN ELECTRONIC CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 8496158 | METHOD AND APPARATUS FOR MONITORING FREE AIR BALL (FAB) |

FORMATION IN WIRE BONDING

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8497731 | LOW PASS FILTER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8497786 | CAPACITIVE KEYBOARD WITH ENHANCED ELECTRODE AREAS |
| FREESCALE SEMICONDUCTOR, INC. | 8501517 | METHOD OF ASSEMBLING PRESSURE SENSOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8501539 | SEMICONDUCTOR DEVICE PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 8502287 | SEMICONDUCTOR DEVICES WITH ENCLOSED VOID CAVITIES |
| FREESCALE SEMICONDUCTOR, INC. | 8502324 | SEMICONDUCTOR WAFER HAVING SCRIBE LANE ALIGNMENT MARKS FOR REDUCING CRACK PROPAGATION |
| FREESCALE SEMICONDUCTOR, INC. | 8504777 | DATA PROCESSOR FOR PROCESSING DECORATED INSTRUCTIONS WITH CACHE BYPASS |
| FREESCALE SEMICONDUCTOR, INC. | 8504884 | THRESHOLD VOLTAGE TECHNIQUES FOR DETECTING AN IMMINENT READ FAILURE IN A MEMORY ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | 8504886 | METHOD FOR PARTITIONING SCAN CHAIN |
| FREESCALE SEMICONDUCTOR, INC. | 8508282 | LIN BUS NETWORK, INTEGRATED CIRCUIT AND METHOD OF COMMUNICATING THEREON |
| FREESCALE SEMICONDUCTOR, INC. | 8509001 | ADAPTIVE WRITE PROCEDURES FOR NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 8509370 | PHASE LOCKED LOOP DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 8509857 | IMPROVEMENTS IN OR RELATING TO HEADSETS |
| FREESCALE SEMICONDUCTOR, INC. | 8510482 | DATA PROCESSING SYSTEM HAVING PERIPHERAL-PACED DMA TRANSFER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8510581 | ANTICIPATION OF POWER ON OF A MOBILE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8510695 | TECHNIQUES FOR ELECTROMIGRATION STRESS DETERMINATION IN INTERCONNECTS OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8511170 | PRESSURE TRANSDUCER HAVING STRUCTURE FOR MONITORING SURFACE CHARGE |
| FREESCALE SEMICONDUCTOR, INC. | 8513066 | A METHOD OF MAKING AN INVERTED-T CHANNEL TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 8513734 | SWITCH MODE CONVERTER EMPLOYING DUAL GATE MOS TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 8513982 | SAMPLE AND HOLD CIRCUIT AND DIFFERENTIAL SAMPLE AND HOLD CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8514007 | ADJUSTABLE POWER SPLITTER AND CORRESPONDING METHODS AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 8514530 | LOAD CONTROL AND PROTECTION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8514611 | MEMORY WITH LOW VOLTAGE MODE OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 8514785 | COMMON RF INTERFACE FOR SEPARATING AND MIXING WIRELESS SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 8515372 | RECEIVER CONFIGURABLE IN A PLURALITY OF MODES |
| FREESCALE SEMICONDUCTOR, INC. | 8516213 | METHOD AND APPARATUS FOR EEPROM EMULATION FOR PREVENTING DATA LOSS IN THE EVENT OF A FLASH BLOCK FAILURE |
| FREESCALE SEMICONDUCTOR, INC. | 8518764 | SEMICONDUCTOR STRUCTURE HAVING A THROUGH SUBSTRATE VIA (TSV) AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 8519513 | SEMICONDUCTOR WAFER PLATING BUS |
| FREESCALE SEMICONDUCTOR, INC. | 8519519 | SEMICONDUCTOR DEVICE HAVING DIE PADS ISOLATED FROM INTERCONNECT PORTION AND METHOD OF ASSEMBLING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8519768 | CLOCK GLITCH DETECTION |
| | | |

8519780 CHARGE PUMP VOLTAGE REGULATOR

FREESCALE SEMICONDUCTOR, INC.

| Owner | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8521463 | SYSTEM FOR PERFORMING ELECTRICAL CHARACTERIZATION OF ASYNCHRONOUS INTEGRATED CIRCUIT INTERFACES |
| FREESCALE SEMICONDUCTOR, INC. | 8522089 | METHOD OF TESTING ASYNCHRONOUS MODULES IN SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8522183 | STATIC TIMING ANALYSIS ADJUSTMENTS FOR AGING EFFECTS |
| FREESCALE SEMICONDUCTOR, INC. | 8524529 | BRACE FOR WIRE BOND |
| FREESCALE SEMICONDUCTOR, INC. | 8524557 | INTEGRATION TECHNIQUE USING THERMAL OXIDE SELECT GATE DIELECTRIC FOR SELECT GATE AND REPLACEMENT GATE FOR LOGIC |
| FREESCALE SEMICONDUCTOR, INC. | 8525311 | LEAD FRAME FOR SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8525316 | EUTECTIC FLOW CONTAINMENT IN A SEMICONDUCTOR FABRICATION PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | 8525597 | CLOCK FREQUENCY OVERSHOOT DETECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8525598 | DIGITAL TO ANALOG CONVERTER FOR PHASE LOCKED LOOP |
| FREESCALE SEMICONDUCTOR, INC. | 8525721 | LOW POWER CYCLE DATA CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 8526539 | COMPUTATIONAL GENERATION OF NARROW-BANDWIDTH DIGITAL SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 8526708 | MEASUREMENT OF CRITICAL DIMENSIONS OF SEMICONDUCTOR WAFERS |
| FREESCALE SEMICONDUCTOR, INC. | 8526756 | A METHOD AND SYSTEM ARRANGED FOR FILTERING AN IMAGE |
| FREESCALE SEMICONDUCTOR, INC. | 8527681 | DATA PROCESSING SYSTEM, DATA PROCESSING METHOD, AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 8527933 | LAYOUT TECHNIQUE FOR STRESS MANAGEMENT CELLS |
| FREESCALE SEMICONDUCTOR, INC. | 8527935 | SYSTEM FOR REDUCING POWER CONSUMPTION OF ELECTRONIC CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8530346 | PROCESS OF FORMING AN ELECTRONIC DEVICE INCLUDING A CONDUCTIVE STUD OVER A BONDING PAD REGION |
| FREESCALE SEMICONDUCTOR, INC. | 8530347 | ELECTRONIC DEVICE INCLUDING INTERCONNECTS WITH A CAVITY THEREBETWEEN AND A PROCESS OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8530950 | METHODS AND STRUCTURES FOR SPLIT GATE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 8530953 | POWER MOS TRANSISTOR DEVICE AND SWITCH APPARATUS COMPRISING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 8530972 | DOUBLE GATE MOSFET WITH COPLANAR SURFACES FOR CONTACTING SOURCE, DRAIN, AND BOTTOM GATE |
| FREESCALE SEMICONDUCTOR, INC. | 8531005 | DEVICES WITH ZENER TRIGGERED ESD PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 8531194 | SELECTABLE THRESHOLD RESET CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8531197 | AN INTEGRATED CIRCUIT DIE, AN INTEGRATED CIRCUIT PACKAGE AND A METHOD FOR CONNECTING AN INTEGRATED CIRCUIT DIE TO AN EXTERNAL DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8531324 | SYSTEMS AND METHODS FOR DATA CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | 8531899 | METHODS FOR TESTING A MEMORY EMBEDDED IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 8532225 | DC COMPENSATION FOR VLIF SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 8532424 | METHOD AND SYSTEM FOR FILTERING IMAGE DATA |
| FREESCALE SEMICONDUCTOR, INC. | 8532583 | SEMICONDUCTOR DEVICE, WIRELESS COMMUNICATION DEVICE AND METHOD FOR GENERATING A SYNTHESIZED FREQUENCY SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 8533400 | SELECTIVE MEMORY ACCESS TO DIFFERENT LOCAL MEMORY PORTS AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 8533441 | METHOD FOR MANAGING BRANCH INSTRUCTIONS AND A DEVICE HAVING BRANCH INSTRUCTION MANAGEMENT CAPABILITIES |

| <u>Owner</u> | Patent # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 8533544 | SYSTEM FOR TREE SEQUENCE TESTING OF A DEVICE AND METHOD FOR TREE SEQUENCE TESTING OF A DEVICE IN A TEST FRAMEWORK ARCHITECTURE |
| FREESCALE SEMICONDUCTOR, INC. | 8533578 | ERROR DETECTION IN A CONTENT ADDRESSABLE MEMORY (CAM) AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 8535982 | PROVIDING AN AUTOMATIC OPTICAL INSPECTION FEATURE FOR SOLDER JOINTS ON SEMICONDUCTOR PACKAGES |
| FREESCALE SEMICONDUCTOR, INC. | 8536006 | LOGIC AND NON-VOLATILE MEMORY (NVM) INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | 8536007 | NON-VOLATILE MEMORY CELL AND LOGIC TRANSISTOR INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | 8536684 | METHOD OF ASSEMBLING SHIELDED INTEGRATED CIRCUIT DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 8536697 | PACKAGED DIE FOR HEAT DISSIPATION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8537512 | ESD PROTECTION USING ISOLATED DIODES |
| FREESCALE SEMICONDUCTOR, INC. | 8537519 | SEMICONDUCTOR DEVICE AND METHOD OF ELECTROSTATIC DISCHARGE PROTECTION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 8537625 | MEMORY VOLTAGE REGULATOR WITH LEAKAGE CURRENT VOLTAGE CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 8539485 | POLLING USING RESERVATION MECHANISM |
| FREESCALE SEMICONDUCTOR, INC. | 8539836 | MEMS SENSOR WITH DUAL PROOF MASSES |
| FREESCALE SEMICONDUCTOR, INC. | 8541862 | SEMICONDUCTOR DEVICE WITH SELF-BIASED ISOLATION |
| FREESCALE SEMICONDUCTOR, INC. | 8542048 | DOUBLE EDGE TRIGGERED FLIP FLOP |
| FREESCALE SEMICONDUCTOR, INC. | 8542642 | CHANNEL CONDITION DEPENDENT SCHEDULING |
| FREESCALE SEMICONDUCTOR, INC. | 8543766 | WRITING DATA TO SYSTEM MEMORY IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 8543856 | SEMICONDUCTOR DEVICE WITH WAKE-UP UNIT |
| FREESCALE SEMICONDUCTOR, INC. | 8543860 | MULTI-CORE CLOCKING SYSTEM WITH INTERLOCKED 'ANTI-FREEZE' MECHANISM |

Freescale Semiconductor, Inc. – Patent Applications; United States

| Owner | Application # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | 10/940121 | SYSTEM AND METHOD FOR FETCHING INFORMATION IN RESPONSE TO HAZARD INDICATION INFORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 11/022813 | INTEGRATED CIRCUIT PACKAGING DEVICE AND METHOD FOR MATCHING IMPEDANCE |
| FREESCALE SEMICONDUCTOR, INC. | 11/096607 | METHOD AND APPARATUS FACILITATING MULTI MODE INTERFACES |
| FREESCALE SEMICONDUCTOR, INC. | 11/205419 | MANAGEMENT OF SECURITY FEATURES IN A COMMUNICATION NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 11/262171 | SYSTEM AND METHOD FOR DECOUPLED PRECOMPUTATION PREFETCHING |
| FREESCALE SEMICONDUCTOR, INC. | 11/271693 | RESOURCE EFFICIENT VIDEO PROCESSING VIA PREDICTION ERROR COMPUTATIONAL ADJUSTMENTS |
| FREESCALE SEMICONDUCTOR, INC. | 11/343781 | DETECTING REFLECTIONS IN A COMMUNICATION CHANNEL |
| FREESCALE SEMICONDUCTOR, INC. | 11/372666 | WARP COMPENSATED PACKAGE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 11/385463 | DATA PROCESSOR HAVING DYNAMIC CONTROL OF INSTRUCTION PREFETCH BUFFER DEPTH AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 11/441869 | METHOD OF INCREASING CODING EFFICIENCY AND REDUCING POWER CONSUMPTION BY ON-LINE SCENE CHANGE DETECTION WHILE ENCODING INTER-FRAME |
| FREESCALE SEMICONDUCTOR, INC. | 11/445981 | SYSTEM AND METHOD FOR POLAR MODULATION USING POWER AMPLIFIER BIAS CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 11/532417 | VIDEO INFORMATION PROCESSING SYSTEM WITH SELECTIVE CHROMA DEBLOCK FILTERING |
| FREESCALE SEMICONDUCTOR, INC. | 11/539522 | SCALING VIDEO PROCESSING COMPLEXITY BASED ON POWER SAVINGS FACTOR |
| FREESCALE SEMICONDUCTOR, INC. | 11/552817 | SYSTEM AND METHOD FOR MEMORY ARRAY ACCESS WITH FAST ADDRESS DECODER |
| FREESCALE SEMICONDUCTOR, INC. | 11/574495 | METHOD FOR ESTIMATING POWER CONSUMPTION |
| FREESCALE SEMICONDUCTOR, INC. | 11/574867 | APPARATUS AND CONTROL INTERFACE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 11/608616 | ADAPTIVE DISABLING OF DEBLOCK FILTERING BASED ON A CONTENT CHARACTERISTIC OF VIDEO INFORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 11/608690 | SYSTEM AND METHOD OF DETERMINING DEBLOCKING CONTROL FLAG OF SCALABLE VIDEO SYSTEM FOR INDICATING PRESENTATION OF DEBLOCKING PARAMETERS FOR MULTIPLE LAYERS |
| FREESCALE SEMICONDUCTOR, INC. | 11/613326 | SEMICONDUCTOR DEVICE INCLUDING AN ACTIVE REGION AND TWO LAYERS HAVING DIFFERENT STRESS CHARACTERISTICS |
| FREESCALE SEMICONDUCTOR, INC. | 11/619294 | PROGRESSIVE MEMORY INITIALIZATION WITH WAITPOINTS |
| FREESCALE SEMICONDUCTOR, INC. | 11/619301 | SELECTIVE GUARDED MEMORY ACCESS ON A PER-INSTRUCTION BASIS |
| FREESCALE SEMICONDUCTOR, INC. | 11/650697 | INTEGRATED ASSIST FEATURES FOR EPITAXIAL GROWTH |
| FREESCALE SEMICONDUCTOR, INC. | 11/685297 | ELECTRONIC DEVICE INCLUDING CHANNEL REGIONS LYING AT DIFFERENT ELEVATIONS AND PROCESSES OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 11/719924 | INTEGRATED CIRCUIT AND A METHOD FOR TESTING A MULTI-TAP INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 11/733978 | TECHNIQUES FOR TRACING PROCESSES IN A MULTI-THREADED |

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| FREESCALE SEMICONDUCTOR, INC. | 11/746998 | THREAD DE-EMPHASIS INSTRUCTION FOR MULTITHREADED PROCESSOR |
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| FREESCALE SEMICONDUCTOR, INC. | 11/748350 | METHOD AND APPARATUS FOR CACHE TRANSACTIONS IN A DATA |
| FREESCALE SEMICONDUCTOR, INC. | 11//40330 | PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 11/759935 | HEAT SPREADER FOR CENTER GATE MOLDING |
| FREESCALE SEMICONDUCTOR, INC. | 11/772655 | ASYMMETRIC CRYPTOGRAPHIC DEVICE WITH LOCAL PRIVATE KEY GENERATION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 11/780900 | ELECTRONIC DEVICE INCLUDING A CAPACITOR AND A PROCESS OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 11/816038 | LEAD-FRAME CIRCUIT PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 11/846196 | TEMPORAL SCALABILITY FOR LOW DELAY SCALABLE VIDEO CODING |
| FREESCALE SEMICONDUCTOR, INC. | 11/854630 | SIMD DOT PRODUCT OPERATIONS WITH OVERLAPPED OPERANDS |
| FREESCALE SEMICONDUCTOR, INC. | 11/871659 | SINGLE-INSTRUCTION MULTIPLE-DATA VECTOR PERMUTATATION INSTRUCTION AND METHOD FOR PERFORMING TABLE LOOKUPS FOR INRANGE INDEX VALUES AND DETERMINING CONSTANT VALUES FOR OUTOF-RANGE INDEX VALUES |
| FREESCALE SEMICONDUCTOR, INC. | 11/911929 | DEVICE AND METHOD FOR CONTROLLING A BACKLIT DISPLAY |
| FREESCALE SEMICONDUCTOR, INC. | 11/912126 | IMPROVED CLEANING OF CIRCUIT SUBSTRATES |
| FREESCALE SEMICONDUCTOR, INC. | 11/916711 | HYBRID METHOD AND DEVICE FOR TRANSMITTING PACKETS |
| FREESCALE SEMICONDUCTOR, INC. | 11/917108 | DEVICE AND METHOD FOR MEDIA ACCESS CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 11/962331 | SYSTEM AND METHOD FOR PROCESSING POTENTIALLY SELF- INCONSISTENT MEMORY TRANSACTIONS |
| FREESCALE SEMICONDUCTOR, INC. | 11/971795 | MULTIPLE FUNCTION SWITCHING REGULATOR FOR USE IN MOBILE ELECTRONIC DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 11/994251 | VECTOR CRC COMPUTATION ON DSP |
| FREESCALE SEMICONDUCTOR, INC. | 11/994270 | DEVICE AND METHOD FOR ARBITRATING BETWEEN DIRECT MEMORY ACCESS TASK REQUESTS |
| FREESCALE SEMICONDUCTOR, INC. | 12/013812 | MICROELECTRONIC REFRIGERATION SYSTEM AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 12/016739 | METHOD OF MAKING A PHASE CHANGE MEMORY CELL HAVING A SILICIDE HEATER IN CONJUNCTION WITH A FINFET |
| FREESCALE SEMICONDUCTOR, INC. | 12/017988 | SHARED RESOURCE BASED THREAD SCHEDULING WITH AFFINITY AND/OR SELECTABLE CRITERIA |
| FREESCALE SEMICONDUCTOR, INC. | 12/032286 | PERIPHERAL MODULE REGISTER ACCESS METHODS AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 12/035967 | DATA PROCESSOR DEVICE SUPPORTING SELECTABLE EXCEPTIONS AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 12/039913 | PACKAGING AN INTEGRATED CIRCUIT DIE USING COMPRESSION MOLDING |
| FREESCALE SEMICONDUCTOR, INC. | 12/053761 | SELECTIVE INTERCONNECT TRANSACTION CONTROL FOR CACHE COHERENCY MAINTENANCE |
| FREESCALE SEMICONDUCTOR, INC. | 12/063422 | HANDOVER BASED ON A QUALITY OF SERVICE METRIC OBTAINED FROM A MAC LAYER OF A RECEIVED SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 12/067587 | SYSTEM AND METHOD FOR STORING STATE INFORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 12/091034 | ELECTRONIC DEVICE AND METHOD FOR CONTROLLING CURRENT |
| FREESCALE SEMICONDUCTOR, INC. | 12/093939 | DEVICE AND METHOD FOR COMPENSATING FOR VOLTAGE DROPS |
| FREESCALE SEMICONDUCTOR, INC. | 12/112502 | CACHE COHERENCY PROTOCOL IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 12/112796 | SNOOP REQUEST MANAGEMENT IN A DATA PROCESSING SYSTEM |
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| FREESCALE SEMICONDUCTOR, INC. | 12/122178 | MODULATION OF A TANTALUM-BASED ELECTRODE WORKFUNCTION |
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| FREESCALE SEMICONDUCTOR, INC. | 12/131691 | MULTI-STRAND SUBSTRATE FOR BALL-GRID ARRAY ASSEMBLIES AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 12/135638 | SYSTEM AND METHOD FOR PARALLEL VIDEO PROCESSING IN MULTICORE DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 12/142028 | SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR PREVENTING STARVATIONS OF TASKS IN A MULTIPLE PROCESSING ENTITY SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 12/160470 | CONTROLLING THE ACCESS OF MASTER ELEMENTS TO SLAVE ELEMENTS OVER A COMMUNICATION BUS |
| FREESCALE SEMICONDUCTOR, INC. | 12/162174 | DEVICE AND METHOD FOR ADDING AND SUBTRACTING TWO VARIABLES AND A CONSTANT |
| FREESCALE SEMICONDUCTOR, INC. | 12/162177 | BARRIER SLURRY COMPOSITION AND BARRIER CMP METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 12/164444 | METHOD FOR IMPLEMENTING A BIT-REVERSED INCREMENT IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 12/195220 | DEBUG INSTRUCTION FOR USE IN A MULTI-THREADED DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 12/203480 | HANDHELD DEVICE FOR TRANSMITTING A VISUAL FORMAT MESSAGE |
| FREESCALE SEMICONDUCTOR, INC. | 12/251746 | MULTIPLE DEVICE TYPES INCLUDING AN INVERTED-T CHANNEL TRANSISTOR AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/259368 | DATA PROCESSOR FOR PROCESSING A DECORATED STORAGE NOTIFY |
| FREESCALE SEMICONDUCTOR, INC. | 12/259369 | PERMISSIONS CHECKING FOR DATA PROCESSING INSTRUCTIONS |
| FREESCALE SEMICONDUCTOR, INC. | 12/259765 | SINGLE AMPLIFIER FILTER FOR CONSTANT GROUP DELAY IN RADIO FREQUENCY TRANSMITTERS |
| FREESCALE SEMICONDUCTOR, INC. | 12/267728 | TECHNIQUE FOR PACKAGING MULTIPLE INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 12/271841 | CONTINUOUS SELFTEST FOR INERTIAL SENSORS AT 0 HZ |
| FREESCALE SEMICONDUCTOR, INC. | 12/279952 | A METHOD AND DEVICE FOR EXCHANGING DATA USING A VIRTUAL FIFO DATA STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 12/280478 | SOFTWARE PIPELINING |
| FREESCALE SEMICONDUCTOR, INC. | 12/280482 | INTEGRATED SYSTEM FOR SEMICONDUCTOR SUBSTRATE PROCESSING USING LIQUID PHASE METAL DEPOSITION |
| FREESCALE SEMICONDUCTOR, INC. | 12/282491 | METHOD AND APPARATUS FOR ENHANCED DATA RATE ADAPTATION AND LOWER POWER CONTROL IN A WLAN SEMICONDUCTOR CHIP |
| FREESCALE SEMICONDUCTOR, INC. | 12/286359 | DATA INTERLEAVER |
| FREESCALE SEMICONDUCTOR, INC. | 12/288955 | METHODS AND APPARATUS FOR REORDERING DATA |
| FREESCALE SEMICONDUCTOR, INC. | 12/300438 | LIN NETWORK, INTEGRATED CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/302221 | SIN-COS SENSOR ARRANGEMENT, INTEGRATED CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/304193 | METHOD AND DEVICE FOR PROVIDING A SECURITY BREACH INDICATIVE AUDIO ALERT |
| FREESCALE SEMICONDUCTOR, INC. | 12/304849 | ELECTROSTATIC DISCHARGE PROTECTION APPARATUS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/304852 | VOLTAGE REGULATION APPARATUS AND METHOD OF REGULATING A VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | 12/305107 | IMPROVEMENTS IN OR RELATING TO BUFFER MANAGEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 12/305160 | METHOD FOR GAMMA CORRECTION AND A DEVICE HAVING GAMMA |

12/328135

FREESCALE SEMICONDUCTOR, INC.

CORRECTION CAPABILITIES

MEMORY INTERFACE DEVICE AND METHODS THEREOF

| FREESCALE SEMICONDUCTOR, INC. | 12/363916 | METHOD OF FABRICATING HIGH ASPECT RATIO TRANSDUCER USING METAL COMPRESSION BONDING |
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| FREESCALE SEMICONDUCTOR, INC. | 12/364112 | VIDEO SCENE CHANGE DETECTION AND ENCODING COMPLEXITY REDUCTION IN A VIDEO ENCODER SYSTEM HAVING MULTIPLE PROCESSING DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 12/366985 | DEBUG CONTROL FOR SNOOP OPERATIONS IN A MULTIPROCESSOR SYSTEM AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 12/375848 | MEMORY MANAGEMENT UNIT AND METHOD OF ACCESSING AN ADDRESS |
| FREESCALE SEMICONDUCTOR, INC. | 12/376069 | METHOD FOR MONOTONICALLY COUNTING AND A DEVICE HAVING MONOTONIC COUNTING CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 12/377351 | METHOD FOR PERFORMING PLURALITY OF BIT OPERATIONS AND A DEVICE HAVING PLURALITY OF BIT OPERATIONS CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 12/377804 | PIPELINED DEVICE AND A METHOD FOR EXECUTING TRANSACTIONS IN A PIPELINED DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 12/398099 | ACCESS MANAGEMENT TECHNIQUE FOR STORAGE-EFFICIENT MAPPING BETWEEN IDENTIFIER DOMAINS |
| FREESCALE SEMICONDUCTOR, INC. | 12/405305 | VIDEO DECODER PLUS A DISCRETE COSINE TRANSFORM UNIT |
| FREESCALE SEMICONDUCTOR, INC. | 12/413101 | ASYNCHRONOUS DATA RECOVERY METHODS AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 12/418259 | TECHNIQUE FOR GENERATING HASH-TUPLE INDEPENDENT OF PRECEDENCE ORDER OF APPLIED RULES |
| FREESCALE SEMICONDUCTOR, INC. | 12/419708 | ELECTRONIC DEVICE AND METHOD OF PACKAGING AN ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 12/422684 | VIDEO DECODING WITH ERROR DETECTION AND CONCEALMENT |
| FREESCALE SEMICONDUCTOR, INC. | 12/427646 | TRACING SUPPORT FOR INTERCONNECT FABRIC |
| FREESCALE SEMICONDUCTOR, INC. | 12/433330 | INTEGRATED CIRCUIT HAVING MEMORY REPAIR INFORMATION STORAGE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/441311 | SEMICONDUCTOR DEVICE AND METHOD OF FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 12/444061 | ERROR CORRECTION VIA LOOKUP IN COMPRESSED ERROR LOCATION DATA |
| FREESCALE SEMICONDUCTOR, INC. | 12/445021 | IMAGE PROCESSING APPARATUS FOR SUPERIMPOSING WINDOWS DISPLAYING VIDEO DATA HAVING DIFFERENT FRAME RATES |
| FREESCALE SEMICONDUCTOR, INC. | 12/446409 | DEVICE HAVING REDUNDANT CORE AND A METHOD FOR PROVIDING CORE REDUNDANCY |
| FREESCALE SEMICONDUCTOR, INC. | 12/459995 | RECEIVER WITH AUTOMATIC GAIN CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 12/485190 | EVENT TRIGGERED MEMORY MAPPED ACCESS |
| FREESCALE SEMICONDUCTOR, INC. | 12/485196 | TRACE CORRELATION FOR PROFILING SUBROUTINES |
| FREESCALE SEMICONDUCTOR, INC. | 12/485579 | FLOW CONTROL MECHANISMS FOR AVOIDANCE OF RETRIES AND/OR DEADLOCKS IN AN INTERCONNECT |
| FREESCALE SEMICONDUCTOR, INC. | 12/492531 | PROBING STRUCTURE FOR EVALUATION OF SLOW SLEW-RATE SQUARE WAVE SIGNALS IN LOW POWER CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 12/502812 | BIPOLAR TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/515242 | MEMORY SYSTEM WITH ECC-UNIT AND FURTHER PROCESSING ARRANGEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 12/515634 | SYSTEM, APPARATUS AND METHOD FOR TRANSLATING DATA |
| FREESCALE SEMICONDUCTOR, INC. | 12/518845 | TRANSMISSION AND RECEPTION CHANNEL SELECTION FOR COMMUNICATING BETWEEN A TRANSMITTER UNIT AND A RECEIVER UNIT |
| FREESCALE SEMICONDUCTOR, INC. | 12/523933 | VERY LOW INTERMEDIATE FREQUENCY (VLIF) RECEIVER |

| FREESCALE SEMICONDUCTOR, INC. | 12/523934 | CALIBRATION SIGNAL GENERATOR |
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| FREESCALE SEMICONDUCTOR, INC. | 12/527372 | REQUEST CONTROLLER, PROCESSING UNIT, ARRANGEMENT, METHOD FOR CONTROLLING REQUESTS AND COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | 12/527733 | DATA COMMUNICATION UNIT, DATA COMMUNICATION NETWORK AND METHOD OF DECODING |
| FREESCALE SEMICONDUCTOR, INC. | 12/551495 | TRANSMITTER SIGNAL INJECTION COMPENSATION |
| FREESCALE SEMICONDUCTOR, INC. | 12/558201 | TIME DOMAIN ADAPTIVE FILTER BANK FOR NETWORK ECHO REDUCTION OR CANCELLATION |
| FREESCALE SEMICONDUCTOR, INC. | 12/563902 | METHOD AND APPARATUS FOR DETERMINING ACCESS PERMISSIONS IN A PARTITIONED DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 12/579873 | FLEXIBLE MEMORY CONTROLLER FOR AUTONOMOUS MAPPING OF MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 12/592290 | METHODS AND APPARATUS FOR PERFORMING CAPACITIVE TOUCH SENSING AND PROXIMITY DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | 12/594229 | IMPROVEMENTS IN OR RELATING TO DIAGNOSTICS OF A CAPACITIVE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/595362 | DATA PROCESSING CONTROL UNIT FOR CONTROLLING MULTIPLE DATA PROCESSING OPERATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 12/600007 | WIRELESS COMMUNICATION UNIT, BASEBAND MODULE, RADIO FREQUENCY MODULE, WIRELESS TERMINAL AND COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | 12/600055 | DATA PROCESSING SYSTEM, METHOD FOR PROCESSING DATA AND COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | 12/600687 | INTEGRATED CIRCUIT, WIRELESS COMMUNICATION UNIT AND METHOD FOR DETERMINING QUADRATURE IMBALANCE |
| FREESCALE SEMICONDUCTOR, INC. | 12/607562 | METHOD AND APPARATUS FOR ACTIVATING SYSTEM COMPONENTS |
| FREESCALE SEMICONDUCTOR, INC. | 12/608525 | INTERCONNECT CONTROLLER FOR A DATA PROCESSING DEVICE WITH TRANSACTION TAG LOCKING AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/617902 | METHOD AND APPARATUS FOR VIDEO DECODING WITH REDUCED COMPLEXITY INVERSE TRANSFORM |
| FREESCALE SEMICONDUCTOR, INC. | 12/618311 | MULTI-CORE SYSTEM ON CHIP |
| FREESCALE SEMICONDUCTOR, INC. | 12/620582 | FOUR STROKE SINGLE CYLINDER COMBUSTION ENGINE STARTING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 12/639394 | ELECTRONIC DEVICE WITH A GATE ELECTRODE HAVING AT LEAST TWO PORTIONS |
| FREESCALE SEMICONDUCTOR, INC. | 12/660951 | DYNAMIC VOLTAGE SCALING INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | 12/665070 | COUPLING LAYER COMPOSITION FOR A SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE, METHOD OF FORMING THE COUPLING LAYER, AND APPARATUS FOR THE MANUFACTURE OF A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 12/672312 | DATA PACKET FREQUENCY |
| FREESCALE SEMICONDUCTOR, INC. | 12/672319 | VOLTAGE SUPPLY CIRCUITRY AND INTEGRATED CIRCUIT THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/675252 | BAND-GAP VOLTAGE REFERENCE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 12/676699 | TIMER UNIT, SYSTEM, COMPUTER PROGRAM PRODUCT AND METHOD FOR TESTING A LOGIC CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 12/682469 | PROLONGING INTERNAL POWER SUPPLY LIFE IN A MOBILE COMMUNICATION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 12/683961 | DIE BONDING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 12/690771 | ESD PROTECTION DEVICE AND METHOD |

12/701687 FATAL FAILURE DIAGNOSTICS CIRCUIT AND METHODOLOGY

FREESCALE SEMICONDUCTOR, INC.

| FREESCALE SEMICONDUCTOR, INC. | 12/701780 | GENERATION, INJECTION AND USE OF PILOT TONES FOR GYRO SYSTEM CHARACTERIZATION |
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| FREESCALE SEMICONDUCTOR, INC. | 12/703239 | PULSE WIDTH MODULATION WITH EFFECTIVE HIGH DUTY RESOLUTION |
| FREESCALE SEMICONDUCTOR, INC. | 12/707961 | DEVICE INCLUDING AN ANTENNA AND METHOD OF USING AN ANTENNA |
| FREESCALE SEMICONDUCTOR, INC. | 12/711398 | FLIP-FLOP HAVING SHARED FEEDBACK AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 12/722225 | METHOD OF FABRICATING A SEMICONDUCTOR DEVICE THAT LIMITS DAMAGE TO ELEMENTS OF THE SEMICONDUCTOR DEVICE THAT ARE EXPOSED DURING PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 12/727258 | METHOD OF MAKING CHIP-ON-LEAD PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 12/731510 | CAPACITIVE TOUCH PAD WITH ADJACENT TOUCH PAD ELECTRIC FIELD SUPPRESSION |
| FREESCALE SEMICONDUCTOR, INC. | 12/742665 | AMPLIFIER CIRCUIT AUDIO CIRCUIT AND ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 12/745966 | SEMICONDUCTOR DEVICE AND APPARATUS INCLUDING SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 12/746793 | RF POWER TRANSISTOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 12/747717 | AMPLIFIER CIRCUIT, ELECTRONIC DEVICE, METHOD FOR CONFIGURING AN AMPLIFIER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 12/748600 | ASYNCHRONOUSLY SCHEDULING MEMORY ACCESS REQUESTS |
| FREESCALE SEMICONDUCTOR, INC. | 12/748617 | SCHEDULING MEMORY ACCESS REQUESTS USING PREDICTED MEMORY TIMING AND STATE INFORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 12/762439 | INTEGRATED CIRCUIT DEVICE WITH REDUCED LEAKAGE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/764689 | MONITOR CIRCUIT FOR DETERMINING THE LIFETIME OF A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 12/768275 | TECHNIQUES FOR UPDATING FILTER COEFFICIENTS OF AN ADAPTIVE FILTER |
| FREESCALE SEMICONDUCTOR, INC. | 12/768366 | TECHNIQUES FOR IMPLEMENTING ADAPTATION CONTROL OF AN ECHO CANCELLER TO FACILITATE DETECTION OF IN-BAND SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 12/784496 | RESISTOR TESTING CIRCUIT AND BATTERY CHARGER INCLUDING RESISTOR TESTING CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 12/788386 | VIDEO PROCESSING SYSTEM, COMPUTER PROGRAM PRODUCT AND METHOD FOR MANAGING A TRANSFER OF INFORMATION BETWEEN A MEMORY UNIT AND A DECODER |
| FREESCALE SEMICONDUCTOR, INC. | 12/788769 | CLOCK SIMULATION DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 12/791996 | HIGH VOLTAGE DEEP TRENCH CAPACITOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/794591 | METHODS AND APPARATUS FOR AN ISFET |
| FREESCALE SEMICONDUCTOR, INC. | 12/811449 | SEMICONDUCTOR PROCESSING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 12/811454 | PROCESSOR BASED SYSTEM HAVING ECC BASED CHECK AND ACCESS VALIDATION INFORMATION MEANS |
| FREESCALE SEMICONDUCTOR, INC. | 12/811804 | MOS TRANSISTOR DRAIN-TO-GATE LEAKAGE PROTECTION CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/812032 | CONTENTION FREE PARALLEL ACCESS SYSTEM AND A METHOD FOR CONTENTION FREE PARALLEL ACCESS TO A GROUP OF MEMORY BANKS |
| FREESCALE SEMICONDUCTOR, INC. | 12/813903 | LEAD FRAME BASED, OVER-MOLDED SEMICONDUCTOR PACKAGE WITH INTEGRATED THROUGH HOLE TECHNOLOGY (THT) HEAT SPREADER PIN(S) AND ASSOCIATED METHOD OF MANUFACTURING |

| FREESCALE SEMICONDUCTOR, INC. | 12/817805 | METHODS OF MAKING LATERALLY DOUBLE DIFFUSED METAL OXIDE SEMICONDUCTOR TRANSISTORS HAVING A REDUCED SURFACE FIELD STRUCTURE |
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| FREESCALE SEMICONDUCTOR, INC. | 12/818235 | CIRCUIT HAVING GATE DRIVERS HAVING A LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | 12/818270 | SWITCHING REGULATOR WITH INPUT CURRENT LIMITING CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 12/838633 | USE OF MULTIPLE INTERNAL SENSORS FOR MEASUREMENT VALIDATION |
| FREESCALE SEMICONDUCTOR, INC. | 12/844922 | INTEGRATED CIRCUIT PACKAGE WITH VOLTAGE DISTRIBUTOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/846042 | DATA PROCESSING HAVING MULTIPLE LOW POWER MODES AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/852513 | SYNCHRONISER CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 12/853106 | MULTISTAGE VOLTAGE REGULATOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 12/855479 | MONOLITHIC MICROWAVE INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 12/856430 | DATA PROCESSING SYSTEM HAVING TEMPORAL REDUNDANCY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/858599 | DATA PROCESSING SYSTEM HAVING SELECTIVE REDUNDANCY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/860565 | PARTIALLY DEPLETED DIELECTRIC RESURF LDMOS |
| FREESCALE SEMICONDUCTOR, INC. | 12/865138 | MEMORY MANAGEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 12/866244 | METHOD AND APPARATUS FOR DECODING RECEIVED DATA SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 12/866247 | REDUCING POWER CONSUMPTION IN A PORTABLE ELECTRONIC DEVICE WITH A LUMINESCENT ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 12/867496 | PROCESSOR FOR USE AS A PATH SEARCHER OF A SPREAD SPECTRUM RECEIVER AND A METHOD OF OPERATION OF THE PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/870491 | TOUCH SENSOR CONTROLLER FOR DRIVING A TOUCH SENSOR SHIELD |
| FREESCALE SEMICONDUCTOR, INC. | 12/872070 | PATTERNING A GATE STACK OF A NON-VOLATILE MEMORY (NVM) USING A DUMMY GATE STACK |
| FREESCALE SEMICONDUCTOR, INC. | 12/874656 | SYSTEM AND METHOD FOR COOPERATIVE PREFETCHING |
| FREESCALE SEMICONDUCTOR, INC. | 12/877193 | 3-D SEMICONDUCTOR DIE STRUCTURE WITH CONTAINING FEATURE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 12/880352 | DATA PROCESSING SYSTEM HAVING END-TO-END ERROR CORRECTION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/886859 | LATERAL CAPACITOR AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 12/886861 | NON-VOLATILE MEMORY (NVM) WITH IMMINENT ERROR PREDICTION |
| FREESCALE SEMICONDUCTOR, INC. | 12/892622 | SEMICONDUCTOR STRUCTURE HAVING A THROUGH SUBSTRATE VIA (TSV) AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 12/899195 | SWITCHED MODE VOLTAGE REGULATOR AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 12/907676 | ROM MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 12/908586 | BIPOLAR TRANSISTOR WITH IMPROVED STABILITY |
| FREESCALE SEMICONDUCTOR, INC. | 12/909632 | IMPROVED BIPOLAR TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/915198 | DATA PROCESSING SYSTEM HAVING SELECTIVE INVALIDATION OF SNOOP REQUESTS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/917470 | DEBUGGER RECOVERY ON EXIT FROM LOW POWER MODE |
| FREESCALE SEMICONDUCTOR, INC. | 12/918185 | DTMF TONE MONITORING APPARATUS AND METHOD OF IDENTIFYING A DTMF TONE |

| FREESCALE SEMICONDUCTOR, INC. | 12/919541 | A METHOD FOR PROTECTING A CRYPTOGRAPHIC MODULE AND A DEVICE HAVING CRYPTOGRAPHIC MODULE PROTECTION CAPABILITIES |
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| FREESCALE SEMICONDUCTOR, INC. | 12/920600 | APPARATUS AND A METHOD FOR DETECTING FAULTS IN THE DELIVERY OF ELECTRICAL POWER TO ELECTRICAL LOADS |
| FREESCALE SEMICONDUCTOR, INC. | 12/933229 | MICROPROCESSOR HAVING A LOW-POWER MODE AND A NON-LOW POWER MODE, DATA PROCESSING SYSTEM AND COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | 12/934275 | A SYSTEM AND A METHOD FOR SELECTING A CACHE WAY |
| FREESCALE SEMICONDUCTOR, INC. | 12/936214 | PLL SYSTEM AND METHOD FOR CONTROLLING A GAIN OF A VCO CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 12/936215 | WIRELESS COMMUNICATION UNIT AND SEMICONDUCTOR DEVICE HAVING A POWER AMPLIFIER THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/936965 | MULTIPLEXING AND DEMULTIPLEXING DATA |
| FREESCALE SEMICONDUCTOR, INC. | 12/937891 | SYNCHRONIZATION OF STATEFUL ELEMENTS IN A PROCESSING RESOURCE USING A SCAN CHAIN |
| FREESCALE SEMICONDUCTOR, INC. | 12/938493 | ELECTRONIC CIRCUIT AND METHOD FOR OPERATING A CIRCUIT IN A STANDBY MODE AND IN AN OPERATIONAL MODE |
| FREESCALE SEMICONDUCTOR, INC. | 12/942285 | METHOD FOR PROGRAMMING A MULTI-STATE NONVOLATILE MEMORY (NVM) |
| FREESCALE SEMICONDUCTOR, INC. | 12/945825 | INTEGRATED ANTENNA PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 12/945828 | RADAR MODULE |
| FREESCALE SEMICONDUCTOR, INC. | 12/948447 | DIFFERENTIAL EQUALIZERS WITH SOURCE DEGENERATION AND FEEDBACK CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 12/954907 | SYSTEM AND METHOD FOR SCAN TESTING INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 12/982856 | CACHE RESULT REGISTER FOR QUICK CACHE INFORMATION LOOKUP |
| FREESCALE SEMICONDUCTOR, INC. | 12/985906 | METHOD FOR FORMING AN OVER PAD METALIZATION (OPM) ON A BOND PAD |
| FREESCALE SEMICONDUCTOR, INC. | 12/988828 | METHOD AND APPARATUS FOR CONTROL OF AN AC ELECTRIC MOTOR WITH FIELD WEAKENING |
| FREESCALE SEMICONDUCTOR, INC. | 12/988831 | METHOD FOR SAMPLING DATA AND APPARATUS THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 12/988832 | METHOD AND APPARATUS FOR DETECTING A SET UP SIGNAL USED FOR DATA COMMUNICATION OVER A COMMUNICATION NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 12/990865 | METHOD AND APPARATUS FOR INTERLEAVING A DATA STREAM USING QUADRATURE PERMUTATION POLYNOMIAL FUNCTIONS (QPP) |
| FREESCALE SEMICONDUCTOR, INC. | 12/990868 | DISPLAY CONTROLLER, IMAGE PROCESSING SYSTEM, DISPLAY SYSTEM, APPARATUS AND COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | 12/990873 | SEMICONDUCTOR DEVICE AND METHOD FOR VALIDATING A STATE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 12/991824 | ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT, EQUIPMENT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 12/991834 | METHOD AND APPARATUS FOR ENABLING COMMUNICATION BETWEEN A FIRST DEVICE AND AT LEAST ONE FURTHER DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 12/994021 | COMPUTER PROGRAM PRODUCT, A METHOD FOR DEBUGGING A SYSTEM, AND A SYSTEM HAVING DEBUGGING CAPABILITIES FOR SETTING, BY A DEBUGGER OR A PROCESSING ENTITY, A VALUE OF A SCHEDULER CONTROL VARIABLE AND DETERMINING, BY THE SCHEDULER, AN EXECUTION FLOW OF THE SC |

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| FREESCALE SEMICONDUCTOR, INC. | 12/994027 | SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR SCHEDULING A PROCESSING ENTITY TASK |
| FREESCALE SEMICONDUCTOR, INC. | 12/994033 | SYSTEM AND COMPUTER PROGRAM PRODUCT FOR SCHEDULING PROCESSOR ENTITY TASKS IN A MULTIPLE PROCESSING ENTITY SYSTEM WITH A MULTIPLE PURPOSE ENTITY CAPABLE OF PERFORMING THE SCHEDULING |
| FREESCALE SEMICONDUCTOR, INC. | 12/995297 | MEMORY SYSTEM WITH REDUNDANT DATA STORAGE AND ERROR CORRECTION |
| FREESCALE SEMICONDUCTOR, INC. | 12/995317 | SYSTEM FOR DISTRIBUTING AVAILABLE MEMORY RESOURCE |
| FREESCALE SEMICONDUCTOR, INC. | 12/997087 | PATCHING OF A READ-ONLY MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 12/999084 | PROCESSING POSITION-RELATED INPUT DATA FROM A ROTATIONAL MACHINE WHOSE ANGULAR SPEED IS VARIABLE |
| FREESCALE SEMICONDUCTOR, INC. | 12/999143 | METHOD OF FORMING A POWER SEMICONDUCTOR DEVICE AND POWER SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/003311 | METHOD AND APPARATUS FOR DETECTING ONE OR MORE PREDETERMINED TONES TRANSMITTED OVER A COMMUNICATION NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 13/003948 | FAULT DETECTION APPARATUS FOR ALPHANUMERIC DISPLAY SYSTEM AND METHOD OF DETECTING A FAULT |
| FREESCALE SEMICONDUCTOR, INC. | 13/004396 | CMOS DEVICE STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | 13/004985 | MULTI-STATE NON-VOLATILE MEMORY CELL INTEGRATION AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/004988 | SEMICONDUCTOR DEVICE HAVING CONDUCTORS WITH DIFFERENT DIMENSIONS AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 13/012643 | MEMS SENSOR WITH FOLDED TORSION SPRINGS |
| FREESCALE SEMICONDUCTOR, INC. | 13/013337 | PROGRAM TRACE MESSAGE GENERATION FOR PAGE CROSSING EVENTS FOR DEBUG |
| FREESCALE SEMICONDUCTOR, INC. | 13/013660 | METHOD AND APPARATUS FOR PROCESSING TEMPORAL AND SPATIAL OVERLAPPING UPDATES FOR AN ELECTRONIC DISPLAY |
| FREESCALE SEMICONDUCTOR, INC. | 13/016327 | SELECTIVE CACHE ACCESS CONTROL APPARATUS AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/016353 | MEMORY HAVING A LATCHING SENSE AMPLIFIER RESISTANT TO NEGATIVES BIAS TEMPERATURE INSTABILITY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/020565 | ELECTRONIC CIRCUIT HAVING SHARED LEAKAGE CURRENT REDUCTION CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 13/023942 | BIPOLAR TRANSISTOR AND METHOD WITH RECESSED BASE ELECTRODE |
| FREESCALE SEMICONDUCTOR, INC. | 13/025201 | PHASE-SHIFTED PULSE WIDTH MODULATION SIGNAL GENERATION DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/025350 | NEAR ZERO CHANNEL LENGTH FIELD DRIFT LDMOS |
| FREESCALE SEMICONDUCTOR, INC. | 13/028930 | MEMS DEVICE HAVING VARIABLE GAP WIDTH AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 13/031545 | ACCELEROMETER AND AUTOMATIC CALIBRATION OF SAME |
| FREESCALE SEMICONDUCTOR, INC. | 13/032107 | MAGNETOMETER TEST ARRANGEMENT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 13/033317 | MEMORY PROTECTION IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 13/033327 | REMOTE PERMISSIONS PROVISIONING FOR STORAGE IN A CACHE AND DEVICE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/033854 | MEMS DEVICE WITH ENHANCED RESISTANCE TO STICTION |
| FREESCALE SEMICONDUCTOR, INC. | 13/034084 | SEMICONDUCTOR DEVICES HAVING REDUCED GATE-DRAIN CAPACITANCE |
| FREESCALE SEMICONDUCTOR, INC. | 13/036251 | MICROPROCESSOR SYSTEMS AND METHODS FOR LATENCY TOLERANCE |

EXECUTION

| FREESCALE SEMICONDUCTOR, INC. | 13/036321 | SYSTEMS AND METHODS FOR RECONFIGURING CACHE MEMORY |
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| FREESCALE SEMICONDUCTOR, INC. | 13/036461 | VIAS BETWEEN CONDUCTIVE LAYERS TO IMPROVE RELIABILITY |
| FREESCALE SEMICONDUCTOR, INC. | 13/036516 | NON-VOLATILE MEMORY (NVM) CELL FOR ENDURANCE AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 13/036604 | MULTIPLE PATTERNING CONSISTENCY PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 13/037013 | SYSTEMS AND METHODS FOR CONFIGURING LOAD/STORE EXECUTION UNITS |
| FREESCALE SEMICONDUCTOR, INC. | 13/038054 | READ STACKING FOR DATA PROCESSOR INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | 13/040797 | METHOD TO FORM A VIA |
| FREESCALE SEMICONDUCTOR, INC. | 13/042948 | SEMICONDUCTOR DEVICES WITH LOW LEAKAGE SCHOTTKY CONTACTS |
| FREESCALE SEMICONDUCTOR, INC. | 13/043075 | SYSTEMS AND METHODS FOR DETECTING SURFACE CHARGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/045307 | HIERARCHICAL ERROR CORRECTION FOR LARGE MEMORIES |
| FREESCALE SEMICONDUCTOR, INC. | 13/046815 | METHOD OF RE-ORDERING RECEIVED DATA BLOCKS IN HYBRID AUTOMATIC REPEAT REQUEST TELECOMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 13/047801 | STEPPER MOTOR CONTROLLER AND METHOD FOR CONTROLLING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 13/051611 | VOLTAGE-CONTROLLED OSCILLATORS AND RELATED SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 13/053962 | SELECTIVE CHECKBIT MODIFICATION FOR ERROR CORRECTION |
| FREESCALE SEMICONDUCTOR, INC. | 13/054124 | SYSTEM FOR MONITORING AND CONTROLLING THE POWER OF A RADIO FREQUENCY (RF) SIGNAL IN A SHORT-RANGE RF TRANSMITTER |
| FREESCALE SEMICONDUCTOR, INC. | 13/054344 | MICRO CONTROLLER UNIT INCLUDING AN ERROR INDICATOR MODULE |
| FREESCALE SEMICONDUCTOR, INC. | 13/054358 | INTEGRATED TESTING CIRCUITRY FOR HIGH-FREQUENCY RECEIVER INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 13/055968 | COMMUNICATIONS MODULE APPARATUS, INTEGRATED CIRCUIT AND METHOD OF COMMUNICATING DATA |
| FREESCALE SEMICONDUCTOR, INC. | 13/056322 | DIE TEMPERATURE ESTIMATOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/057384 | SECURITY KEY GENERATOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/058350 | VOLTAGE REGULATOR WITH LOW AND HIGH POWER MODES |
| FREESCALE SEMICONDUCTOR, INC. | 13/059084 | SYSTEM AND METHOD FOR COMMUNICATING ON AN ELECTRICAL BUS |
| FREESCALE SEMICONDUCTOR, INC. | 13/059085 | SEMICONDUCTOR DEVICE, WIRELESS COMMUNICATION DEVICE AND METHOD FOR GENERATING A SYNTHESIZED FREQUENCY SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 13/061626 | METHOD AND APPARATUS FOR TRANSMITTING DATA |
| FREESCALE SEMICONDUCTOR, INC. | 13/061967 | METHOD AND APPARATUS FOR TRANSMITTING DATA |
| FREESCALE SEMICONDUCTOR, INC. | 13/062958 | WIRELESS COMMUNICATION UNIT, INTEGRATED CIRCUIT AND METHOD OF POWER CONTROL OF A POWER AMPLIFIER THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/063214 | METHOD FOR ADJUSTING TIME SLOTS IN A COMMUNICATION NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 13/063679 | WAKE-UP CONTROL SYSTEM AND METHOD FOR CONTROLLING RECEIVER WAKE-UP |
| FREESCALE SEMICONDUCTOR, INC. | 13/070049 | LOW-LEAKAGE, HIGH-CAPACITANCE CAPACITOR STRUCTURES AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 13/075768 | CIRCUIT FOR PREVENTING A DUMMY READ IN A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 13/077491 | NON-VOLATILE MEMORY AND LOGIC CIRCUIT PROCESS INTEGRATION |
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| FREESCALE SEMICONDUCTOR, INC. | 13/077963 | METHOD AND SYSTEM TO COMPENSATE FOR TEMPERATURE AND PRESSURE IN PIEZO RESISTIVE DEVICES |
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| FREESCALE SEMICONDUCTOR, INC. | 13/080944 | MEMORY CONTROLLER AND METHOD FOR ACCESSING A PLURALITY OF NON-VOLATILE MEMORY ARRAYS |
| FREESCALE SEMICONDUCTOR, INC. | 13/085217 | RESISTIVE RANDOM ACCESS MEMORY (RAM) CELL AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 13/085533 | METHOD OF MAKING A SEMICONDUCTOR STRUCTURE USEFUL IN MAKING A SPLIT GATE NON-VOLATILE MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | 13/088100 | METHOD FOR ETCHED CAVITY DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 13/088106 | ETCHING TRENCHES IN A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 13/088579 | MEMS DEVICE WITH CENTRAL ANCHOR FOR STRESS ISOLATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/090056 | DYNAMIC LOCKSTEP CACHE MEMORY REPLACEMENT LOGIC |
| FREESCALE SEMICONDUCTOR, INC. | 13/090057 | CACHE MEMORY WITH DYNAMIC LOCKSTEP SUPPORT |
| FREESCALE SEMICONDUCTOR, INC. | 13/092037 | ISOLATED CAPACITORS WITHIN SHALLOW TRENCH ISOLATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/093154 | DYNAMIC PROGRAMMING FOR FLASH MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 13/094110 | APPARATUS AND METHOD FOR CHECKPOINT REPAIR IN A PROCESSING DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/095544 | MIXER CIRCUITS FOR SECOND ORDER INTERCEPT POINT CALIBRATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/096102 | SEMICONDUCTOR DEVICE WITH PROTECTIVE MATERIAL AND METHOD FOR ENCAPSULATING |
| FREESCALE SEMICONDUCTOR, INC. | 13/096282 | MICROPROCESSOR SYSTEMS AND METHODS FOR REGISTER FILE CHECKPOINTING |
| FREESCALE SEMICONDUCTOR, INC. | 13/096543 | SEMICONDUCTOR DEVICE STRUCTURE AS A CAPACITOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/097411 | VOLTAGE REGULATOR WITH DIFFERENT INVERTING GAIN STAGES |
| FREESCALE SEMICONDUCTOR, INC. | 13/097721 | SELECTIVE ERROR DETECTION AND ERROR CORRECTION FOR A MEMORY INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | 13/101793 | MEMS DEVICE WITH IMPACTING STRUCTURE FOR ENHANCED RESISTANCE TO STICTION |
| FREESCALE SEMICONDUCTOR, INC. | 13/103609 | SELECTIVE ROUTING OF LOCAL MEMORY ACCESSES AND DEVICE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/104449 | PHASE LOCKED LOOP CIRCUIT HAVING A VOLTAGE CONTROLLED OSCILLATOR WITH IMPROVED BANDWIDTH |
| FREESCALE SEMICONDUCTOR, INC. | 13/104991 | OBJECT DETECTION DEVICE WITH VARIABLE SENSITIVITY ELECTRIC FIELD MEASUREMENT CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/106703 | SYSTEM AND METHOD FOR SCALABLE MOVEMENT AND REPLICATION OF DATA |
| FREESCALE SEMICONDUCTOR, INC. | 13/111580 | MEMORY WITH DESCRETE STORAGE ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | 13/112077 | METHOD OF FORMING A SEMICONDUCTOR DEVICE FEATURING A GATE STRESSOR AND SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/116325 | MICROPROCESSOR SYSTEMS AND METHODS FOR HANDLING INSTRUCTIONS WITH MULTIPLE DEPENDENCIES |
| FREESCALE SEMICONDUCTOR, INC. | 13/117191 | METHOD FOR FORMING AN ASYMMETRIC SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/120477 | DATA PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 13/120874 | BUS DRIVER FOR AVOIDING AN OVERVOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/121693 | TEMPERATURE COMPENSATION IN A PHASE-LOCKED LOOP |
| FREESCALE SEMICONDUCTOR, INC. | 13/124961 | INTEGRATED CIRCUIT, COMMUNICATION UNIT AND METHOD FOR PHASE |

COMPENSATION

| FREESCALE SEMICONDUCTOR, INC. | 13/125502 | METHOD FOR SINGULATING ELECTRONIC COMPONENTS FROM A SUBSTRATE |
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| FREESCALE SEMICONDUCTOR, INC. | 13/125856 | MULTIMODE VOLTAGE REGULATOR AND METHOD FOR PROVIDING A MULTIMODE VOLTAGE REGULATOR OUTPUT VOLTAGE AND AN OUTPUT CURRENT TO A LOAD |
| FREESCALE SEMICONDUCTOR, INC. | 13/126038 | METHOD AND APPARATUS FOR GENERATING A CLOCK SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 13/128025 | MANAGEMENT OF MULTIPLE RESOURCE PROVIDERS |
| FREESCALE SEMICONDUCTOR, INC. | 13/128900 | ALLOCATION OF COMMUNICATION CHANNELS |
| FREESCALE SEMICONDUCTOR, INC. | 13/128903 | OPERATING PARAMETER CONTROL FOR A POWER AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 13/129516 | POWER MOS TRANSISTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/129845 | COMPILER OPTIMISATION LIKE IDIOM RECOGNITION THROUGH PATTERN MATCHING USING VALUE NUMBERING |
| FREESCALE SEMICONDUCTOR, INC. | 13/129936 | HIGH POWER SEMICONDUCTOR DEVICE FOR WIRELESS APPLICATIONS AND METHOD OF FORMING A HIGH POWER SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/130187 | CURRENT SENSING CIRCUITRY AND INTEGRATED CIRCUIT AND METHOD FOR SENSING A CURRENT |
| FREESCALE SEMICONDUCTOR, INC. | 13/131349 | CLOCK GLITCH DETECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/133168 | CIRCUIT AND METHOD FOR SPEED MONITORING OF AN ELECTRIC MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/133958 | METHOD, SYSTEM AND INTEGRATED CIRCUIT FOR ENABLING ACCESS TO A MEMORY ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 13/139893 | DETERMINING INITIAL ROTOR POSITION OF AN ALTERNATING CURRENT MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/140025 | SYSTEM AND METHOD FOR EFFICIENT IMAGE FEATURE EXTRACTION |
| FREESCALE SEMICONDUCTOR, INC. | 13/142425 | CAPACITANCE SENSING CIRCUIT AND METHOD OF CAPACITANCE SENSING |
| FREESCALE SEMICONDUCTOR, INC. | 13/142431 | MICROPROCESSOR ARCHITECTURE AND METHOD OF INSTRUCTION DECODING |
| FREESCALE SEMICONDUCTOR, INC. | 13/142857 | PACKAGE ASSEMBLY AND METHOD OF TUNING A NATURAL RESONANT FREQUENCY OF A PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/143550 | PROCESSING DATA FLOWS |
| FREESCALE SEMICONDUCTOR, INC. | 13/143551 | PRIORITY SEARCH TREES |
| FREESCALE SEMICONDUCTOR, INC. | 13/143863 | LOGARITHMIC DETECTOR AND METHOD OF PRE-CHARGING AN AVERAGE FILTER ON A LOGARITHMIC DETECTOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/145122 | INTEGRATED CIRCUIT COMPRISING FREQUENCY GENERATION CIRCUITRY FOR CONTROLLING A FREQUENCY SOURCE |
| FREESCALE SEMICONDUCTOR, INC. | 13/145125 | INTEGRATED CIRCUIT COMPRISING FREQUENCY GENERATION CIRCUITRY FOR CONTROLLING A FREQUENCY SOURCE |
| FREESCALE SEMICONDUCTOR, INC. | 13/149217 | CONTROL OF INTERRUPT GENERATION FOR CACHE |
| FREESCALE SEMICONDUCTOR, INC. | 13/149304 | CACHE LOCKING CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 13/150924 | ACTIVE TILING PLACEMENT FOR IMPROVED LATCH-UP IMMUNITY |
| FREESCALE SEMICONDUCTOR, INC. | 13/151409 | METHOD OF MAKING A DUAL PORT PRESSURE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/153166 | SYSTEMS AND METHODS FOR TRACKING INTELLECTUAL PROPERTY |
| FREESCALE SEMICONDUCTOR, INC. | 13/156346 | METHOD AND SYSTEM FOR ADDRESS CONFLICT RESOLUTION |
| FREESCALE SEMICONDUCTOR, INC. | 13/159635 | HIGH EFFICIENCY AMPLIFIER WITH REDUCED PARASITIC CAPACITANCE |
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FREESCALE SEMICONDUCTOR, INC. 13/159878 SELECTIVE MASKING FOR ERROR CORRECTION

| FREESCALE SEMICONDUCTOR, INC. | 13/160979 | CIRCUIT AND METHOD FOR DETERMINING COMPARATOR OFFSETS OF ELECTRONIC DEVICES |
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| FREESCALE SEMICONDUCTOR, INC. | 13/161954 | LOW VOLTAGE DETECTOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/164009 | METHOD AND APPARATUS FOR SNOOP-AND-LEARN INTELLIGENCE IN DATA PLANE |
| FREESCALE SEMICONDUCTOR, INC. | 13/166552 | RECOVERY METHOD FOR POOR YIELD AT INTEGRATED CIRCUIT DIE PANELIZATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/166561 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING A COBALT SILICIDE |
| FREESCALE SEMICONDUCTOR, INC. | 13/169664 | USING BUILT-IN SELF TEST FOR PREVENTING SIDE CHANNEL SECURITY ATTACKS ON MULTI-PROCESSOR SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 13/170286 | DATA PROCESSING SYSTEM HAVING A SEQUENCE PROCESSING UNIT AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/170289 | DATA PROCESSING SYSTEM HAVING A SEQUENCE PROCESSING UNIT AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/182568 | INTEGRATED ASSIST FEATURES FOR EPITAXIAL GROWTH |
| FREESCALE SEMICONDUCTOR, INC. | 13/182710 | APPARATUS AND METHODS FOR QUAD FLAT NO LEAD PACKAGING |
| FREESCALE SEMICONDUCTOR, INC. | 13/182734 | SYSTEMS AND METHODS FOR MEMORY REGION DESCRIPTOR ATTRIBUTE OVERRIDE |
| FREESCALE SEMICONDUCTOR, INC. | 13/191459 | POWER SUPPLY AND DATA SIGNAL INTERFACE CIRCUIT WITH OVERVOLTAGE PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 13/192976 | METHOD OF MAKING A DIE WITH RECESSED ALUMINUM DIE PADS |
| FREESCALE SEMICONDUCTOR, INC. | 13/193855 | COMBINED OUTPUT BUFFER AND ESD DIODE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/194714 | OSCILLATOR SYSTEMS HAVING ANNULAR RESONANT CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | 13/195505 | CODE COVERAGE CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | 13/201077 | DATA PROCESSING WITH VARIABLE OPERAND SIZE |
| FREESCALE SEMICONDUCTOR, INC. | 13/201977 | SEMICONDUCTOR DEVICE WITH APPRAISAL CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | 13/202775 | INTEGRATED PROTECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/203298 | METHOD AND APPARATUS FOR SELECTING AT LEAST ONE DEVICE TO BE WIRELESSLY CONTROLLED |
| FREESCALE SEMICONDUCTOR, INC. | 13/210281 | METHOD AND DEVICE FOR CONTROLLING DEBUG EVENT RESOURCES |
| FREESCALE SEMICONDUCTOR, INC. | 13/210392 | BRACE FOR LONG BOND WIRE |
| FREESCALE SEMICONDUCTOR, INC. | 13/210563 | ATTACHING A MEMS TO A BONDING WAFER |
| FREESCALE SEMICONDUCTOR, INC. | 13/210566 | SYSTEMS AND METHODS FOR HANDLING INSTRUCTIONS OF IN-ORDER AND OUT-OF-ORDER EXECUTION QUEUES |
| FREESCALE SEMICONDUCTOR, INC. | 13/212420 | SYSTEMS AND METHODS FOR HANDLING INSTRUCTIONS OF IN-ORDER AND OUT-OF-ORDER EXECUTION QUEUES |
| FREESCALE SEMICONDUCTOR, INC. | 13/212478 | MEMORY DEVICE AND METHOD USING ENCODE VALUES FOR ACCESS ERROR CONDITION DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | 13/213387 | DATA PROCESSING SYSTEM OPERABLE IN SINGLE AND MULTI-THREAD MODES AND HAVING MULTIPLE CACHES AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/213831 | MEMORY MANAGEMENT UNIT TAG MEMORY WITH CAM EVALUATE SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 13/213900 | MEMORY MANAGEMENT UNIT TAG MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 13/213992 | IMPLANT FOR PERFORMANCE ENHANCEMENT OF SELECTED TRANSISTORS IN AN INTEGRATED CIRCUIT |

13/214827 CIRCUIT SIMULATION ACCELERATION USING MODEL CACHING

FREESCALE SEMICONDUCTOR, INC.

| FREESCALE SEMICONDUCTOR, INC. | 13/216769 | PHYSICAL VERIFICATION DEVICE AND METHODS THEREOF |
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| FREESCALE SEMICONDUCTOR, INC. | 13/219071 | ANGULAR RATE SENSOR WITH DIFFERENT GAP SIZES |
| FREESCALE SEMICONDUCTOR, INC. | 13/220302 | INTEGRATED CIRCUIT HAVING CRITICAL PATH VOLTAGE SCALING AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/220389 | MULTI-THREADING FLIP-FLOP CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/220891 | BACK SIDE ALIGNMENT STRUCTURE AND MANUFACTURING METHOD FOR THREE-DIMENSIONAL SEMICONDUCTOR DEVICE PACKAGES |
| FREESCALE SEMICONDUCTOR, INC. | 13/220898 | LEAD FRAME HAVING A FLAG WITH IN-PLANE AND OUT-OF-PLANE MOLD LOCKING FEATURES |
| FREESCALE SEMICONDUCTOR, INC. | 13/222143 | SEMICONDUCTOR DEVICE PACKAGING HAVING PRE-ENCAPSULATION THROUGH VIA FORMATION USING DROP-IN SIGNAL CONDUITS |
| FREESCALE SEMICONDUCTOR, INC. | 13/222148 | SEMICONDUCTOR DEVICE PACKAGING HAVING PRE-ENCAPSULATION THROUGH VIA FORMATION USING LEAD FRAMES WITH ATTACHED SIGNAL CONDUITS |
| FREESCALE SEMICONDUCTOR, INC. | 13/222150 | SEMICONDUCTOR DEVICE PACKAGING HAVING PRE-ENCAPSULATION THROUGH VIA FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/222323 | MOSFET MISMATCH CHARACTERIZATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/222335 | MOSFET MISMATCH CHARACTERIZATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/223573 | PROCESS OF FORMING AN ELECTRONIC DEVICE INCLUDING A RESISTOR-CAPACITOR FILTER |
| FREESCALE SEMICONDUCTOR, INC. | 13/227965 | CONTACT FOR A NON-VOLATILE MEMORY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/228001 | DUAL PORT STATIC RANDOM ACCESS MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | 13/228215 | CAPACITIVE SENSOR RADIATION MEASUREMENT |
| FREESCALE SEMICONDUCTOR, INC. | 13/228260 | INCIDENT CAPACITIVE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/233393 | INTEGRATED CIRCUIT HAVING A STANDARD CELL AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 13/234305 | MEMORY MANAGEMENT UNIT (MMU) HAVING REGION DESCRIPTOR GLOBALIZATION CONTROLS AND METHOD OF OEPRATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/235499 | LEVEL SHIFTER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/238791 | PHASE CHANGE MEMORY CELL WITH HEATER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/239640 | ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT FOR AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/239649 | MULTI-PROCESSOR DATA PROCESSING SYSTEM HAVING SYNCHRONIZED EXIT FROM DEBUG MODE AND METHOD THEREFORE |
| FREESCALE SEMICONDUCTOR, INC. | 13/245888 | METHOD OF REDUCING POWER LEAKAGE OF INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/246990 | METHOD FOR PACKAGING AN ELECTRONIC DEVICE ASSEMBLY HAVING A CAPPED DEVICE INTERCONNECT |
| FREESCALE SEMICONDUCTOR, INC. | 13/248348 | INTERFACE SYSTEM AND METHOD WITH BACKWARD COMPATABILITY |
| FREESCALE SEMICONDUCTOR, INC. | 13/249256 | METHOD AND APPARATUS FOR CALCULATING SENSOR MODELLING COEFFICIENTS |
| FREESCALE SEMICONDUCTOR, INC. | 13/249271 | METHOD AND CIRCUIT FOR CALCULATING SENSOR MODELLING COEFFICIENTS |
| FREESCALE SEMICONDUCTOR, INC. | 13/249829 | MEMORY PROTECTION UNIT (MPU) HAVING A SHARED PORTION AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/250368 | METHODS AND APPARATUS FOR TESTING MULTIPLE-IC DEVICES |

| FREESCALE SEMICONDUCTOR, INC. | 13/250385 | VOLTAGE-CONTROLLED OSCILLATORS AND RELATED SYSTEMS |
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| FREESCALE SEMICONDUCTOR, INC. | 13/255250 | RECEIVING NODE IN A PACKET COMMUNICATIONS SYSTEM AND METHOD FOR MANAGING A BUFFER IN A RECEIVING NODE IN A PACKET COMMUNICATIONS SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 13/255520 | RADIO FREQUENCY REMOTE CONTROLLER DEVICE, INTEGRATED CIRCUIT AND METHOD FOR SELECTING AT LEAST ONE DEVICE TO BE CONTROLLED |
| FREESCALE SEMICONDUCTOR, INC. | 13/255523 | CONNECTION QUALITY VERIFICATION FOR INTEGRATED CIRCUIT TEST |
| FREESCALE SEMICONDUCTOR, INC. | 13/258769 | WIRELESS COMMUNICATION DEVICE AND SEMICONDUCTOR PACKAGE DEVICE HAVING A POWER AMPLIFIER THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/258791 | TONE RELAY SYSTEM AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 13/258807 | APPARATUS, COMMUNICATIONS SYSTEM AND METHOD FOR OPTIMIZING DATA PACKET FLOW |
| FREESCALE SEMICONDUCTOR, INC. | 13/268580 | STACKED SEMICONDUCTOR DIE WITH CONTINUOUS CONDUCTIVE VIAS |
| FREESCALE SEMICONDUCTOR, INC. | 13/268681 | STACKED SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 13/269573 | CIRCUIT TO REDUCE PEAK POWER DURING TRANSITION FAULT TESTING OF INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/269574 | HETEROGENEOUS MULTI-CORE INTEGRATED CIRCUIT AND METHOD FOR DEBUGGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 13/272285 | THREE-DIMENSIONAL SOLAR CELL HAVING INCREASED EFFICIENCY |
| FREESCALE SEMICONDUCTOR, INC. | 13/272542 | INTEGRATED CIRCUIT HAVING LATCH-UP RECOVERY CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/272725 | MULTIPLE CORE DATA PROCESSOR WITH USAGE MONITORING |
| FREESCALE SEMICONDUCTOR, INC. | 13/273389 | SUBSTRATE BONDING WITH METAL GERMANIUM SILICON MATERIAL |
| FREESCALE SEMICONDUCTOR, INC. | 13/273622 | SEMICONDUCTOR DEVICE AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | 13/275310 | ON-CHIP VOLTAGE REGULATOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/276875 | GAN-ON-SI SWITCH DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 13/279807 | METHOD OF MAKING A NON-VOLATILE MEMORY CELL HAVING A FLOATING GATE |
| FREESCALE SEMICONDUCTOR, INC. | 13/282192 | INERTIAL SENSOR WITH OFF-AXIS SPRING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 13/282210 | TRANSISTORS WITH DIFFERENT THRESHOLD VOLTAGES |
| FREESCALE SEMICONDUCTOR, INC. | 13/283187 | SYSTEMS AND METHODS FOR SEMAPHORE-BASED PROTECTION OF SHARED SYSTEM RESOURCES |
| FREESCALE SEMICONDUCTOR, INC. | 13/284253 | TRANSMIT POWER CONTROL TECHNIQUES FOR NODES IN AN AD-HOC NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 13/284395 | HIGH SIDE DRIVER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/285073 | SEMICONDUCTOR DEVICE WITH VIAS ON A BRIDGE CONNECTING TWO BUSES |
| FREESCALE SEMICONDUCTOR, INC. | 13/285434 | DATA PROCESSING SYSTEM WITH SAFE CALL AND RETURN |
| FREESCALE SEMICONDUCTOR, INC. | 13/285557 | LATERALLY DIFFUSED METAL OXIDE SEMICONDUCTOR TRANSISTOR FOR RADIO FREQUENCY POWER AMPLIFIER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/286175 | BUILT-IN SELF TRIM FOR NON-VOLATILE MEMORY REFERENCE CURRENT |
| FREESCALE SEMICONDUCTOR, INC. | 13/288037 | SCAN TESTING OF INTEGRATED CIRCUIT WITH CLOCK GATING CELLS |
| FREESCALE SEMICONDUCTOR, INC. | 13/289671 | TESTING A SWITCHED MODE SUPPLY WITH WAVEFORM GENERATOR AND CAPTURE CHANNEL |
| FREESCALE SEMICONDUCTOR, INC. | 13/292103 | METHOD OF PACKAGING SEMICONDUCTOR DIE |

| FREESCALE SEMICONDUCTOR, INC. | 13/292104 | SEMICONDUCTOR SENSOR DEVICE AND METHOD OF PACKAGING SAME |
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| FREESCALE SEMICONDUCTOR, INC. | 13/293119 | PRESSURE SENSOR AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 13/293910 | INSULATED GATE FIELD EFFECT TRANSISTORS |
| FREESCALE SEMICONDUCTOR, INC. | 13/299564 | SEMICONDUCTOR DEVICE PACKAGING HAVING SUBSTRATE WITH PRE- ENCAPSULATION THROUGH VIA FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/299566 | METHOD AND APPARATUS TO IMPROVE RELIABILITY OF VIAS |
| FREESCALE SEMICONDUCTOR, INC. | 13/303166 | SEMICONDUCTOR SENSOR DEVICE WITH FOOTED LID |
| FREESCALE SEMICONDUCTOR, INC. | 13/305410 | METHODS AND APPARATUS TO IMPROVE RELIABILITY OF ISOLATED VIAS |
| FREESCALE SEMICONDUCTOR, INC. | 13/305702 | LOW LEAKAGE CURRENT OPERATION OF INTEGRATED CIRCUIT USING SCAN CHAIN |
| FREESCALE SEMICONDUCTOR, INC. | 13/306983 | MULTI-CORE DECOMPRESSION OF BLOCK CODED VIDEO DATA |
| FREESCALE SEMICONDUCTOR, INC. | 13/307271 | MESSAGE PASSING USING DIRECT MEMORY ACCESS UNIT IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 13/307303 | COMPUTER SYSTEMS AND METHODS FOR REGISTER BASED MESSAGE PASSING |
| FREESCALE SEMICONDUCTOR, INC. | 13/308236 | METHODS AND APPARATUS FOR TESTING MULTIPLE-IC DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 13/313179 | METHOD OF PROTECTING AGAINST VIA FAILURE AND STRUCTURE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/318158 | INTEGRATED CIRCUIT AND INTEGRATED CIRCUIT PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/318542 | INTEGRATED CIRCUIT COMPRISING TRACE LOGIC AND METHOD FOR PROVIDING TRACE INFORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/320575 | TOUCH-SCREEN INTERFACE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/322942 | MULTICHANNEL RECEIVER SYSTEM AND METHOD FOR MULTICHANNEL RECEIVER MONITORING |
| FREESCALE SEMICONDUCTOR, INC. | 13/322944 | INTEGRATED CIRCUIT WITH CHANNEL ESTIMATION MODULE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/324910 | CUSTOMIZED SHIELD PLATE FOR A FIELD EFFECT TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/325092 | SEMICONDUCTOR DEVICE PACKAGING USING ENCAPSULATED CONDUCTIVE BALLS FOR PACKAGE-ON-PACKAGE BACK SIDE COUPLING |
| FREESCALE SEMICONDUCTOR, INC. | 13/325747 | TOUCH SENSE INTERFACE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/326636 | PACKAGED LEADLESS SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/326685 | CONFIGURABLE FLIP-FLOP |
| FREESCALE SEMICONDUCTOR, INC. | 13/339139 | PLANAR INVERTED-F ANTENNAS, AND MODULES AND SYSTEMS IN WHICH THEY ARE INCORPORATED |
| FREESCALE SEMICONDUCTOR, INC. | 13/339165 | EXTENDABLE-ARM ANTENNAS, AND MODULES AND SYSTEMS IN WHICH THEY ARE INCORPORATED |
| FREESCALE SEMICONDUCTOR, INC. | 13/343207 | PROCESS OF FORMING AN ELECTRONIC DEVICE INCLUDING A PLURALITY OF SINGULATED DIE |
| FREESCALE SEMICONDUCTOR, INC. | 13/343331 | NON-VOLATILE MEMORY (NVM) AND LOGIC INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/344415 | CAPACITANCE-TO-VOLTAGE INTERFACE CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 13/344431 | TRANSISTORS AND SEMICONDUCTOR DEVICES WITH OXYGEN-DIFFUSION BARRIER LAYERS |
| FREESCALE SEMICONDUCTOR, INC. | 13/350090 | SEMICONDUCTOR DEVICES WITH NONCONDUCTIVE VIAS |
| FREESCALE SEMICONDUCTOR, INC. | 13/350098 | SEMICONDUCTOR DEVICES WITH COMPLIANT INTERCONNECTS |
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SKEWED SRAM CELL

FREESCALE SEMICONDUCTOR, INC.

| FREESCALE SEMICONDUCTOR, INC. | 13/351937 | FULLY DECOUPLED LATERAL AXIS GYROSCOPE WITH THICKNESS-INSENSITIVE Z-AXIS SPRING AND SYMMETRIC TEETER TOTTER SENSING ELEMENT |
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| FREESCALE SEMICONDUCTOR, INC. | 13/355748 | LOCALIZED ALLOYING FOR IMPROVED BOND RELIABILITY |
| FREESCALE SEMICONDUCTOR, INC. | 13/358137 | SEMICONDUCTOR DEVICE HAVING A NANOTUBE LAYER AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 13/359174 | METHOD OF FORMING A SEMICONDUCTOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 13/360119 | A DELAY LINE PHASE SHIFTER WITH SELECTABLE PHASE SHIFT |
| FREESCALE SEMICONDUCTOR, INC. | 13/360920 | MEMS DEVICE ASSEMBLY AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 13/361171 | ENCAPSULANT WITH COROSION INHIBITOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/361191 | STRUCTURE AND METHOD FOR HEALING TUNNEL DIELECTRIC OF NON-VOLATILE MEMORY CELLS |
| FREESCALE SEMICONDUCTOR, INC. | 13/362636 | PACKAGED INTEGRATED CIRCUIT USING WIRE BONDS |
| FREESCALE SEMICONDUCTOR, INC. | 13/362697 | SEMICOCNDUCTOR DEVICE HAVING DIFFERENT NON-VOLATILE MEMORIES HAVING NANOCRYSTALS OF DIFFERING DENSITIES AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/362720 | SYSTEMS AND METHODS FOR REDUCING BRANCH MISPREDICTION PENALTY |
| FREESCALE SEMICONDUCTOR, INC. | 13/362873 | VIBRATION ROBUST X-AXIS RING GYRO TRANSDUCER |
| FREESCALE SEMICONDUCTOR, INC. | 13/365454 | MEMS DEVICE WITH STRESS ISOLATION AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/366347 | CELLULAR MODEM PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 13/369563 | STACK-BASED TRACE MESSAGE GENERATION FOR DEBUG AND DEVICE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/370282 | POWER SUPPLY CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/370420 | DATA PROCESSING SYSTEM OPERABLE IN SINGLE AND MULTI-THREAD MODES AND HAVING MULTIPLE CACHES AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/371307 | LOW VOLTAGE CMOS POWER ON RESET CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/371635 | METHOD AND APPARATUS FOR HIGH PRESSURE SENSOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/375802 | BATTERY CHARGING CIRCUIT AND ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/376611 | DEVICE FOR FORMING A HIGH-RESOLUTION IMAGE, IMAGING SYSTEM, AND METHOD FOR DERIVING A HIGH-SPATIAL-RESOLUTION IMAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/377991 | INTEGRATED CIRCUIT, COMMUNICATION UNIT AND METHOD FOR PHASE ADJUSTMENT |
| FREESCALE SEMICONDUCTOR, INC. | 13/378230 | DEGREE-OF-FOCUS DETERMINATION MODULE, POSITION-OF-BEST-FOCUS SELECTION MODULES, IMAGE PROCESSING MODULE, IMAGING SYSTEM, AND CORRESPONDING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 13/378239 | INTEGRATED CIRCUIT COMPRISING VOLTAGE MODULATION CIRCUITRY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/382716 | DIVERSITY ANTENNA SYSTEM AND TRANSMISSION METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 13/382779 | DATA ADMINISTRATION UNIT, DATA ACCESS UNIT, NETWORK ELEMENT, NETWORK, AND METHOD FOR UPDATING A DATA STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 13/382789 | INTEGRATED CIRCUIT, TRANSCEIVER AND METHOD FOR LEAKAGE CANCELLATION IN A RECEIVE PATH |
| FREESCALE SEMICONDUCTOR, INC. | 13/382796 | SIGNAL PROCESSING SYSTEM AND INTEGRATED CIRCUIT COMPRISING A PREFETCH MODULE AND METHOD THEREFOR |
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DIVERSITY RECEIVER AND TRANSCEIVER

FREESCALE SEMICONDUCTOR, INC.

| FREESCALE SEMICONDUCTOR, INC. | 13/384835 | SIGNAL PROCESSING SYSTEM, INTEGRATED CIRCUIT COMPRISING BUFFER CONTROL LOGIC AND METHOD THEREFOR |
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| FREESCALE SEMICONDUCTOR, INC. | 13/388468 | CONTROLLER SYSTEM, INTEGRATED CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/389194 | TRANSISTOR POWER SWITCH DEVICE AND METHOD OF MEASURING ITS CHARACTERISTICS |
| FREESCALE SEMICONDUCTOR, INC. | 13/389205 | ENCODING MODULE, APPARATUS AND METHOD FOR DETERMINING A POSITION OF A DATA BIT WITHIN AN INTERLEAVED DATA STREAM |
| FREESCALE SEMICONDUCTOR, INC. | 13/391296 | DEVICE AND METHOD FOR TURBO-ENCODING A BLOCK OF DATA |
| FREESCALE SEMICONDUCTOR, INC. | 13/391744 | SOFTWARE PROBE MINIMIZATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/392638 | DUTY CYCLE CORRECTOR AND DUTY CYCLE CORRECTION METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 13/392925 | DEVICE AND METHOD FOR PERFORMING BITWISE MANIPULATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 13/392977 | SYSTEM AND METHOD FOR FILTERING RECEIVED DATA UNITS |
| FREESCALE SEMICONDUCTOR, INC. | 13/393589 | DISTRIBUTED DEBUG SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 13/397034 | SEMICONDUCTOR DEVICE PACKAGE HAVING BACKSIDE CONTACT AND METHOD FOR MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | 13/397452 | DATA PROCESSING SYSTEM WITH LATENCY TOLERANCE EXECUTION |
| FREESCALE SEMICONDUCTOR, INC. | 13/398177 | TRANSISTOR-LEVEL LAYOUT SYNTHESIS |
| FREESCALE SEMICONDUCTOR, INC. | 13/398811 | SEMICONDUCTOR DEVICES AND METHODS OF ASSEMBLING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 13/398816 | METHOD OF PACKAGING SEMICONDUCTOR DIE WITH CAP ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 13/400966 | MEMS PRESSURE TRANSDUCER ASSEMBLY AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 13/401847 | SYSTEM FOR TESTING ELECTRONIC CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 13/402413 | Embedded Electrical Component Surface Interconnect |
| FREESCALE SEMICONDUCTOR, INC. | 13/403458 | METHOD FOR FORMING DIE ASSEMBLY WITH HEAT SPREADER |
| FREESCALE SEMICONDUCTOR, INC. | 13/403597 | RECOVERABLE AND RECONFIGURABLE PIPELINE STRUCTURE FOR STATERETENTION POWER GATING |
| FREESCALE SEMICONDUCTOR, INC. | 13/403743 | METAL-INSULATOR-METAL CAPACITOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/403964 | INTER-PARTITION COMMUNICATION IN MULTI-CORE PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/403969 | DATA PROCESSOR WITH ASYNCHRONOUS SYSTEM RESET |
| FREESCALE SEMICONDUCTOR, INC. | 13/404945 | EMBEDDED ELECTRONIC COMPONENT |
| FREESCALE SEMICONDUCTOR, INC. | 13/405965 | HIERARCHICAL ERROR CORRECTION |
| FREESCALE SEMICONDUCTOR, INC. | 13/406439 | COMBINED ENVIRONMENTAL PARAMETER SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/412680 | BIPOLAR PRIMARY SENSE AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 13/413162 | METHOD FOR IMPLEMENTING SECURITY OF NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 13/413440 | SEMICONDUCTOR DEVICE WITH COMPOSITE DRIFT REGION |
| FREESCALE SEMICONDUCTOR, INC. | 13/413652 | SEMICONDUCTOR PACKAGE AND LEAD FRAME THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/414697 | METHOD FOR TESTING COMPARATOR AND DEVICE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/415196 | MULTIPLE PAGE SIZE MEMORY MANAGEMENT UNIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/416892 | CIRCUIT AND METHOD FOR MEASURING VOLTAGE |
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| FREESCALE SEMICONDUCTOR, INC. | 13/419531 | DATA PROCESSING SYSTEM WITH LATENCY TOLERANCE EXECUTION |
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| FREESCALE SEMICONDUCTOR, INC. | 13/431469 | MICROELECTROMECHANICAL SYSTEM PACKAGE AND METHOD OF TESTING |
| FREESCALE SEMICONDUCTOR, INC. | 13/431506 | INTEGRATED CIRCUIT HAVING A STAGGERED HETEROJUNCTION BIPOLAR TRANSISTOR ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | 13/435089 | PHASE LOCKED LOOP WITH ADAPTIVE LOOP FILTER |
| FREESCALE SEMICONDUCTOR, INC. | 13/435981 | FULLY COMPLEMENTARY SELF-BIASED DIFFERENTIAL RECEIVER WITH STARTUP CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/436052 | SYSTEMS WITH MULTIPLE PORT RANDOM NUMBER GENERATORS AND METHODS OF THEIR OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/436074 | RANDOM VALUE PRODUCTION METHODS AND SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 13/439857 | VITERBI DECODER FOR DECODING CONVOLUTIONALLY ENCODED DATA STREAM |
| FREESCALE SEMICONDUCTOR, INC. | 13/440728 | SYSTEM AND METHOD FOR CACHE ACCESS |
| FREESCALE SEMICONDUCTOR, INC. | 13/441217 | ELECTRONIC DEVICES WITH MULTIPLE AMPLIFIER STAGES AND METHODS OF THEIR MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 13/441335 | SMART CHARGE PUMP CONFIGURATION FOR NONVOLATILE MEMORIES |
| FREESCALE SEMICONDUCTOR, INC. | 13/441414 | WRITE CONTENTION-FREE, NOISE-TOLERANT MULTIPORT BITCELL |
| FREESCALE SEMICONDUCTOR, INC. | 13/441426 | NON-VOLATILE MEMORY (NVM) AND LOGIC INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/441448 | INTEGRATED CIRCUIT PACKAGE AND METHOD OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | 13/441924 | LEAD FRAME WITH GROOVED LEAD FINGER |
| FREESCALE SEMICONDUCTOR, INC. | 13/442014 | SEMICONDUCTOR DEVICE WITH EMBEDDED HEAT SPREADING |
| FREESCALE SEMICONDUCTOR, INC. | 13/442015 | SEMICONDUCTOR DEVICE WITH HEAT DISSIPATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/442028 | EMULATED ELECTRICALLY ERASABLE MEMORY HAVING SECTOR MANAGEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 13/442046 | RERAM DEVICE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 13/442142 | LOGIC TRANSISTOR AND NON-VOLATILE MEMORY CELL INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/442878 | METHOD OF ASSEMBLING SEMICONDUCTOR DEVICE WITH INSULATING SUBSTRATE AND HEAT SINK |
| FREESCALE SEMICONDUCTOR, INC. | 13/443720 | TEMPERATURE SENSOR DIODE |
| FREESCALE SEMICONDUCTOR, INC. | 13/443906 | SEMICONDUCTOR TRAY CARRIER |
| FREESCALE SEMICONDUCTOR, INC. | 13/444195 | HIGH PRECISION SINGLE EDGE CAPTURE AND DELAY MEASUREMENT CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/445582 | CONTROLLER FOR MANAGING A RESET OF A SUBSET OF THREADS IN A MULTI-THREAD SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 13/447305 | INTEGRATED CIRCUIT POWER MANAGEMENT VERIFICATION METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 13/447369 | METHOD OF FORMING AN INVERTED T SHAPED CHANNEL STRUCTURE FOR AN INVERTED T CHANNEL FIELD EFFECT TRANSISTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/448062 | Semiconductor Device with False Drain |
| FREESCALE SEMICONDUCTOR, INC. | 13/448531 | SPLIT-GATE NON-VOLATILE MEMORY CELLS HAVING IMPROVED OVERLAP TOLERANCE |
| FREESCALE SEMICONDUCTOR, INC. | 13/448994 | Semiconductor Device with Integrated Breakdown Protection |
| FREESCALE SEMICONDUCTOR, INC. | 13/449411 | PREDICATE TRACE COMPRESSION |
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FREESCALE SEMICONDUCTOR, INC.

Sharing Stacked BJT Clamps for System Level ESD Protection

| FREESCALE SEMICONDUCTOR, INC. | 13/452501 | ERROR DETECTION WITHIN A MEMORY |
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| FREESCALE SEMICONDUCTOR, INC. | 13/452838 | TWO-TOUCH GESTURE DETECTION ON A FOUR-WIRE RESISTIVE TOUCHSCREEN |
| FREESCALE SEMICONDUCTOR, INC. | 13/453127 | High Speed Gallium Nitride Transistor Devices |
| FREESCALE SEMICONDUCTOR, INC. | 13/454505 | DIRECT MEMORY ACCESS BUFFER UTILIZATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/455154 | PRESSURE SENSOR DEVICE AND METHOD OF ASSEMBLING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 13/455400 | SAMPLE AND HOLD CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/455800 | APPARATUS AND METHOD FOR MEMORY COPY AT A PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/456217 | BUFFER AND CONTROL CIRCUIT FOR SYNCHRONOUS MEMORY CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | 13/457248 | MEMORY WITH WORD LEVEL POWER GATING |
| FREESCALE SEMICONDUCTOR, INC. | 13/457669 | EMULATED ELECTRICALLY ERASABLE MEMORY PARALLEL RECORD MANAGEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 13/458205 | DELAY COMPENSATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/458224 | VERTICALLY PACKAGED INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/458537 | SENSOR DEVICE AND RELATED FABRICATION METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 13/458947 | MIM CAPACITOR FORMATION METHOD AND STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 13/458950 | MICROELECTROMECHANICAL SYSTEMS DEVICES AND METHODS FOR THE FABRICATION THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/459344 | ERASING A NON-VOLATILE MEMORY (NVM) SYSTEM HAVING ERROR CORRECTION CODE (ECC) |
| FREESCALE SEMICONDUCTOR, INC. | 13/459500 | NON-VOLATILE MEMORY (NVM) RESET SEQUENCE WITH BUILT-IN READ CHECK |
| FREESCALE SEMICONDUCTOR, INC. | 13/459545 | METHOD THE CONFIGURE SERIAL COMMUNICATIONS AND DEVICE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/459841 | FIFO BUFFER SYSTEM PROVIDING SAME CLOCK CYCLE RESPONSE TO POP COMMANDS |
| FREESCALE SEMICONDUCTOR, INC. | 13/460020 | GLASS FRIT WAFER BOND PROTECTIVE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 13/460213 | METHOD AND SYSTEM FOR WAFER AND STRIP LEVEL BATCH DIE ATTACH ASSEMBLY |
| FREESCALE SEMICONDUCTOR, INC. | 13/460226 | METHOD AND APPARATUS FOR RADIO-FREQUENCY CONTROLLABLE LED LAMP FIXTURE ANTENNA |
| FREESCALE SEMICONDUCTOR, INC. | 13/460287 | Virtualized Instruction Extensions for System Partitioning |
| FREESCALE SEMICONDUCTOR, INC. | 13/460719 | Cryptographic Processing with Random Number Generator Checking |
| FREESCALE SEMICONDUCTOR, INC. | 13/461799 | SEMICONDUCTOR DEVICE WITH HEAT SPREADER |
| FREESCALE SEMICONDUCTOR, INC. | 13/461801 | SEMICONDUCTOR DEVICE WITH STAGGERED LEADS |
| FREESCALE SEMICONDUCTOR, INC. | 13/462823 | METHOD AND SYSTEM FOR TESING OSCILLATING CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/462827 | FLANK WETTABLE SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/462993 | APPARATUS AND METHOD FOR DYNAMIC ALLOCATION OF EXECUTION QUEUES |
| FREESCALE SEMICONDUCTOR, INC. | 13/463034 | Verification of Design Derived From Power Intent |
| FREESCALE SEMICONDUCTOR, INC. | 13/465651 | TESTER AND METHOD FOR TESTING A STRIP OF DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 13/465761 | Semiconductor Device with Drain-End Drift Diminution |
| FREESCALE SEMICONDUCTOR, INC. | 13/466642 | MISMATCH VERIFICATION DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/470448 | PASSIVATED TEST STRUCTURES TO ENABLE SAW SINGULATION OF WAFER |
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FREESCALE SEMICONDUCTOR, INC. 13/451876

METHODS AND SYSTEMS FOR ERASE BIASING OF SPLIT-GATE NON-VOLATILE MEMORY CELLS

| FREESCALE SEMICONDUCTOR, INC. | 13/471402 | Cell Balance Configuration for Pin Count Reduction |
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| FREESCALE SEMICONDUCTOR, INC. | 13/472319 | SYSTEMS AND METHODS FOR PROVIDING SEMAPHORE-BASED PROTECTION OF SYSTEM RESOURCES |
| FREESCALE SEMICONDUCTOR, INC. | 13/475947 | TAMPER DETECTOR FOR SECURE MODULE |
| FREESCALE SEMICONDUCTOR, INC. | 13/475948 | MEMORY BUILT-IN-SELF-TESTING IN MULTI-CORE INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/476711 | TEST FLOW TO DETECT A LATENT LEAKY BIT OF A NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 13/477764 | LOW-TEMPERATURE FLIP CHIP DIE ATTACH |
| FREESCALE SEMICONDUCTOR, INC. | 13/478557 | CAVITY-TYPE SEMICONDUCTOR PACKAGE AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 13/479168 | SENSOR DEVICE AND RELATED OPERATING METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 13/479319 | NON-OVERLAPPING CLOCK GENERATOR CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 13/479668 | PHOTRONIC DEVICE WITH REFLECTOR AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 13/480931 | TRANSISTORS WITH DUAL LAYER PASSIVATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/480971 | STATE RETENTION SUPPLY VOLTAGE DISTRIBUTION USING CLOCK NETWORK SHIELDING |
| FREESCALE SEMICONDUCTOR, INC. | 13/480977 | VEHICLE-BORNE RADAR SYSTEMS WITH CONTINUOUS-TIME, SIGMA DELTA ANALOG-TO-DIGITAL CONVERTERS, AND METHODS OF THEIR OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/481908 | HANDLING OF WAKE-UP MESSAGES IN CONTROLLER AREA NETWORKS |
| FREESCALE SEMICONDUCTOR, INC. | 13/482332 | MEMS Sensor With Stress Isolation and Method of Fabrication |
| FREESCALE SEMICONDUCTOR, INC. | 13/483064 | SEMICONDUCTOR DEVICE WITH REDISTRIBUTED CONTACTS |
| FREESCALE SEMICONDUCTOR, INC. | 13/483069 | MULTI-CORE WIRE |
| FREESCALE SEMICONDUCTOR, INC. | 13/483764 | MULTI-PORT REGISTER FILE WITH MULTIPLEXED DATA |
| FREESCALE SEMICONDUCTOR, INC. | 13/483968 | STRESS-BASED TECHNIQUES FOR DETECTING AN IMMINENT READFAILURE IN A NON-VOLATILE MEMORY ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | 13/484022 | TECHNIQUES FOR CHECKING COMPUTER-AIDED DESIGN LAYERS OF A DEVICE TO REDUCE THE OCCURRENCE OF MISSING DECK RULES |
| FREESCALE SEMICONDUCTOR, INC. | 13/484304 | SAMPLING SWITCH CIRCUIT THAT USES CORRELATED LEVEL SHIFTING |
| FREESCALE SEMICONDUCTOR, INC. | 13/484326 | CIRCUITRY INCLUDING RESISTIVE RANDOM ACCESS MEMORY STORAGE CELLS AND METHODS FOR FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 13/484353 | MOLD COMPOUND COMPATIBILITY TEST SYSTEM AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/484664 | SYSTEM, METHOD AND APPARATUS FOR HIGH POWER LEADLESS SURFACE MOUNTED SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/485078 | PROCESSOR RESOURCE AND EXECUTION PROTECTION METHODS AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 13/485120 | Virtualized Interrupt Delay Mechanism |
| FREESCALE SEMICONDUCTOR, INC. | 13/485742 | VOLTAGE-CONTROLLED OSCILLATORS AND RELATED SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 13/485886 | METHODS AND STRUCTURES FOR REDUCING HEAT EXPOSURE OF THERMALLY SENSITIVE SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 13/485912 | INTEGRATED CIRCUIT DIE ASSEMBLY WITH HEAT SPREADER |
| FREESCALE SEMICONDUCTOR, INC. | 13/486641 | FIELD FOCUSING FEATURES IN A RERAM CELL |
| FREESCALE SEMICONDUCTOR, INC. | 13/486690 | FIELD FOCUSING FEATURES IN A RERAM CELL |
| FREESCALE SEMICONDUCTOR, INC. | 13/488446 | METHOD FOR DETERMINING COORDINATES |
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| FREESCALE SEMICONDUCTOR, INC. | 13/488452 | TEST EQUIPMENT MANIFOLD INTERFACE |
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| FREESCALE SEMICONDUCTOR, INC. | 13/489139 | INDUCTIVE ELEMENT WITH INTERRUPTER REGION AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 13/489460 | BACKLIT VIDEO DISPLAY WITH DYNAMIC LUMINANCE SCALING |
| FREESCALE SEMICONDUCTOR, INC. | 13/489462 | METHOD OF ASSEMBLING SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/489466 | METHOD OF APPARATUS FOR MOLDING SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/489471 | SEMICONDUCTOR DEVICE AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 13/490451 | STACKED DIE SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/491712 | CLOCKED MEMORY WITH LATCHING PREDECODER CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | 13/491722 | CLOCKED MEMORY WITH WORD LINE ACTIVATION DURING A FIRST PORTION OF THE CLOCK CYCLE |
| FREESCALE SEMICONDUCTOR, INC. | 13/491760 | INTEGRATING FORMATION OF A REPLACEMENT GATE TRANSISTOR AND A NON-VOLATILE MEMORY CELL USING AN INTERLAYER DIELECTRIC |
| FREESCALE SEMICONDUCTOR, INC. | 13/491771 | INTEGRATING FORMATION OF A REPLACEMENT GATE TRANSISTOR AND A NON-VOLATILE MEMORY CELL USING A HIGH-K DIELECTRIC |
| FREESCALE SEMICONDUCTOR, INC. | 13/493814 | MODIFIED HIGH-K GATE DIELECTRIC STACK |
| FREESCALE SEMICONDUCTOR, INC. | 13/494160 | TEST VEHICLES FOR ENCAPSULATED SEMICONDUCTOR DEVICE PACKAGES |
| FREESCALE SEMICONDUCTOR, INC. | 13/494501 | VRS INTERFACE WITH 1/T ARMING FUNCTION |
| FREESCALE SEMICONDUCTOR, INC. | 13/495011 | SEMICONDUCTOR DEVICE DIE BONDING |
| FREESCALE SEMICONDUCTOR, INC. | 13/495013 | METHOD OF TESTING PARALLEL POWER CONNECTIONS OF SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/500362 | PIXEL DATA PROCESSING APPARATUS AND METHOD OF PROCESSING PIXEL DATA |
| FREESCALE SEMICONDUCTOR, INC. | 13/500691 | INTEGRATED CIRCUITS AND METHODS FOR DEBUGGING |
| FREESCALE SEMICONDUCTOR, INC. | 13/500700 | RESPONSE TO WEAROUT IN AN ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/501472 | CONFERENCE CALL SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | 13/502378 | MEMORY DEVICE AND METHOD FOR SENSING A CONTENT OF A MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | 13/503861 | VERTICAL POWER TRANSISTOR DEVICE, SEMICONDUCTOR DIE AND METHOD OF MANUFACTURING A VERTICAL POWER TRANSISTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/503862 | INTEGRATED CIRCUIT AND METHOD FOR REDUCTION OF SUPPLY VOLTAGE CHANGES |
| FREESCALE SEMICONDUCTOR, INC. | 13/504737 | INTEGRATED CIRCUIT AND METHOD FOR REDUCING VIOLATIONS OF A TIMING CONSTRAINT |
| FREESCALE SEMICONDUCTOR, INC. | 13/508066 | RECEIVER AND METHOD FOR EQUALIZING SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 13/508091 | AREA EFFICIENT COUNTERS ARRAY SYSTEM AND METHOD FOR UPDATING COUNTERS |
| FREESCALE SEMICONDUCTOR, INC. | 13/508279 | ADVANCED COMMUNICATION CONTROLLER UNIT AND METHOD FOR RECORDING PROTOCOL EVENTS |
| FREESCALE SEMICONDUCTOR, INC. | 13/509922 | BYPASS CAPACITOR CIRCUIT AND METHOD OF PROVIDING A BYPASS CAPACITANCE FOR AN INTEGRATED CIRCUIT DIE |
| FREESCALE SEMICONDUCTOR, INC. | 13/510011 | PUMP SYSTEM AND MOTORIZED VEHICLE |
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CIRCUIT AND ELECTRONIC DEVICE

METHOD FOR COMPENSATING A TIMING SIGNAL, AN INTEGRATED

13/510103

FREESCALE SEMICONDUCTOR, INC.

| FREESCALE SEMICONDUCTOR, INC. | 13/510312 | METHOD AND SYSTEM FOR ENABLING ACCESS TO FUNCTIONALITY PROVIDED BY RESOURCES OUTSIDE OF AN OPERATING SYSTEM ENVIRONMENT |
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| FREESCALE SEMICONDUCTOR, INC. | 13/511321 | INTEGRATED CIRCUIT COMPRISING REFERENCE VOLTAGE GENERATION CIRCUITRY AND ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/511974 | MULTI-CHIP DEVICE WITH TEMPERATURE CONTROL ELEMENT FOR TEMPERATURE CALIBRATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/517842 | REDISTRIBUTED CHIP PACKAGING WITH THERMAL CONTACT TO DEVICE BACKSIDE |
| FREESCALE SEMICONDUCTOR, INC. | 13/521478 | A NETWORK ELEMENT, TELECOMMUNICATION SYSTEM, INTEGRATED CIRCUIT AND A METHOD FOR PROVIDING A TELEPHONY CONNECTION |
| FREESCALE SEMICONDUCTOR, INC. | 13/522382 | DEBUGGER SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR DEBUGGING INSTRUCTIONS |
| FREESCALE SEMICONDUCTOR, INC. | 13/522865 | CHIP DAMAGE DETECTION DEVICE FOR A SEMICONDUCTOR INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/523675 | SENSING DEVICE AND RELATED OPERATING METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 13/524555 | SENSE AMPLIFIER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/524918 | SYSTEM AND METHOD FOR IMPROVED JOB PROCESSING TO REDUCE CONTENTION FOR SHARED RESOURCES |
| FREESCALE SEMICONDUCTOR, INC. | 13/524947 | SYSTEM AND METHOD FOR IMPROVED JOB PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 13/525347 | POWER MANAGEMENT SYSTEM FOR ELECTRONIC CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/525348 | SYSTEM FOR REDUCING MEMORY LATENCY IN PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/525494 | Temporal Multithreading |
| FREESCALE SEMICONDUCTOR, INC. | 13/525882 | Synchronous Rectifier Timer for Discontinuous Mode DC/DC Converter |
| FREESCALE SEMICONDUCTOR, INC. | 13/528375 | Trench FET with Source Recess Etch |
| FREESCALE SEMICONDUCTOR, INC. | 13/529589 | Semiconductor Device with Floating RESURF Region |
| FREESCALE SEMICONDUCTOR, INC. | 13/529595 | Semiconductor Device Apparatus and Assembly with Opposite Die Orientations |
| FREESCALE SEMICONDUCTOR, INC. | 13/529601 | CELL ROUTABILITY PRIORITIZATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/530081 | SCAN TESTING OF INTEGRATED CIRCUITS AND ON-CHIP MODULES |
| FREESCALE SEMICONDUCTOR, INC. | 13/530085 | CHANNEL DIAGNOSTIC SYSTEM FOR SENT RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | 13/530095 | SYSTEM FOR REDUCING DYNAMIC POWER CONSUMPTION OF WAKEUP SOURCE |
| FREESCALE SEMICONDUCTOR, INC. | 13/530117 | METHOD OF MAKING SURFACE MOUNT STACKED SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 13/530118 | SEMICONDUCTOR DEVICE WITH REDISTRIBUTED CONTACTS |
| FREESCALE SEMICONDUCTOR, INC. | 13/530169 | EMULATED ELECTRICALLY ERASABLE MEMORY HAVING AN ADDRESS RAM FOR DATA STORED IN FLASH MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 13/531317 | Equivalence Classes Over Parameter State Space |
| FREESCALE SEMICONDUCTOR, INC. | 13/532804 | SYSTEM AND METHOD FOR SOFT ERROR DETECTION IN MEMORY DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 13/532973 | METHOD FOR PRECONDITIONING THIN FILM STORAGE ARRAY FOR DATA RETENTION |
| FREESCALE SEMICONDUCTOR, INC. | 13/533501 | IMAGE REJECTION FOR LOW IF RECEIVERS |
| FREESCALE SEMICONDUCTOR, INC. | 13/533610 | Semiconductor Device with Selectively Etched Surface Passivation |
| FREESCALE SEMICONDUCTOR, INC. | 13/533645 | CODEWORD ERROR INJECTION VIA CHECKBIT MODIFICATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/533651 | Semiconductor Device with Selectively Etched Surface Passivation |
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METHODS FOR FORMING HIGH GAIN TUNABLE BIPOLAR TRANSISTORS

13/534971

FREESCALE SEMICONDUCTOR, INC.

| FREESCALE SEMICONDUCTOR, INC. | 13/535028 | METHODS AND STRUCTURES FOR REDUCING HEAT EXPOSURE OF THERMALLY SENSITIVE SEMICONDUCTOR DEVICES |
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| FREESCALE SEMICONDUCTOR, INC. | 13/535438 | FILM-ASSIST MOLDED GEL-FILL CAVITY PACKAGE WITH OVERFLOW RESERVOIR |
| FREESCALE SEMICONDUCTOR, INC. | 13/536307 | SPLIT GATE PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | 13/536694 | Method for Analyzing Placement Context Sensitivity of Standard Cells |
| FREESCALE SEMICONDUCTOR, INC. | 13/537209 | MEMORY WITH WORD LINE ACCESS CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 13/537299 | Schottky Diode with Leakage Current Control Structures |
| FREESCALE SEMICONDUCTOR, INC. | 13/537308 | ANALOG TO DIGITAL CONVERSION ARCHITECTURE AND METHOD WITH INPUT AND REFERENCE VOLTAGE SCALING |
| FREESCALE SEMICONDUCTOR, INC. | 13/537388 | A SEMICONDUCTOR PACKAGE STRUCTURE HAVING AN AIR GAP AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | 13/537392 | SEMICONDUCTOR DEVICE PACKAGE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 13/537619 | HIGH BREAKDOWN VOLTAGE LDMOS DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/538200 | METHOD AND DEVICE FOR LOW POWER CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 13/538496 | SYSTEMS AND METHODS FOR ANALYZING TRANSACTIONS IN A COMPUTER SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 13/538529 | SEMICONDUCTOR DEVICE AND DRIVER CIRCUIT WITH DRAIN AND ISOLATION STRUCTURE INTERCONNECTED THROUGH A DIODE CIRCUIT, AND METHOD OF MANUFACTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/538565 | SEMICONDUCTOR DEVICE AND DRIVER CIRCUIT WITH SOURCE AND ISOLATION STRUCTURE INTERCONNECTED THROUGH A DIODE CIRCUIT, AND METHOD OF MANUFACATURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/538577 | SEMICONDUCTOR DEVICE AND DRIVER CIRCUIT WITH A CURRENT CARRYING REGION AND ISOLATION STRUCTURE INTERCONNECTED THROUGH A RESISTOR CIRCUIT, AND METHOD OF MANUFACTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/538585 | POWER TRANSISTOR WITH HEAT DISSIPATION AND METHOD THEREFORE |
| FREESCALE SEMICONDUCTOR, INC. | 13/539070 | Applications for Nanopillar Structures |
| FREESCALE SEMICONDUCTOR, INC. | 13/540606 | Virtualized Trusted Descriptors |
| FREESCALE SEMICONDUCTOR, INC. | 13/540634 | DIGITAL GLITCH FILTER |
| FREESCALE SEMICONDUCTOR, INC. | 13/544181 | Angular Rate Sensor With Quadrature Error Compensation |
| FREESCALE SEMICONDUCTOR, INC. | 13/544430 | DEVICE PACKAGE WITH RIGID INTERCONNECT STRUCTURE CONNECTING DIE AND SUBSTRATE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/545746 | BIPOLAR TRANSISTOR WITH HIGH BREAKDOWN VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/545774 | HIGH ISOLATION SWITCH |
| FREESCALE SEMICONDUCTOR, INC. | 13/546902 | Sensor Package and Method of Forming Same |
| FREESCALE SEMICONDUCTOR, INC. | 13/547042 | BANDGAP REFERENCE CIRCUIT AND REGULATOR CIRCUIT WITH COMMON AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | 13/547045 | METHOD AND SYSTEM FOR BOOTING ELECTRONIC DEVICE FROM NAND FLASH MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 13/547049 | SYSTEM FOR TESTING ERROR DETECTION CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 13/548304 | SHALLOW TRENCH ISOLATION FOR SOI STRUCTURES COMBINING SIDEWALL SPACER AND BOTTOM LINER |
| FREESCALE SEMICONDUCTOR, INC. | 13/548843 | METHODS AND STRUCTURES FOR MULTIPORT MEMORY DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 13/548846 | WORD LINE DRIVER CIRCUITS AND METHODS FOR SRAM BIT CELL WITH REDUCED BIT LINE PRE-CHARGE VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/548848 | SRAM BIT CELL WITH REDUCED BIT LINE PRECHARGE VOLTAGE |
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| FREESCALE SEMICONDUCTOR, INC. | 13/549040 | CLASSIFYING PROCESSOR TESTCASES |
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| FREESCALE SEMICONDUCTOR, INC. | 13/549342 | CORE-AFFINE PROCESSING ON SYMMETRIC MULTIPROCESSING SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 13/549515 | PROXIMITY OR TOUCH SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/549517 | QFN DEVICE AND LEAD FRAME THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/549518 | POWER DEVICE AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 13/550627 | PACKAGED SEMICONDUCTOR DIE WITH POWER RAIL PADS |
| FREESCALE SEMICONDUCTOR, INC. | 13/550676 | ERROR DETECTION AT AN OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/551220 | TECHNIQUES FOR REDUCING PROCESSOR POWER CONSUMPTION THROUGH DYNAMIC PROCESSOR RESOURCE ALLOCATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/552527 | VIRTUALIZED PROTECTED STORAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/554034 | SEMICONDUCTOR PACKAGE DESIGN PROVIDING REDUCED ELECTROMAGNETIC COUPLING BETWEEN CIRCUIT COMPONENTS |
| FREESCALE SEMICONDUCTOR, INC. | 13/554828 | Method and System for Phase Compensation in Multi-Path Communication Device |
| FREESCALE SEMICONDUCTOR, INC. | 13/555848 | CONFIGURABLE MULTISTAGE CHARGE PUMP USING A SUPPLY DETECT SCHEME |
| FREESCALE SEMICONDUCTOR, INC. | 13/556257 | Prediction of Electronic Component Behavior in Bus-Based Systems |
| FREESCALE SEMICONDUCTOR, INC. | 13/557449 | METHODS AND SYSTEMS FOR ADJUSTING NVM CELL BIAS CONDITIONS FOR READ/VERIFY OPERATIONS TO COMPENSATE FOR PERFORMANCE DEGRADATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/557481 | METHODS AND SYSTEMS FOR ADJUSTING NVM CELL BIAS CONDITIONS BASED UPON OPERATING TEMPERATURE TO REDUCE PERFORMANCE DEGRADATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/557629 | METHODS AND SYSTEMS FOR ADJUSTING NVM CELL BIAS CONDITIONS FOR PROGRAM/ERASE OPERATIONS TO REDUCE PERFORMANCE DEGRADATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/560010 | SINGLE-EVENT LATCH-UP PREVENTION TECHNIQUES FOR A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/560533 | HYBRID TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/561959 | LDMOS DEVICE AND METHOD FOR IMPROVED SOA |
| FREESCALE SEMICONDUCTOR, INC. | 13/561990 | METHODS FOR PRODUCING STACKED ELECTROSTATIC DISCHARGE CLAMPS |
| FREESCALE SEMICONDUCTOR, INC. | 13/562398 | METHOD FOR PLATING A SEMICONDUCTOR PACKAGE LEAD |
| FREESCALE SEMICONDUCTOR, INC. | 13/562443 | METHOD AND SYSTEM FOR DERIVED LAYER CHECKING FOR SEMICONDUCTOR DEVICE DESIGN |
| FREESCALE SEMICONDUCTOR, INC. | 13/562534 | METHOD FOR FORMING AN ELECTRICAL CONNECTION BETWEEN METAL LAYERS |
| FREESCALE SEMICONDUCTOR, INC. | 13/562538 | METHOD FOR FORMING AN ELECTRICAL CONNECTION BETWEEN METAL LAYERS |
| FREESCALE SEMICONDUCTOR, INC. | 13/562853 | CAPACITIVE PRESSURE SENSOR IN AN OVERMOLDED PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/563224 | DEVICES AND METHODS FOR CONTROLLING MEMORY CELL PRECHARGE OPERATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 13/563233 | RERAM DEVICE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 13/564490 | SPACE EFFICIENT CHECKPOINT FACILITY AND TECHNIQUE FOR PROCESSOR WITH INTEGRALLY INDEXED REGISTER MAPPING AND FREE-LIST ARRAYS |
| FREESCALE SEMICONDUCTOR, INC. | 13/564505 | VARIABLE RELUCTANCE SENSOR INTERFACE WITH INTEGRATION BASED ARMING THRESHOLD |

| FREESCALE SEMICONDUCTOR, INC. | 13/566363 | METHOD AND APPARATUS FOR LIMITING ACCESS TO AN INTEGRATED CIRCUIT (IC) |
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| FREESCALE SEMICONDUCTOR, INC. | 13/567035 | MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/569148 | Block-Based Crest Factor Reduction |
| FREESCALE SEMICONDUCTOR, INC. | 13/570843 | Interrupt priority management using partition-based priority blocking processor registers |
| FREESCALE SEMICONDUCTOR, INC. | 13/570874 | Processor interrupt interface with interrupt partitioning and virtualization enhancements |
| FREESCALE SEMICONDUCTOR, INC. | 13/574889 | INTEGRATED CIRCUIT DEVICE AND METHOD OF USING COMBINATORIAL LOGIC IN A DATA PROCESSING CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/577072 | DATA PROCESSING METHOD, DATA PROCESSOR AND APPARATUS INCLUDING A DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/577937 | INTEGRATED CIRCUIT DESIGN TOOL APPARATUS AND METHOD OF DESIGNING AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/578276 | DETECTOR AND METHOD FOR DETECTING AN OSCILLATORY SIGNAL AMONG NOISE |
| FREESCALE SEMICONDUCTOR, INC. | 13/580583 | INTEGRATED CIRCUIT DEVICE COMPRISING CLOCK GATING CIRCUITRY, ELECTRONIC DEVICE AND METHOD FOR DYNAMICALLY CONFIGURING CLOCK GATING |
| FREESCALE SEMICONDUCTOR, INC. | 13/582524 | TOKEN BUCKET MANAGEMENT APPARATUS AND METHOD OF MANAGING A TOKEN BUCKET |
| FREESCALE SEMICONDUCTOR, INC. | 13/582769 | INTEGRATED CIRCUIT DEVICE, SIGNAL PROCESSING SYSTEM, ELECTRONIC DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/588194 | Selective Memory Scrubbing Based on Data Type |
| FREESCALE SEMICONDUCTOR, INC. | 13/588205 | SENSOR PACKAGES AND METHOD OF PACKAGING DIES OF VARIOUS SIZES |
| FREESCALE SEMICONDUCTOR, INC. | 13/588243 | Data Type Dependent Memory Scrubbing |
| FREESCALE SEMICONDUCTOR, INC. | 13/589249 | SPLIT-GATE MEMORY CELLS HAVING SELECT-GATE SIDEWALL METAL SILICIDE REGIONS AND RELATED MANUFACTURING METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 13/589580 | RANDOM TIMESLOT CONTROLLER FOR ENABLING BUILT-IN SELF TEST MODULE |
| FREESCALE SEMICONDUCTOR, INC. | 13/590411 | BIPOLAR TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/590995 | SEMICONDUCTOR DEVICE WITH HCI PROTECTION REGION |
| FREESCALE SEMICONDUCTOR, INC. | 13/591924 | STACKED MICROELECTRONIC PACKAGES HAVING SIDEWALL CONDUCTORS AND METHODS FOR THE FABRICATION THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/591969 | STACKED MICROELECTRONIC PACKAGES HAVING PATTERENED SIDEWALL CONDUCTORS AND METHODS FOR THE FABRICATION THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/591990 | STACKED MICROELECTRONIC PACKAGES HAVING SIDEWALL CONDUCTORS AND METHODS FOR THE FABRICATION THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/592764 | Sensor Packages and Method of Packaging Dies of Differing Sizes |
| FREESCALE SEMICONDUCTOR, INC. | 13/593677 | LOW DROPOUT VOLTAGE REGULATOR WITH A FLOATING VOLTAGE REFERENCE |
| FREESCALE SEMICONDUCTOR, INC. | 13/594732 | Copper Ball Bond Features and Structure |
| FREESCALE SEMICONDUCTOR, INC. | 13/595282 | ADAPTIVE ERROR CORRECTION FOR NON-VOLATILE MEMORIES |
| FREESCALE SEMICONDUCTOR, INC. | 13/596112 | LOW POWER, HIGH RESOLUTION TIMING GENERATOR FOR ULTRA-WIDE BANDWIDTH COMMUNICATION SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 13/596337 | DEVICE MATCHING TOOL AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/596764 | NON-VOLATILE MEMORY (NVM) THAT USES SOFT PROGRAMMING |

| FREESCALE SEMICONDUCTOR, INC. | 13/596802 | Thermally Enhanced Electronic Component Packages with Through Mold Vias |
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| FREESCALE SEMICONDUCTOR, INC. | 13/596881 | METHOD AND APPARATUS FOR FILTERING TRACE INFORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/596886 | METHOD AND APPARATUS FOR FILTERING TRACE INFORMATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/597824 | Sensor Packaging Method and Sensor Packages |
| FREESCALE SEMICONDUCTOR, INC. | 13/598240 | DATA PROCESSOR DEVICE FOR HANDLING A WATCHPOINT AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/598763 | PRESSURE SENSOR WITH DIFFERENTIAL CAPACITIVE OUTPUT |
| FREESCALE SEMICONDUCTOR, INC. | 13/599244 | ESD PROTECTION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/599388 | IDENTIFICATION MECHANISM FOR SEMICONDUCTOR DEVICE DIE |
| FREESCALE SEMICONDUCTOR, INC. | 13/600364 | HEAT SPREADER FOR USE WITHIN A PACKAGED SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/600648 | LEADFRAMES, AIR-CAVITY PACKAGES, AND ELECTRONIC DEVICES WITH OFFSET VENT HOLES, AND METHODS OF THEIR MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 13/601746 | SEMICONDUCTOR DEVICE STRUCTURES AND METHODS FOR COPPER BOND PADS |
| FREESCALE SEMICONDUCTOR, INC. | 13/601831 | ZENER DIODE DEVICE AND FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/601973 | VIRTUALIZED LOCAL STORAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/601987 | SECURE PROVISIONING IN AN UNTRUSTED ENVIRONMENT |
| FREESCALE SEMICONDUCTOR, INC. | 13/601993 | CIRCUIT FOR SECURE PROVISIONING IN AN UNTRUSTED ENVIRONMENT |
| FREESCALE SEMICONDUCTOR, INC. | 13/602199 | SYSTEM FOR COMPENSATING FOR VARIATIONS IN CLOCK SIGNAL FREQUENCY |
| FREESCALE SEMICONDUCTOR, INC. | 13/603402 | Automatic Verification of Dependency |
| FREESCALE SEMICONDUCTOR, INC. | 13/603653 | TRACE MESSAGING DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/603801 | GaN Dual Field Plate Device with Single Field Plate Metal |
| FREESCALE SEMICONDUCTOR, INC. | 13/604639 | PROCESSOR WITH PROGRAMMABLE VIRTUAL PORTS |
| FREESCALE SEMICONDUCTOR, INC. | 13/604646 | TOUCH PAD CAPACITIVE SENSOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/605214 | SEMICONDUCTOR DEVICE WITH DIAGONAL CONDUCTION PATH |
| FREESCALE SEMICONDUCTOR, INC. | 13/605357 | TUNABLE SCHOTTKY DIODE |
| FREESCALE SEMICONDUCTOR, INC. | 13/605662 | BANDGAP REFERENCE CIRCUIT WITH STARTUP CIRCUIT AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/605984 | MASTER SLAVE FLIP-FLOP WITH LOW POWER CONSUMPTION |
| FREESCALE SEMICONDUCTOR, INC. | 13/605985 | VOLTAGE LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | 13/605987 | VOLTAGE LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | 13/605990 | LEAD FRAME FOR ASSEMBLING SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/606438 | SEMICONDUCTOR DEVICE AND RELATED FABRICATION METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 13/606797 | SEMICONDUCTOR DEVICE AND RELATED FABRICATION METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 13/606858 | Reducing Leakage in Standard Cells |
| FREESCALE SEMICONDUCTOR, INC. | 13/606980 | Assertion-Based Design Partitioning |
| FREESCALE SEMICONDUCTOR, INC. | 13/607730 | OSCILLATOR CIRCUIT FOR GENERATING CLOCK SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 13/607731 | SEMICONDUCTOR DEVICE AND METHOD OF ASSEMBLING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 13/607732 | MICROWAVE ADAPTORS AND RELATED OSCILLATOR SYSTEMS |
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| FREESCALE SEMICONDUCTOR, INC. | 13/607734 | TRIMMING CIRCUIT FOR CLOCK SOURCE |
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| FREESCALE SEMICONDUCTOR, INC. | 13/607735 | POWER ADAPTER AND ELECTRICAL CONNECTOR THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/607736 | SYSTEM ON CHIP AND CONTROL MODULE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/607810 | TIMING CONTROL IN SYNCHRONOUS MEMORY DATA TRANSFER |
| FREESCALE SEMICONDUCTOR, INC. | 13/607812 | OSCILLATOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/609281 | POWER MOSFET STRUCTURE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 13/609282 | COMPARATOR AND RELAXATION OSCILLATOR EMPLOYING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 13/609283 | RECONFIGURABLE INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/610488 | MICROELECTRONIC PACKAGES HAVING TRENCH VIAS AND METHODS FOR THE MANUFACTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/610901 | POWER MOSFET CURRENT SENSE STRUCTURE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 13/611076 | TECHNIQUES FOR REDUCING INDUCTANCE IN THROUGH-DIE VIAS OF AN ELECTRONIC ASSEMBLY |
| FREESCALE SEMICONDUCTOR, INC. | 13/611793 | SEMICONDUCTOR DEVICES WITH IMPEDANCE MATCHING CIRCUITS, AND METHODS OF MANUFACTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/612231 | TRENCH SEMICONDUCTOR DEVICES WITH EDGE TERMINATION STRUCTURES, AND METHODS OF MANUFACTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/613614 | TRANSISTORS WITH IMMERSED CONTACTS |
| FREESCALE SEMICONDUCTOR, INC. | 13/613979 | HIGH POWER SEMICONDUCTOR PACKAGE SUBSYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 13/614448 | Method and System for Calibrating an Inertial Sensor |
| FREESCALE SEMICONDUCTOR, INC. | 13/614722 | LDMOS WITH ENHANCED SAFE OPERATING AREA (SOA) AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/614850 | QUIESCENT CURRENT DETERMINATION USING IN-PACKAGE VOLTAGE MEASUREMENTS |
| FREESCALE SEMICONDUCTOR, INC. | 13/616169 | NON-VOLATILE MEMORY (NVM) WITH ADAPTIVE WRITE OPERATIONS |
| FREESCALE SEMICONDUCTOR, INC. | 13/616206 | NVM WITH CHARGE PUMP AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/616922 | SYSTEMS AND METHODS FOR CODE PROTECTION IN NON-VOLATILE MEMORY SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 13/617851 | Thermally Enhanced Package with Lid Heat Spreader |
| FREESCALE SEMICONDUCTOR, INC. | 13/618185 | Matrix Lid Heatspreader for Flip Chip Package |
| FREESCALE SEMICONDUCTOR, INC. | 13/624232 | METHOD AND APPARATUS FOR MULTI-CHIP STRUCTURE SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/627327 | VOLTAGE TRANSLATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/627333 | PHASE LOCKED LOOP WITH BURN-IN MODE |
| FREESCALE SEMICONDUCTOR, INC. | 13/628814 | THERMAL SENSOR SYSTEM AND METHOD BASED ON CURRENT RATIO |
| FREESCALE SEMICONDUCTOR, INC. | 13/628939 | THERMAL SENSOR SYSTEM AND METHOD BASED ON CURRENT RATIO |
| FREESCALE SEMICONDUCTOR, INC. | 13/629643 | PHASE LOCKED LOOP WITH POWER SUPPLY CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 13/630346 | Techniques for Utilizing Transaction Lookaside Buffer Entry Numbers to Improve Processor Performance |
| FREESCALE SEMICONDUCTOR, INC. | 13/630996 | METHOD AND APPARATUS TO IMPROVE RELIABILITY OF VIAS |
| FREESCALE SEMICONDUCTOR, INC. | 13/632549 | Method and system for automatically controlling the insertion of control word in CPRI daisy chain configuration |
| FREESCALE SEMICONDUCTOR, INC. | 13/632616 | Multiply and accumulate feedback |
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SPLIT GATE FLASH CELL

13/633124

FREESCALE SEMICONDUCTOR, INC.

| FREESCALE SEMICONDUCTOR, INC. | 13/634716 | POWER GATING CONTROL MODULE, INTEGRATED CIRCUIT DEVICE, SIGNAL PROCESSING SYSTEM, ELECTRONIC DEVICE, AND METHOD THEREFOR |
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| FREESCALE SEMICONDUCTOR, INC. | 13/634726 | INTEGRATED CIRCUIT DEVICE, CALIBRATION MODULE, AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/634730 | ELECTRONIC CIRCUIT AND METHOD FOR STATE RETENTION POWER GATING |
| FREESCALE SEMICONDUCTOR, INC. | 13/634755 | MEMORY UNIT, INFORMATION PROCESSING DEVICE, AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 13/634760 | METHOD FOR PROVIDING DATA PROTECTION FOR DATA STORED WITHIN A MEMORY ELEMENT AND INTEGRATED CIRCUIT DEVICE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/634992 | INTEGRATED CIRCUIT, ELECTRONIC DEVICE AND METHOD FOR CONFIGURING A SIGNAL PATH FOR A TIMING SENSITIVE SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 13/634999 | INFORMATION PROCESSING DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 13/635006 | INTEGRATED CIRCUIT DEVICE AND METHOD FOR GENERATING A TUNING SIGNAL FOR CALIBRATING A VOLTAGE CONTROLLED OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/635166 | VOLTAGE LEVEL SHIFTER, DECOUPLER FOR A VOLTAGE LEVEL SHIFTER, AND VOLTAGE SHIFTING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 13/635186 | VOLTAGE LEVEL SHIFTER HAVING A FIRST OPERATING MODE AND A SECOND OPERATING MODE |
| FREESCALE SEMICONDUCTOR, INC. | 13/635205 | MULTI-CHANNEL SNIFFER SYSTEM AND METHOD FOR MULTI-CHANNEL SNIFFER SYNCHRONIZATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/635214 | AUDIO COMMUNICATION DEVICE, METHOD FOR OUTPUTTING AN AUDIO SIGNAL, AND COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 13/643358 | INTEGRATED CIRCUIT DEVICE, SIGNAL PROCESSING SYSTEM AND METHOD FOR MANAGING POWER RESOURCES OF A SIGNAL PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 13/645050 | OPPORTUNISTIC CACHE REPLACEMENT POLICY |
| FREESCALE SEMICONDUCTOR, INC. | 13/647951 | LATENT SLOW BIT DETECTION FOR NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 13/648501 | Compiler Optimized Safety Mechanism |
| FREESCALE SEMICONDUCTOR, INC. | 13/649461 | Method and System for Low Power Transmission and Data Alignment |
| FREESCALE SEMICONDUCTOR, INC. | 13/650138 | TIMING EVENT GENERATION CIRCUIT FOR MOBILE COMMUNICATION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/650141 | PROCESSOR SWITCHABLE BETWEEN TEST AND DEBUG MODES |
| FREESCALE SEMICONDUCTOR, INC. | 13/650872 | CHIP-LEVEL HUMIDITY PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | 13/651995 | ENCAPSULANT FOR A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/653155 | ELECTRONIC CIRCUITS WITH VARIABLE ATTENUATORS AND METHODS OF THEIR OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/656073 | FLEXIBLE CONTROL MECHANISM FOR STORE GATHERING IN A WRITE BUFFER |
| FREESCALE SEMICONDUCTOR, INC. | 13/656103 | Resurf High Voltage Diode |
| FREESCALE SEMICONDUCTOR, INC. | 13/656122 | High Voltage Diode |
| FREESCALE SEMICONDUCTOR, INC. | 13/656253 | DYNAMICALLY BIASED OUTPUT STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 13/656551 | AMPLIFIER CALIBRATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/657250 | PACKAGING FOR SEMICONDUCTOR SENSOR DEVICES AND METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 13/660243 | A PACKAGED INTEGRATED CIRCUIT HAVING LARGE SOLDER PADS AND |

METHOD FOR FORMING

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| FREESCALE SEMICONDUCTOR, INC. | 13/661131 | VIA PLACEMENT AND ELECTRONIC CIRCUIT DESIGN PROCESSING METHOD AND ELECTRONIC CIRCUIT DESIGN UTILIZING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 13/661157 | METHOD OF MAKING A LOGIC TRANSISTOR AND A NON-VOLATILE MEMORY (NVM) CELL |
| FREESCALE SEMICONDUCTOR, INC. | 13/661377 | METHODS AND STRUCTURES FOR CAPPING A STRUCTURE WITH A PROTECTIVE COATING |
| FREESCALE SEMICONDUCTOR, INC. | 13/661861 | SRAM WITH IMPROVED WRITE OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/663462 | SEMICONDUCTOR DEVICE WITH THERMAL DISSIPATION LEAD FRAME |
| FREESCALE SEMICONDUCTOR, INC. | 13/663636 | CONTROL GATE WORD LINE DRIVER CIRCUIT FOR MULTIGATE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 13/663991 | PRODUCTION-TEST DIE TEMPERATURE MEASUREMENT |
| FREESCALE SEMICONDUCTOR, INC. | 13/663998 | SENSOR SINGLE TRACK TRIM USING STATIONARY HARDWARE AND FIELDS |
| FREESCALE SEMICONDUCTOR, INC. | 13/664565 | SYSTEM AND METHOD FOR ASSIGNING A MESSAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/665256 | SYSTEMS AND METHODS FOR DETERMINING AGING DAMAGE FOR SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 13/665518 | GATE DRIVER WITH DESATURATION DETECTION AND ACTIVE CLAMPING |
| FREESCALE SEMICONDUCTOR, INC. | 13/665665 | LDMOS Device with Minority Carrier Shunt Region |
| FREESCALE SEMICONDUCTOR, INC. | 13/665840 | METHODS AND INTEGRATED CIRCUIT PACKAGE FOR SENSING FLUID PROPERTIES |
| FREESCALE SEMICONDUCTOR, INC. | 13/665864 | METHOD AND APPARATUS FOR A TUNABLE DRIVER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/665902 | LCD DRIVER VERIFICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 13/665903 | RELAXATION OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/665906 | MEMORY CONTROLLER FOR MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/665917 | MEMORY DEVICE REDUNDANCY MANAGEMENT SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 13/665921 | SYSTEM FOR GENERATING GATED CLOCK SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 13/666289 | Vector NCO and Twiddle Factor Generator |
| FREESCALE SEMICONDUCTOR, INC. | 13/668496 | DELAY COMPENSATED CONTINUOUS TIME SIGMA DELTA ANALOG-TO- DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 13/668951 | HARDWARE-BASED MEMORY INITIALIZATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/671503 | SEMICONDUCTOR DEVICE AND DRIVER CIRCUIT WITH AN ACTIVE DEVICE AND ISOLATION STRUCTURE INTERCONNECTED THROUGH A DIODE CIRCUIT, AND METHOD OF MANUFACTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/671506 | SEMICONDUCTOR DEVICE AND DRIVER CIRCUIT WITH AN ACTIVE DEVICE AND ISOLATION STRUCTURE INTERCONNECTED THROUGH A RESISTOR CIRCUIT, AND METHOD OF MANUFACTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/671623 | ZENER TRIGGERED BIPOLAR BASED ESD PROTECTION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/671951 | OFFSET ERROR AUTOMATIC CALIBRATION INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/673212 | WETTABLE LEAD ENDS ON A FLAT-PACK NO-LEAD MICROELECTRONIC PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/674367 | PROGRAMMING A NON-VOLATILE MEMORY (NVM) SYSTEM HAVING ERROR CORRECTION CODE (ECC) |
| FREESCALE SEMICONDUCTOR, INC. | 13/675008 | TRACE ROUTING WITHIN A SEMICONDUCTOR PACKAGE SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | 13/677800 | INTEGRATED CIRCUIT WITH DEGRADATION MONITORING |
| FREESCALE SEMICONDUCTOR, INC. | 13/678117 | TEMPERATURE DEPENDENT TIMER CIRCUIT |
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| FREESCALE SEMICONDUCTOR, INC. | 13/678789 | TABLE MODEL CIRCUIT SIMULATION ACCELERATION USING MODEL CACHING |
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| FREESCALE SEMICONDUCTOR, INC. | 13/679481 | DYNAMIC READ SCHEME FOR HIGH RELIABILITY HIGH PERFORMANCE FLASH MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 13/679515 | NON-VOLATILE MEMORY ROBUST START-UP USING ANALOG-TO-DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | 13/681401 | SEMICONDUCTOR WAFER DICING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 13/681406 | SYSTEM AND METHOD FOR PERFORMING SCAN TEST |
| FREESCALE SEMICONDUCTOR, INC. | 13/681437 | SEMICONDUCTOR DEVICE PACKAGE WITH CAP ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 13/681956 | Low-Power Voltage Tamper Detection |
| FREESCALE SEMICONDUCTOR, INC. | 13/682350 | FLEXIBLE CONTROL MECHANISM FOR STORE GATHERING IN A WRITE BUFFER |
| FREESCALE SEMICONDUCTOR, INC. | 13/682367 | FLEXIBLE CONTROL MECHANISM FOR STORE GATHERING IN A WRITE BUFFER |
| FREESCALE SEMICONDUCTOR, INC. | 13/682558 | INTEGRATED CIRCUIT ELECTRICAL PROTECTION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/682604 | TRIGGER CIRCUIT AND METHOD FOR IMPROVED TRANSIENT IMMUNITY |
| FREESCALE SEMICONDUCTOR, INC. | 13/682749 | LOW POWER SCAN FLIP-FLOP CELL |
| FREESCALE SEMICONDUCTOR, INC. | 13/682751 | METHOD AND SYSTEM FOR DEBLOCK FILTERING CODED MACROBLOCKS |
| FREESCALE SEMICONDUCTOR, INC. | 13/682755 | SYSTEM FOR DATA TRANSFER BETWEEN ASYNCHRONOUS CLOCK DOMAINS |
| FREESCALE SEMICONDUCTOR, INC. | 13/684840 | TEST STRUCTURE ACTIVATED BY PROBE NEEDLE |
| FREESCALE SEMICONDUCTOR, INC. | 13/686102 | ELECTRONIC DEVICES WITH CAVITY-TYPE, PERMEABLE MATERIAL FILLED PACKAGES, AND METHODS OF THEIR MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | 13/686889 | Voltage Ramp-Up Protection |
| FREESCALE SEMICONDUCTOR, INC. | 13/686901 | METHOD AND INTEGRATED CIRCUIT THAT PROVIDES TRACKING BETWEEN MULTIPLE REGULATED VOLTAGES |
| FREESCALE SEMICONDUCTOR, INC. | 13/687299 | Inertial Sensor and Method of Levitation Effect Compensation |
| FREESCALE SEMICONDUCTOR, INC. | 13/687424 | Spring for Microelectromechanical Systems (MEMS) Device |
| FREESCALE SEMICONDUCTOR, INC. | 13/688820 | ELECTRONIC DEVICES WITH EMBEDDED DIE INTERCONNECT STRUCTURES, AND METHODS OF MANUFACTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/689034 | SEMICONDUCTOR DEVICE PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/689037 | SYSTEMS AND METHODS FOR DELIVERING POWER IN RESPONSE TO A CONNECTION EVENT |
| FREESCALE SEMICONDUCTOR, INC. | 13/689043 | SYSTEMS AND METHODS FOR CONTROLLING POWER IN SEMICONDUCTOR CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 13/689274 | METHODS FOR THE FABRICATION OF SEMICONDUCTOR DEVICES INCLUDING SUB-ISOLATION BURIED LAYERS |
| FREESCALE SEMICONDUCTOR, INC. | 13/689331 | MEMORY COLUMN DROWSY CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 13/689845 | SEMICONDUCTOR DEVICE PACKAGES PROVIDING ENHANCED EXPOSED TOE FILLETS |
| FREESCALE SEMICONDUCTOR, INC. | 13/690046 | OVER VOLTAGE PROTECTION FOR A THIN OXIDE LOAD CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/690336 | AC COUPLED LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | 13/690888 | RANDOM ACCESS OF A CACHE PORTION USING AN ACCESS MODULE |
| FREESCALE SEMICONDUCTOR, INC. | 13/695670 | INTEGRATED CIRCUIT, ELECTRONIC DEVICE AND ESD PROTECTION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/698122 | POWER SWITCHING APPARATUS AND METHOD FOR IMPROVING CURRENT |

SENSE ACCURACY

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| FREESCALE SEMICONDUCTOR, INC. | 13/701303 | INTEGRATED CIRCUIT DEVICE, ELECTRONIC DEVICE AND METHOD FOR DETECTING TIMING VIOLATIONS WITHIN A CLOCK |
| FREESCALE SEMICONDUCTOR, INC. | 13/709049 | EMBEDDED LOGIC ANALYZER |
| FREESCALE SEMICONDUCTOR, INC. | 13/709103 | Reducing the Power Consumption of Memory Devices |
| FREESCALE SEMICONDUCTOR, INC. | 13/712051 | INTEGRATED CIRCUITS INCLUDING INTEGRATED PASSIVE DEVICES AND METHODS OF MANUFACTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/712070 | SYSTEMS WITH ADJUSTABLE SAMPLING PARAMETERS AND METHODS OF THEIR OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/714415 | BAND GAP REFERENCE VOLTAGE GENERATOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/716193 | SYSTEM AND METHOD FOR CLEANING BOND WIRE |
| FREESCALE SEMICONDUCTOR, INC. | 13/716194 | RAIL TO RAIL DIFFERENTIAL BUFFER INPUT STAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/717646 | MULTI-VOLTAGE DOMAIN CIRCUIT DESIGN VERIFICATION METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 13/718081 | SEMICONDUCTOR PACKAGE SIGNAL ROUTING USING CONDUCTIVE VIAS |
| FREESCALE SEMICONDUCTOR, INC. | 13/718598 | REDUCING MEMS STICTION BY INTRODUCTION OF A CARBON BARRIER |
| FREESCALE SEMICONDUCTOR, INC. | 13/718614 | REDUCING MEMS STICTION BY DEPOSITION OF NANOCLUSTERS |
| FREESCALE SEMICONDUCTOR, INC. | 13/723207 | SYSTEM FOR OPTIMIZING NUMBER OF DIES PRODUCED ON A WAFER |
| FREESCALE SEMICONDUCTOR, INC. | 13/731242 | METHODS OF FORMING 3-D CIRCUITS WITH INTEGRATED PASSIVE DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 13/732533 | SUPPRESSION OF REDUNDANT CACHE STATUS UPDATES |
| FREESCALE SEMICONDUCTOR, INC. | 13/735050 | SYSTEM FOR MANAGING UPLINK QUALITY OF SERVICE (Q0S) IN CELLULAR NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | 13/735052 | BOSE-CHAUDHURI-HOCQUENGHEM (BCH) DECODER |
| FREESCALE SEMICONDUCTOR, INC. | 13/735053 | CONFIGURABLE CIRCUIT AND MESH STRUCTURE FOR INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/735054 | INTEGRATED CIRCUIT DESIGN VERIFICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 13/736310 | Memory Having Improved Reliability for Certain Data Types |
| FREESCALE SEMICONDUCTOR, INC. | 13/736322 | Memory Using Voltage to Improve Reliability for Certain Data Types |
| FREESCALE SEMICONDUCTOR, INC. | 13/736440 | Schmitt Trigger Circuit with Near Rail-to-Rail Hysteresis |
| FREESCALE SEMICONDUCTOR, INC. | 13/739732 | METHOD AND APPARATUS FOR TESTING RANDOM NUMBER GENERATOR TESTER |
| FREESCALE SEMICONDUCTOR, INC. | 13/739749 | BUS SIGNAL ENCODED WITH DATA AND CLOCK SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | 13/740404 | METHODS AND SYSTEMS FOR PUSHING DIRTY LINEFILL BUFFER CONTENTS TO EXTERNAL BUS UPON LINEFILL REQUEST FAILURES |
| FREESCALE SEMICONDUCTOR, INC. | 13/740823 | TRANSMISSION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 13/740862 | MULTIPORT MEMORY WITH MATCHING ADDRESS AND DATA LINE CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 13/740868 | MULTIPORT MEMORY WITH MATCHING ADDRESS CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 13/741743 | MICROELECTRONIC ASSEMBLY HAVING A HEAT SPREADER FOR A PLURALITY OF DIE |
| FREESCALE SEMICONDUCTOR, INC. | 13/742532 | DIGITAL TO ANALOG CONVERTER WITH CURRENT STEERING SOURCE FOR REDUCED GLITCH ENERGY ERROR |
| FREESCALE SEMICONDUCTOR, INC. | 13/742540 | Reducing Output Voltage Ripple of Power Supplies |
| FREESCALE SEMICONDUCTOR, INC. | 13/743323 | CAPACITOR CHARGING CIRCUIT WITH LOW SUB-THRESHOLD TRANSISTOR LEAKAGE CURRENT |
| FREESCALE SEMICONDUCTOR, INC. | 13/743324 | WELL-BIASING CIRCUIT FOR INTEGRATED CIRCUIT |
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| FREESCALE SEMICONDUCTOR, INC. | 13/745425 | DMA-ASSISTED IRREGULAR SAMPLING SEQUENCES |
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| FREESCALE SEMICONDUCTOR, INC. | 13/746840 | SYSTEMS AND METHODS FOR REDUCED COUPLING BETWEEN DIGITAL SIGNAL LINES |
| FREESCALE SEMICONDUCTOR, INC. | 13/746841 | SYSTEMS AND METHODS FOR ADAPTIVE SOFT PROGRAMMING FOR NON-VOLATILE MEMORY USING TEMPERATURE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/746874 | SEMICONDUCTOR DEVICES AND METHODS FOR CONFIGURING CONDUCTIVE ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | 13/746891 | Vector Comparator System for Finding a Peak Number |
| FREESCALE SEMICONDUCTOR, INC. | 13/747088 | FLASH MEMORY WITH BIAS VOLTAGE FOR WORD LINE/ROW DRIVER |
| FREESCALE SEMICONDUCTOR, INC. | 13/747094 | DIE EDGE SEALING STRUCTURES AND RELATED FABRICATION METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 13/747504 | DYNAMIC DETECTION METHOD FOR LATENT SLOW-TO-ERASE BIT FOR HIGH PERFORMANCE AND HIGH RELIABILITY FLASH MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 13/747608 | MANUFACTURING METHODS FOR LATERALLY DIFFUSED METAL OXIDE SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 13/748076 | Semiconductor Device with Enhanced 3D RESURF |
| FREESCALE SEMICONDUCTOR, INC. | 13/748381 | SYSTEMS AND METHOD FOR GYROSCOPE CALIBRATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/748598 | POWER SUPPLY FOR INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/748796 | SIGMA-DELTA MODULATOR WITH TRIMMED REFERENCE VOLTAGE FOR QUANTIZER |
| FREESCALE SEMICONDUCTOR, INC. | 13/748798 | METHODS AND STRUCTURES FOR DYNAMICALLY CALIBRATING REFERENCE VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/748808 | METHOD OF MAKING A NON-VOLATILE MEMORY (NVM) CELL STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 13/749542 | VARIABLE DELAY AND SETUP TIME FLIP-FLOP |
| FREESCALE SEMICONDUCTOR, INC. | 13/750057 | AREA-EFFICIENT HIGH VOLTAGE BIPOLAR-BASED ESD PROTECTION TARGETING NARROW DESIGN WINDOWS |
| FREESCALE SEMICONDUCTOR, INC. | 13/750419 | INTEGRATED CIRCUIT HAVING VARYING SUBSTRATE DEPTH AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 13/750936 | Layout-Optimized Random Mask Distribution System and Method |
| FREESCALE SEMICONDUCTOR, INC. | 13/750956 | Cryptographic Key Derivation Device and Method Therefor |
| FREESCALE SEMICONDUCTOR, INC. | 13/751318 | ELECTRONIC DEVICE MODULE WITH INTEGRATED ANTENNA STRUCTURE, AND RELATED MANUFACTURING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 13/751548 | PROGRAMMING A SPLIT GATE BIT CELL |
| FREESCALE SEMICONDUCTOR, INC. | 13/753034 | MICROELECTROMECHANICAL SYSTEM DEVICES HAVING CRACK RESISTANT MEMBRANE STRUCTURES AND METHODS FOR THE FABRICATION THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/753047 | NON-VOLATILE MEMORY CELLS HAVING CARBON IMPURITIES AND RELATED MANUFACTURING METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 13/753544 | RELAXATION OSCILLATOR WITH SELF-BIASED COMPARATOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/754086 | SEMICONDUCITIVE CATECHOL GROUP ENCAPSULANT ADHESION PROMOTER FOR A PACKAGED ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/754873 | Amplitude Loop Control for Oscillators |
| FREESCALE SEMICONDUCTOR, INC. | 13/755606 | DYNAMIC HEALING OF NON-VOLATILE MEMORY CELLS |
| FREESCALE SEMICONDUCTOR, INC. | 13/755904 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE ASSEMBLY HAVING A HEAT SPREADER |
| FREESCALE SEMICONDUCTOR, INC. | 13/756248 | NONVOLATILE MEMORY BITCELL |
| FREESCALE SEMICONDUCTOR, INC. | 13/758263 | LEAD FRAME ARRAY PACKAGE WITH FLIP CHIP DIE ATTACH |
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Write Transaction Interpretation for Interrupt Assertion

13/758268

FREESCALE SEMICONDUCTOR, INC.

| FREESCALE SEMICONDUCTOR, INC. | 13/759054 | MEMORY ERROR MANAGEMENT SYSTEM |
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| FREESCALE SEMICONDUCTOR, INC. | 13/759056 | VOLTAGE SCALE-DOWN CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/759241 | ELECTROSTATIC DISCHARGE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/760109 | SYSTEM AND METHOD FOR MAINTAINING PACKET ORDER IN AN ORDERED DATA STREAM |
| FREESCALE SEMICONDUCTOR, INC. | 13/760465 | STICTION RESISTANT MEMES DEVICE AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/760882 | METHODS OF FABRICATING BIPOLAR TRANSISTORS WITH IMPROVED GAIN |
| FREESCALE SEMICONDUCTOR, INC. | 13/762344 | SYSTEM AND METHOD FOR SCAN CHAIN RE-ORDERING |
| FREESCALE SEMICONDUCTOR, INC. | 13/763036 | Embedded NVM in a HKMG Process |
| FREESCALE SEMICONDUCTOR, INC. | 13/764246 | PRESSURE LEVEL ADJUSTMENT IN A CAVITY OF A SEMICONDUCTOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | 13/764398 | METHODS RELATING TO THE FABRICATION OF DEVICES HAVING CONDUCTIVE SUBSTRATE VIAS WITH CATCH-PAD ETCH-STOPS |
| FREESCALE SEMICONDUCTOR, INC. | 13/764523 | ESD Protection with Integrated LDMOS Triggering Junction |
| FREESCALE SEMICONDUCTOR, INC. | 13/764946 | FINE GRAIN VOLTAGE SCALING OF BACK BIASING |
| FREESCALE SEMICONDUCTOR, INC. | 13/764958 | METHODS AND STRUCTURES FOR REDUCING STRESS ON DIE ASSEMBLY |
| FREESCALE SEMICONDUCTOR, INC. | 13/766445 | METHODS RELATING TO INTERMETALLIC TESTING OF BOND INTEGRITY BETWEEN BOND PADS AND COPPER-CONTAINING BOND WIRES |
| FREESCALE SEMICONDUCTOR, INC. | 13/766771 | SOLAR POWERED IC CHIP |
| FREESCALE SEMICONDUCTOR, INC. | 13/767064 | Timing Margins for On-chip Variations from Sensitivity Data |
| FREESCALE SEMICONDUCTOR, INC. | 13/770070 | CIRCUIT AND METHOD FOR VOLTAGE EQUALIZATION IN LARGE BATTERIES |
| FREESCALE SEMICONDUCTOR, INC. | 13/770170 | CIRCUIT AND METHOD FOR BATTERY EQUALIZATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/770224 | SPRING SYSTEM FOR MEMS DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/770548 | METHODS FOR FORMING ELECTROSTATIC DISCHARGE PROTECTION CLAMPS WITH INCREASED CURRENT CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 13/771025 | LEVEL SHIFTER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/773432 | SEMICONDUCTOR DEVICE AND RELATED FABRICATION METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 13/773434 | Low Power Quantizer For Analog To Digital Converter |
| FREESCALE SEMICONDUCTOR, INC. | 13/773578 | SEMICONDUCTOR PACKAGES WITH LOW STAND-OFF INTERCONNECTIONS BETWEEN CHIPS |
| FREESCALE SEMICONDUCTOR, INC. | 13/773594 | SEMICONDUCTOR PACKAGE WITH INNER AND OUTER LEADS |
| FREESCALE SEMICONDUCTOR, INC. | 13/773603 | SEMICONDUCTOR GRID ARRAY PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/774340 | Transition Control For a Hybrid Switched-Mode Power Supply (SMPS) |
| FREESCALE SEMICONDUCTOR, INC. | 13/774486 | Thin Beam Deposited Fuse |
| FREESCALE SEMICONDUCTOR, INC. | 13/775313 | METHODS AND SYSTEMS FOR ADDRESS MAPPING BETWEEN HOST AND EXPANSION DEVICES WITHIN SYSTEM-IN-PACKAGE (SiP) SOLUTIONS |
| FREESCALE SEMICONDUCTOR, INC. | 13/775330 | METHODS AND SYSTEMS FOR INTERCONNECTING HOST AND EXPANSION DEVICES WITHIN SYSTEM-IN-PACKAGE (SiP) SOLUTIONS |
| FREESCALE SEMICONDUCTOR, INC. | 13/776052 | ROBUST SECTOR ID SCHEME FOR TRACKING DEAD SECTORS TO AUTOMATE SEARCH AND COPYDOWN |
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13/777715 METHOD FOR BONDING SEMICONDUCTOR DEVICES

FREESCALE SEMICONDUCTOR, INC.

| FREESCALE SEMICONDUCTOR, INC. | 13/777858 | MISHFET and Schottky Device Integration |
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| FREESCALE SEMICONDUCTOR, INC. | 13/778546 | SCAN DIAGNOSIS ANALYSIS USING CALLOUT CLUSTERING |
| FREESCALE SEMICONDUCTOR, INC. | 13/779751 | DATA ACQUISITION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 13/779859 | SPLIT GATE NON-VOLATILE MEMORY (NVM) CELL AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/780101 | SYNCHRONOUS MULTIPLE PORT MEMORY WITH ASYNCHRONOUS PORTS |
| FREESCALE SEMICONDUCTOR, INC. | 13/780574 | NON-VOLATILE MEMORY (NVM) AND LOGIC INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/780591 | NON-VOLATILE MEMORY (NVM) AND LOGIC INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/780969 | SENSE AMPLIFIER VOLTAGE REGULATOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/781391 | MICROELECTROMECHANICAL SYSTEM DEVICES HAVING THROUGH SUBSTRATE VIAS AND METHODS FOR THE FABRICATION THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/781722 | RESURF SEMICONDUCTOR DEVICE CHARGE BALANCING |
| FREESCALE SEMICONDUCTOR, INC. | 13/781727 | METHODS OF MAKING LOGIC TRANSISTORS AND NON-VOLATILE MEMORY CELLS |
| FREESCALE SEMICONDUCTOR, INC. | 13/781732 | PACKAGED SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/785482 | SYSTEM FOR REDUCING ELECTROMAGNETIC INDUCTION INTERFERENCE |
| FREESCALE SEMICONDUCTOR, INC. | 13/787290 | SYSTEMS AND METHODS FOR INDICATING THAT AN INTERFACE IS BEING TOUCHED |
| FREESCALE SEMICONDUCTOR, INC. | 13/787799 | Temperature-Based Adaptive Erase or Program Parallelism |
| FREESCALE SEMICONDUCTOR, INC. | 13/788046 | Prioritized Design for Manufacturing Virtualization with Design Rule Checking Filtering |
| FREESCALE SEMICONDUCTOR, INC. | 13/788344 | Test Control Point Insertion and X-Bounding for Logic Built-in Self-Test (LBIST) usin Observation |
| FREESCALE SEMICONDUCTOR, INC. | 13/789017 | ROBUST MEMORY START-UP USING CLOCK COUNTER |
| FREESCALE SEMICONDUCTOR, INC. | 13/789340 | SEMICONDUCTOR DIES HAVING SUBSTRATE SHUNTS AND RELATED FABRICATION METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 13/789387 | PROGRAMMABLE DIRECT MEMORY ACCESS CHANNELS |
| FREESCALE SEMICONDUCTOR, INC. | 13/789660 | LEAD FRAME FOR SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/789661 | SYSTEM AND METHOD FOR DYNAMICALLY MIGRATING STASH TRANSACTIONS |
| FREESCALE SEMICONDUCTOR, INC. | 13/790004 | INTEGRATION TECHNIQUE USING THERMAL OXIDE SELECT GATE DIELECTRIC FOR SELECT GATE AND A PARTIAL REPLACEMENT GATE FOR LOGIC |
| FREESCALE SEMICONDUCTOR, INC. | 13/790014 | INTEGRATING FORMATION OF A LOGIC TRANSISTOR AND A NON- VOLATILE MEMORY CELL USING A PARTIAL REPLACEMENT GATE TECHNIQUE |
| FREESCALE SEMICONDUCTOR, INC. | 13/790225 | INTEGRATING FORMATION OF A REPLACEMENT GATE TRANSISTOR AND A NON-VOLATILE MEMORY CELL HAVING THIN FILM STORAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/790627 | Gate Security Feature |
| FREESCALE SEMICONDUCTOR, INC. | 13/790717 | SYSTEM AND METHOD FOR MONITORING A GYROSCOPE |
| FREESCALE SEMICONDUCTOR, INC. | 13/791012 | SYMMETRICAL DATA REPLICATION FOR FAILURE MANAGEMENT IN NON-VOLATILE MEMORY SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 13/791329 | SYSTEM AND METHOD FOR REDUCING OFFSET VARIATION IN MULTIFUNCTION SENSOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 13/791343 | SYSTEM AND METHOD FOR MONITORING AN ACCELEROMETER |
| FREESCALE SEMICONDUCTOR, INC. | 13/792748 | Semiconductor Device with Integrated Electrostatic Discharge (ESD) Clamp |
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| FREESCALE SEMICONDUCTOR, INC. | 13/792876 | Semiconductor Device with Increased Safe Operating Area |
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| FREESCALE SEMICONDUCTOR, INC. | 13/794739 | MULTIPLIER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/794789 | MOLD CHASE |
| FREESCALE SEMICONDUCTOR, INC. | 13/794836 | WIRE BONDING APPARATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 13/794841 | LEAD FRAME FOR SEMICONDUCTOR PACKAGE WITH ENHANCED STRESS RELIEF |
| FREESCALE SEMICONDUCTOR, INC. | 13/795704 | MCU-BASED COMPENSATION AND CALIBRATION FOR MEMS DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 13/795789 | MULTIPORT MEMORY WITH MATCHING ADDRESS CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 13/798052 | BRACE FOR BOND WIRE |
| FREESCALE SEMICONDUCTOR, INC. | 13/798715 | A RESOLUTION PROGRAMMABLE DYNAMIC IR-DROP SENSOR WITH PEAK IR-DROP TRACKING ABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | 13/798902 | ANGULAR RATE SENSOR HAVING MULTIPLE AXIS SENSING CAPABILITY |
| FREESCALE SEMICONDUCTOR, INC. | 13/798980 | SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/799031 | SEMICONDUCTOR DEVICE ASSEMBLY HAVING A HEAT SPREADER |
| FREESCALE SEMICONDUCTOR, INC. | 13/799343 | WIRELESS CHARGING SYSTEMS, DEVICES, AND METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 13/801514 | DEEP TRENCH ISOLATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/801576 | SYSTEM AND METHOD FOR ORDERING PACKET TRANSFERS IN A DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/802006 | NOISE ISOLATION BETWEEN CIRCUIT BLOCKS IN AN INTEGRATED CIRCUIT CHIP |
| FREESCALE SEMICONDUCTOR, INC. | 13/810000 | ELECTRONIC CIRCUIT, SAFETY CRITICAL SYSTEM, AND METHOD FOR PROVIDING A RESET SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 13/810350 | INTEGRATED CIRCUIT DEVICE, DATA STORAGE ARRAY SYSTEM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/810523 | CLOCK CIRCUIT FOR PROVIDING AN ELECTRONIC DEVICE WITH A CLOCK SIGNAL, ELECTRONIC DEVICE WITH A CLOCK CIRCUIT AND METHOD FOR PROVIDING AN ELECTRONIC DEVICE WITH A CLOCK SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | 13/810746 | DISPLAY CONTROLLING UNIT, IMAGE DISPLAYING SYSTEM AND METHOD FOR OUTPUTTING IMAGE DATA |
| FREESCALE SEMICONDUCTOR, INC. | 13/811400 | METHOD FOR OPTIMISING CELL VARIANT SELECTION WITHIN A DESIGN PROCESS FOR AN INTEGRATED CIRCUIT DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/811921 | LATCH CIRCUIT, FLIP-FLOP CIRCUIT AND FREQUENCY DIVIDER |
| FREESCALE SEMICONDUCTOR, INC. | 13/811942 | MULTI-CORE PROCESSOR AND METHOD OF POWER MANAGEMENT OF A MULTI-CORE PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/812168 | APPARATUS AND METHOD FOR REDUCING PROCESSOR LATENCY |
| FREESCALE SEMICONDUCTOR, INC. | 13/812889 | ELECTRONIC CIRCUIT AND METHOD FOR STATE RETENTION POWER GATING |
| FREESCALE SEMICONDUCTOR, INC. | 13/814764 | PUSH-PUSH OSCILLATOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/816595 | OPTIMIZATION METHOD FOR COMPILER, OPTIMIZER FOR A COMPILER AND STORAGE MEDIUM STORING OPTIMIZING CODE |
| FREESCALE SEMICONDUCTOR, INC. | 13/817940 | MEMORY MANAGEMENT UNIT FOR A MICROPROCESSOR SYSTEM, MICROPROCESSOR SYSTEM AND METHOD FOR MANAGING MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 13/818480 | VIDEO PROCESSING SYSTEM AND METHOD FOR PARALLEL PROCESSING OF VIDEO DATA |
| FREESCALE SEMICONDUCTOR, INC. | 13/821070 | METHODS FOR PROCESSING A SEMICONDUCTOR WAFER, A SEMICONDUCTOR WAFER AND A SEMICONDUCTOR DEVICE |

| FREESCALE SEMICONDUCTOR, INC. | 13/824537 | LOW-VOLTAGE EXIT DETECTOR, ERROR DETECTOR, LOW-VOLTAGE SAFE CONTROLLER, BROWN-OUT DETECTION METHOD, AND BROWN-OUT SELF-HEALING METHOD |
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| FREESCALE SEMICONDUCTOR, INC. | 13/824959 | INTEGRATED CIRCUIT DEVICE, WIRELESS COMMUNICATION UNIT AND METHOD OF MANUFACTURE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/824965 | METHOD AND DEVICE FOR DETECTING A RACE CONDITION |
| FREESCALE SEMICONDUCTOR, INC. | 13/826117 | COMPUTER SYSTEMS AND METHODS WITH RESOURCE TRANSFER HINT INSTRUCTION |
| FREESCALE SEMICONDUCTOR, INC. | 13/826209 | TRANSISTOR WITH CHARGE ENHANCED FIELD PLATE STRUCTURE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 13/826347 | BUILT-IN SELF TEST (BIST) WITH CLOCK CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | 13/826427 | MEMORY WITH POWER SAVINGS FOR UNNECESSARY READS |
| FREESCALE SEMICONDUCTOR, INC. | 13/826958 | NON-VOLATILE MEMORY (NVM) WITH WORD LINE DRIVER/DECODER USING A CHARGE PUMP VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/827004 | DATA PROCESSOR DEVICE FOR HANDLING A WATCHPOINT AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/828213 | VOLTAGE REGULATOR WITH CURRENT LIMITER |
| FREESCALE SEMICONDUCTOR, INC. | 13/828810 | MICROELECTROMECHANICAL SYSTEM DEVICES HAVING THROUGH SUBSTRATE VIAS AND METHODS FOR THE FABRICATION THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/829549 | METHODS AND APPARATUS FOR SENSING MOTION OF A PORTABLE CONTAINER AND PROVIDING HUMAN PERCEPTIBLE INDICIA BASED ON THE SENSED MOTION |
| FREESCALE SEMICONDUCTOR, INC. | 13/829737 | STACKED MICROELECTRONIC PACKAGES HAVING SIDEWALL CONDUCTORS AND METHODS FOR THE FABRICATION THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 13/830701 | ADDRESS CALCULATION FOR RECEIVED DATA |
| FREESCALE SEMICONDUCTOR, INC. | 13/831828 | DUAL SUPPLY LEVEL SHIFTER CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 13/831850 | METHOD AND APPARATUS FOR DETECTING A COLLISION BETWEEN MULTIPLE THREADS OF EXECUTION FOR ACCESSING A MEMORY ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | 13/831870 | Method and Apparatus for Memory Array Access |
| FREESCALE SEMICONDUCTOR, INC. | 13/833290 | MULTIPLE AXIS RATE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/833509 | TASK SCHEDULING METHOD AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | 13/835068 | NEGATIVE CHARGE PUMP REGULATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/835690 | Method and Apparatus for Sensing On-Chip Characteristics |
| FREESCALE SEMICONDUCTOR, INC. | 13/835911 | APPLICATION OF NORMALLY CLOSED POWER SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 13/836882 | COMPENSATED HYSTERESIS CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/837565 | METHOD FOR PROVISIONING DECOUPLING CAPACITANCE IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 13/837652 | NON-VOLATILE MEMORY (NVM) WITH BLOCK-SIZE-AWARE PROGRAM/ERASE |
| FREESCALE SEMICONDUCTOR, INC. | 13/838133 | SYSTEM AND METHOD FOR ASSIGNING MEMORY ACCESS TRANSFERS BETWEEN COMMUNICATION CHANNELS |
| FREESCALE SEMICONDUCTOR, INC. | 13/839079 | SYSTEM AND METHOD FOR IMPROVED MEMS OSCILLATOR STARTUP |
| FREESCALE SEMICONDUCTOR, INC. | 13/841242 | METHOD AND DEVICE FOR HANDLING DATA VALUES |
| FREESCALE SEMICONDUCTOR, INC. | 13/841630 | METHOD AND DEVICE FOR GENERATING AN EXCEPTION |
| FREESCALE SEMICONDUCTOR, INC. | 13/841916 | SYSTEM AND METHOD FOR TRANSFERRING DATA BETWEEN COMPONENTS OF A DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/842006 | METHOD AND DEVICE IMPLEMENTING EXECUTE-ONLY MEMORY |

PROTECTION

| FREESCALE SEMICONDUCTOR, INC. | 13/842516 | CONTINUOUS RUN-TIME INTEGRITY CHECKING FOR VIRTUAL MEMORY |
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| FREESCALE SEMICONDUCTOR, INC. | 13/843090 | SYSTEM AND METHOD FOR MULTICORE PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | 13/843179 | THREAD-SUSPENDING EXECUTION BARRIER |
| FREESCALE SEMICONDUCTOR, INC. | 13/848348 | Power Monitoring Circuitry |
| FREESCALE SEMICONDUCTOR, INC. | 13/848734 | HELIX SUBSTRATE AND THREE-DIMENSIONAL PACKAGE WITH SAME |
| FREESCALE SEMICONDUCTOR, INC. | 13/848819 | INHIBITING PROPAGATION OF SURFACE CRACKS IN A MEMS DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/849460 | METHODS AND SYSTEMS FOR SELECTIVELY FORMING METAL LAYERS ON LEAD FRAMES AFTER DIE ATTACHMENT |
| FREESCALE SEMICONDUCTOR, INC. | 13/849543 | SOLAR POWERED IC CHIP |
| FREESCALE SEMICONDUCTOR, INC. | 13/853061 | SYSTEM FOR MANAGING CONFIGURATION UPDATES IN CLUSTER OF COMPUTATIONAL DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 13/854137 | SEMICONDUCTOR DEVICE AND METHOD OF ASSEMBLING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 13/854140 | SEMICONDUCTOR DEVICE AND METHOD OF ASSEMBLING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 13/857131 | STIFFENED SEMICONDUCTOR DIE PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/857143 | METHOD OF FORMING STACKED DIE PACKAGE USING REDISTRIBUTED CHIP PACKAGING |
| FREESCALE SEMICONDUCTOR, INC. | 13/859490 | METHODS AND APPARATUS FOR CALIBRATING TRANSDUCER-INCLUDING DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 13/861509 | Double Patterning Aware Routing Without Stitching |
| FREESCALE SEMICONDUCTOR, INC. | 13/862473 | FLUID COOLED SEMICONDUCTOR DIE PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | 13/864729 | INTEGRATED CIRCUIT CHIP WITH DISCONTINUOUS GUARD RING |
| FREESCALE SEMICONDUCTOR, INC. | 13/865185 | WIRE BONDING MACHINE AND METHOD FOR TESTING WIRE BOND CONNECTIONS |
| FREESCALE SEMICONDUCTOR, INC. | 13/865794 | Startup Circuits with Native Transistors |
| FREESCALE SEMICONDUCTOR, INC. | 13/866034 | MIXED SIGNAL IP CORE PROTOTYPING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 13/867656 | MEMS DEVICE WITH STRESS ISOLATION AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/867720 | ESTIMATION OF SIDEWALL SKEW ANGLES OF A STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | 13/868125 | METHOD OF FABRICATING MEMS DEVICE HAVING RELEASE ETCH STOP LAYER |
| FREESCALE SEMICONDUCTOR, INC. | 13/868777 | AMPLIFIER USING NONLINEAR DRIVERS |
| FREESCALE SEMICONDUCTOR, INC. | 13/871411 | METHODS AND SYSTEMS FOR GATE DIMENSION CONTROL IN MULTI-GATE STRUCTURES FOR SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | 13/872643 | SELECTIVE GATE OXIDE PROPERTIES ADJUSTMENT USING FLUORINE |
| FREESCALE SEMICONDUCTOR, INC. | 13/873217 | STANDARD CELL FOR SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 13/873454 | AMPLIFIERS AND RELATED RECEIVER SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | 13/873621 | METHOD AND APPARATUS FOR ACCELERATING SPARSE MATRIX OPERATIONS IN FULL ACCURACY CIRCUIT SIMULATION |
| FREESCALE SEMICONDUCTOR, INC. | 13/873655 | Integrated Circuit Design Verification Through Forced Clock Glitches |
| FREESCALE SEMICONDUCTOR, INC. | 13/873752 | SELF-DEFINING, LOW CAPACITANCE WIRE BOND PAD |
| FREESCALE SEMICONDUCTOR, INC. | 13/873917 | SCALABLE SPLIT GATE MEMORY CELL ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | 13/873988 | SYNCHRONOUS MULTIPLE PORT MEMORY WITH ASYNCHRONOUS PORTS |
| FREESCALE SEMICONDUCTOR, INC. | 13/873998 | FOUR-PORT MEMORY WITH MULTPLE CORES |

| FREESCALE SEMICONDUCTOR, INC. | 13/874119 | NON-VOLATILE MEMORY (NVM) WITH VARIABLE VERIFY OPERATIONS |
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| FREESCALE SEMICONDUCTOR, INC. | 13/874127 | BIASING SPLIT GATE MEMORY CELL DURING POWER-OFF MODE |
| FREESCALE SEMICONDUCTOR, INC. | 13/874477 | METHOD AND APPARATUS FOR GENERATING GATE-LEVEL ACTIVITY DATA FOR USE IN CLOCK GATING EFFICIENCY ANALYSIS |
| FREESCALE SEMICONDUCTOR, INC. | 13/875618 | ELECTROSTATIC DISCHARGE (ESD) CLAMP CIRCUIT WITH HIGH EFFECTIVE HOLDING VOLTAGE |
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| FREESCALE SEMICONDUCTOR, INC. | 13/988821 | ERROR CORRECTING DEVICE, METHOD FOR MONITORING AN ERROR CORRECTING DEVICE AND DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | 13/989280 | METHOD AND APPARATUS FOR MANAGING POWER IN A MULTI-CORE PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | 13/989288 | SWITCHING ARRANGEMENT, INTEGRATED CIRCUIT COMPRISING SAME, METHOD OF CONTROLLING A SWITCHING ARRANGEMENT, AND RELATED COMPUTER PRORAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | 13/995190 | INTEGRATED CIRCUIT DEVICE AND METHOD FOR PERFORMING CONDITIONAL NEGATION OF DATA |
| FREESCALE SEMICONDUCTOR, INC. | 14/003361 | METHOD FOR RANKING PATHS FOR POWER OPTIMIZATION OF AN INTEGRATED CIRCUIT DESIGN AND CORRESPONDING COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | 14/005475 | INTEGRATED CIRCUIT DEVICE AND METHODS OF PERFORMING BIT MANIPULATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | 14/006022 | INTEGRATED CIRCUIT DEVICE AND METHOD FOR ENABLING CROSS-CONTEXT ACCESS |
| FREESCALE SEMICONDUCTOR, INC. | 14/006034 | PROCESSOR SYSTEM WITH PREDICATE REGISTER, COMPUTER SYSTEM, METHOD FOR MANAGING PREDICATES AND COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | 14/006388 | INTEGRATED CIRCUIT AND METHOD FOR REDUCING AN IMPACT OF ELECTRICAL STRESS IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 14/007861 | INTEGRATED CIRCUIT DEVICE AND METHODS FOR PERFORMING CUTTHROUGH FORWARDING |
| FREESCALE SEMICONDUCTOR, INC. | 14/008581 | APPARATUS FOR FORWARD WELL BIAS IN A SEMICONDUCTOR INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 14/008583 | A METHOD AND APPARATUS FOR CONTROLLING FETCH-AHEAD IN A VLES PROCESSOR ARCHITECTURE |
| FREESCALE SEMICONDUCTOR, INC. | 14/009009 | RECEIVER DEVICE, MULTI-FREQUENCY RADAR SYSTEM AND VEHICLE |
| FREESCALE SEMICONDUCTOR, INC. | 14/009099 | AMPLIFIERS AND RELATED INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | 14/010557 | PRESSURE SENSOR DEVICE AND METHOD OF ASSEMBLING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 14/011160 | METHOD FOR FORMING A PACKAGED SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 14/011289 | Sequential Wafer Bonding |
| FREESCALE SEMICONDUCTOR, INC. | 14/012884 | NEGATIVE VOLTAGE MEASUREMENT |
| FREESCALE SEMICONDUCTOR, INC. | 14/013792 | ELECTRO-MECHANICAL OSCILLATOR AND COMMON-MODE DETECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 14/013923 | MICROELECTRONIC PACKAGES CONTAINING OPPOSING DEVICES AND METHODS FOR THE FABRICATION THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 14/015006 | Split Gate Nanocrystal Memory Integration |
| FREESCALE SEMICONDUCTOR, INC. | 14/015429 | SYSTEMS AND METHODS FOR SECURE BOOT ROM PATCH |
| FREESCALE SEMICONDUCTOR, INC. | 14/015519 | CLOCK GLITCH DETECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | 14/015889 | SECURE FIRMWARE FLASH CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | 14/016080 | METHOD AND CIRCUIT FOR CONTROLLING TURN-OFF OF A SEMICONDUCTOR SWITCHING ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | 14/016125 | SINGLE PORT MEMORY THAT EMULATES DUAL PORT MEMORY |

| FREESCALE SEMICONDUCTOR, INC. | 14/016931 | ELECTRONIC DEVICE INCLUDING INTERCONNECTS WITH A CAVITY THEREBETWEEN AND A PROCESS OF FORMING THE SAME |
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| FREESCALE SEMICONDUCTOR, INC. | 14/016957 | WAFER-LEVEL GATE STRESS TESTING |
| FREESCALE SEMICONDUCTOR, INC. | 14/017867 | EDGE COUPLING OF SEMICONDUCTOR DIES |
| FREESCALE SEMICONDUCTOR, INC. | 14/018091 | SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 14/019066 | MULTIPLE SENSE AXIS MEMS GYROSCOPE HAVING A SINGLE DRIVE MODE |
| FREESCALE SEMICONDUCTOR, INC. | 14/020532 | ESD PROTECTION USING ISOLATED DIODES |
| FREESCALE SEMICONDUCTOR, INC. | 14/020840 | PACKAGE-ON-PACKAGE SEMICONDUCTOR SENSOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 14/020841 | COPPER PILLAR BUMP AND FLIP CHIP PACKAGE USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 14/021485 | Method of Forming Different Voltage Devices with High-K Metal Gate |
| FREESCALE SEMICONDUCTOR, INC. | 14/022646 | METHODS FOR FORMING CONTACT LANDING REGIONS IN SPLIT-GATE NON-VOLATILE MEMORY (NVM) CELL ARRAYS |
| FREESCALE SEMICONDUCTOR, INC. | 14/022872 | MASTER-SLAVE FLIP-FLOP WITH REDUCED SETUP TIME |
| FREESCALE SEMICONDUCTOR, INC. | 14/023440 | NON-VOLATILE MEMORY (NVM) CELL AND HIGH-K AND METAL GATE TRANSISTOR INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | 14/023781 | UNIVERSAL SPI (SERIAL PERIPHERAL INTERFACE) |
| FREESCALE SEMICONDUCTOR, INC. | 14/024742 | RECESSED SEMICONDUCTOR DIE STACK |
| FREESCALE SEMICONDUCTOR, INC. | 14/028489 | SYSTEM AND METHOD FOR DATA SYNCHRONIZATION ACROSS DIGITAL DEVICE INTERFACES |
| FREESCALE SEMICONDUCTOR, INC. | 14/029766 | SEMICONDUCTOR DEVICE AND LEAD FRAME WITH INTERPOSER |
| FREESCALE SEMICONDUCTOR, INC. | 14/029779 | HEAT SPREADER FOR INTEGRATED CIRCUIT DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 14/029783 | SIDE VENTED PRESSURE SENSOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | 14/029976 | SQUIB DRIVER DIAGNOSTIC CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | 14/030952 | SYSTEM-IN-PACKAGES CONTAINING EMBEDDED SURFACE MOUNT DEVICES AND METHODS FOR THE FABRICATION THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | 14/033622 | NON-VOLATILE MEMORY (NVM) WITH DYNAMICALLY ADJUSTED REFERENCE CURRENT |
| FREESCALE SEMICONDUCTOR, INC. | 14/034213 | STACKED PROTECTION DEVICES AND RELATED FABRICATION METHODS |
| FREESCALE SEMICONDUCTOR, INC. | 14/035704 | TEMPERATURE DEPENDENT BIASING FOR LEAKAGE POWER REDUCTION |
| FREESCALE SEMICONDUCTOR, INC. | 14/035999 | PACKAGE ENCAPSULANT RELIEF FEATURE |
| FREESCALE SEMICONDUCTOR, INC. | 14/038401 | A MEMORY HAVING ONE TIME PROGRAMMABLE (OTP) ELEMENTS AND A METHOD OF PROGRAMMING THE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 14/039562 | SYSTEM AND METHOD FOR ENABLING MAXIMUM PERFORMANCE OPERATION WITHIN AN EXTENDED AMBIENT TEMPERATURE RANGE |
| FREESCALE SEMICONDUCTOR, INC. | 14/039622 | 3D DEVICE PACKAGING USING THROUGH-SUBSTRATE PILLARS |
| FREESCALE SEMICONDUCTOR, INC. | 14/040795 | METHOD AND DEVICE FOR GENERATING FLOATING-POINT VALUES |
| FREESCALE SEMICONDUCTOR, INC. | 14/041449 | METHOD OF MAKING A FLOATING GATE NONVOLATILE MEMORY (NVM) WITH BREAKDOWN PREVENTION |
| FREESCALE SEMICONDUCTOR, INC. | 14/041591 | NON-VOLATILE MEMORY (NVM) AND HIGH-K AND METAL GATE INTEGRATION USING GATE-LAST METHODOLOGY |
| FREESCALE SEMICONDUCTOR, INC. | 14/041647 | NON-VOLATILE MEMORY (NVM) AND HIGH-K AND METAL GATE INTEGRATION USING GATE-FIRST METHODOLOGY |
| FREESCALE SEMICONDUCTOR, INC. | 14/041662 | NON-VOLATILE MEMORY (NVM) AND HIGH-K AND METAL GATE INTEGRATION USING GATE-LAST METHODOLOGY |
| FREESCALE SEMICONDUCTOR, INC. | 14/041697 | DYNAMIC PROGRAMMING FOR FLASH MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | 14/041910 | DATA PROCESSING SYSTEM WITH CACHE LINEFILL BUFFER AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | 14/041968 | MOLD LOCKS FOR LAMINATE SUBSTRATES |
| FREESCALE SEMICONDUCTOR, INC. | 14/042623 | DEVICES AND STACKED MICROELECTRONIC PACKAGES WITH PARALLEL CONDUCTORS AND INTRA-CONDUCTOR ISOLATOR STRUCTURES AND METHODS OF THEIR FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 14/042628 | DEVICES AND STACKED MICROELECTRONIC PACKAGAES WITH INTRENCH PACKAGE SURFACE CONDUCTORS AND METHODS OF THEIR FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | 14/042662 | ELECTRONIC COMPONENT PACKAGE AND METHOD FOR FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | 61/835718 | TIN-BASED WIREBOND STRUCTURES |
| | | |

Freescale Semiconductor, Inc. – Registered Patents; Foreign

| <u>Owner</u> | Country | Patent # | Title |
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| FREESCALE SEMICONDUCTOR, INC. | SG | 33552 | CHEMICAL—MECHANICAL POLISHER AND A PROCESS FOR POLISHING |
| FREESCALE SEMICONDUCTOR, INC. | SG | 33620 | METHOD AND APPARATUS FOR PLATI NG METALS |
| FREESCALE SEMICONDUCTOR, INC. | SG | 33670 | PRECONDITIONER FOR A POLISHING PAD AND METHOD FOR USING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | SG | 40873 | METHOD FOR READING AND RESTORI NG DATA IN A DATA STORAGE ELEM ENT |
| FREESCALE SEMICONDUCTOR, INC. | SG | 45265 | TRENCH ISOLATION STRUCTURE IN AN INTEGRATED CIRCUIT AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | SG | 45511 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | SG | 50467 | DOUBLE IMPLANTED LATERALLY DIF FUSED MOS DEVICE AND METHOD TH EREOF |
| FREESCALE SEMICONDUCTOR, INC. | SG | 50524 | SEMICONDUCTOR DEVICE HAVING ANTI-REFLECTIVE COATING AND METHOD FOR MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | SG | 52265 | SMART OPTICAL CONNECTOR AND SMART OPTICAL CONNECTOR SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | SG | 55996 | PROCESS FOR POLISHING A SEMICO NDUCTOR DEVICE SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | SG | 60216 | PACKAGING APPARATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | SG | 63831 | METHOD FOR DEPOSITING A DIFFUSION BARRIER |
| FREESCALE SEMICONDUCTOR, INC. | SG | 65067 | CIRCUIT AND METHOD OF LIMITING LEAKAGE CURRENT IN A MEMORY C IRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | SG | 65654 | CIRCUIT FOR TRACKING RAPID CHA NGES IN MID-POINT VOLTAGE OF A DATA SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | SG | 67359 | METHOD OF FORMING A UNILATERAL , GRADED- CHANNEL SEMICONDUCTOR DEVICE USING A GATE ELECTRODE DISPOSABLE SPACER |
| FREESCALE SEMICONDUCTOR, INC. | SG | 67526 | METHOD AND APPARATUS FOR PROCESSING A SEMICONDUCTOR WAFER ON A ROBOTIC TRACK HAVING ACCESS TO IN SITU WAFER BACKSIDE PARTICLE DETECTION |

| FREESCALE SEMICONDUCTOR, INC. | SG | 67542 | VARIABLE CAPACITOR AND METHOD FOR FABRICATING THE SAME |
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| FREESCALE SEMICONDUCTOR, INC. | SG | 67572 | A CHEMICAL MECHANICAL POLISHING (CMP) SLURRY FOR COPPER AND METHOD OF USE IN INTEGRATED CIRCUIT MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | SG | 68697 | A CHEMICAL MECHANICAL POLISHING SYSTEM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | SG | 69172 | DATA PROCESSING SYSTEM HAVING A SELF-ALIGNING STACK POINTER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | SG | 69959 | SEMICONDUCTOR DEVICE AND FERRO ELECTRIC CAPACITOR |
| FREESCALE SEMICONDUCTOR, INC. | SG | 71045 | A METHOD FOR MANUFACTURING A L OW DIELECTRIC CONSTANT INTERLE VEL INTEGRATED CIRCUIT STRUCTU RE |
| FREESCALE SEMICONDUCTOR, INC. | SG | 71075 | METHOD FOR PACKAGING AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | SG | 71111 | PROCESS FOR DEPOSITING A LAYER OF MATERIAL ON A SUBSTRATE AND A PLATING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | SG | 71717 | MEMORY SUITABLE FOR OPERATION AT LOW POWER SUPPLY VOLTAGES AND SENSE AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | SG | 72653 | SEMICONDUCTOR DEVICE HAVING FIELD ISOLATION AND A PROCESS FOR FORMING THE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | SG | 72750 | INTEGRATED CIRCUIT HAVING A DUMMY STRUCTURE ANI METHOD OF MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | SG | 74622 | CLOCK RECOVERY CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | SG | 75330 | A METHOD FOR MANUFACTURING AND DESIGNING AN ELECTRONIC DEVICE AND ELECTRONIC APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | SG | 77642 | POINT OF USE DILUTION TOOL AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | SG | 78283 | METHOD AND APPARATUS FOR PERFORMING OPERATIVE TESTING ON AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | SG | 79962 | PROCESS FOR POLISHING DISSIMILAR CONDUCTIVE LAYERS IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | SG | 82537 | STATIC RANDOM ACCESS MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | SG | 83793 | METHOD OF FORMING A COPPER LAYER OVER A SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | SG | 84587 | SEMICONDUCTOR DEVICE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | SG | 84605 | SEMICONDUCTOR DEVICE MEMORY CELL AND METHOD FOR SELECTIVELY ERASING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | SG | 84609 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | SG | 85687 | INTEGRATED CIRCUIT HAVING A DUMMY STRUCTURE AND METHOD OF MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | SG | 85688 | A METHOD FOR MANUFACTURING A LOW DIELECTRIC CONSTANT INTERLEVEL INTEGRATED CIRCUIT STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | SG | 85710 | METHOD FOR FABRICATING A SEMICONDUCTOR |

STRUCTURE INCLUDING A METAL OXIDE INTERFACE

| FREESCALE SEMICONDUCTOR, INC. | SG | 85923 | SEMICONDUCTOR DEVICE AND A PROCESS FOR DESIGNING A MASK |
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| FREESCALE SEMICONDUCTOR, INC. | SG | 86339 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | SG | 88743 | CONFIGURABLE LOGIC ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | SG | 88747 | A METHOD AND MACHINE FOR UNDER FILLING AN ASSEMBLY TO FORM A SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | SG | 88805 | PEAK PROGRAM CURRENT APPARATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | SG | 89364 | METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE HAVING A STABLE CRYSTALLINE INTERFACE WITH SILICON |
| FREESCALE SEMICONDUCTOR, INC. | SG | 89365 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | SG | 89366 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE AND A CONDUCTIVE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | SG | 90163 | A SIGNAL PROCESSING CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | SG | 90219 | SEMICONDUCTOR DEVICE AND A PROCESS FOR FORMING THE SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | SG | 90854 | ETCHING SOLUTION AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | SG | 91317 | SEMICONDUCTOR STRUCTURE HAVING A CRYSTALLINE ALKALINE EARTH METAL SILICON NITRIDE/OXIDE INTERFACE WITH SILICON |
| FREESCALE SEMICONDUCTOR, INC. | SG | 92191 | METHOD OF MANUFACTURING A HETEROJUNCTION BICMOS INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | SG | 92367 | METHOD AND APPARATUS FOR MANUFACTURING AN INTERCONNECT STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | SG | 92495 | SINGLE SUPPLY HFET WITH TEMPERATURE COMPENSATION |
| FREESCALE SEMICONDUCTOR, INC. | SG | 93085 | ULTRA-LATE PROGRAMMING ROM AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | SG | 93163 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND CHEMICAL-MECHANICAL POLISHING SYSTEM THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | SG | 93596 | DUAL METAL GATE TRANSISTORS FOR CMOS PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | SG | 93833 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | SG | 95621 | UV CURE PROCESS AND TOOL FOR LOW K FILM FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | SG | 97850 | SEMICONDUCTOR DEVICE HAVING X- SHAPED DIE SUPPORT MEMBER AND METHOD FOR MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | SG | 98005 | SEMICONDUCTOR DEVICE AND PROCESS THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | SG | 98237 | SEMICONDUCTOR TILING STRUCTURE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | SG | 98892 | LITHOGRAPHY METHOD FOR FORMING SEMICONDUCTOR DEVICES ON A WAFER AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | SG | 98893 | HIGH K DIELECTRIC FILM AND METHOD FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | SG | 99991 | METHOD AND DEVICE FOR CREATING AND USING PRE- |

INTERNALIZED PROGRAM FILES

| FREESCALE SEMICONDUCTOR, INC. | SG | 100552 | METHOD OF FORMING AN INTEGRATED CIRCUIT DEVICE USING DUMMY FEATURES AND STRUCTURE THEREOF |
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| FREESCALE SEMICONDUCTOR, INC. | SG | 100560 | INTEGRATION OF TWO MEMORY TYPES ON THE SAME INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | SG | 100732 | PROGRAMMABLE DELAY CONTROL IN A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | SG | 101116 | SEMICONDUCTOR DEVICE AND A METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | SG | 101201 | SYSTEM AND METHOD FOR CONTROLLING BUS ARBITRATION DURING CACHE MEMORY BURST CYCLES |
| FREESCALE SEMICONDUCTOR, INC. | SG | 101423 | METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE HAVING A CRYSTALLINE ALKALINE EARTH METAL OXIDE INTERFACE WITH SILICON |
| FREESCALE SEMICONDUCTOR, INC. | SG | 101949 | METHOD AND APPARATUS FOR TESTING AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | SG | 102485 | PROCESS FOR MAKING A MIM CAPACITOR |
| FREESCALE SEMICONDUCTOR, INC. | SG | 102553 | CIRCUIT AND METHOD OF FREQUENCY SYNTHESIZER CONTROL WITH A SERIAL PERIPHERAL INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | SG | 103040 | METHOD OF FORMING A BOND PAD AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | SG | 103248 | PROGRAMMABLE DELAY CONTROL IN A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | SG | 106181 | SEMICONDUCTOR PACKAGE DEVICE AND METHOD OF FORMATION AND TESTING |
| FREESCALE SEMICONDUCTOR, INC. | SG | 107700 | METHOD AND SYSTEM FOR DETERMINING A THICKNESS OF A LAYER |
| FREESCALE SEMICONDUCTOR, INC. | SG | 112136 | METHOD FOR ELIMINATING VOIDING IN PLATED SOLDER |
| FREESCALE SEMICONDUCTOR, INC. | SG | 113084 | THIN GAAS WITH COPPER BACK-METAL STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | SG | 113189 | METHOD AND APPARATUS FOR TRANSLATING DETECTED WAFER DEFECT COORDINATES TO RETICLE COORDINATES USING CAD DATA |
| FREESCALE SEMICONDUCTOR, INC. | SG | 113301 | METAL REDUCTION IN WAFER SCRIBE AREA |
| FREESCALE SEMICONDUCTOR, INC. | SG | 113302 | UNDERFILL FILM FOR PRINTED WIRING ASSEMBLIES |
| FREESCALE SEMICONDUCTOR, INC. | SG | 113645 | APPARATUS AND METHOD FOR POWER MANAGEMENT IN A TIRE PRESSURE MONITORING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | SG | 113921 | WIREBONDING INSULATED WIRE |
| FREESCALE SEMICONDUCTOR, INC. | SG | 114077 | MULTI-DIE SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | SG | 116107 | CIRCUIT DEVICE WITH AT LEAST PARTIAL PACKAGING AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | SG | 119489 | SEMICONDUCTOR DEVICE WITH NANOCLUSTERS |
| FREESCALE SEMICONDUCTOR, INC. | IL | 121044 | DYNAMIC MEMORY DEVICE WITH REF RESH METHOD |
| FREESCALE SEMICONDUCTOR, INC. | SG | 121556 | METHOD AND APPARATUS FOR FORMING AN SOI BODY-CONTACTED TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | SG | 122151 | WIREBONDING INSULATED WIRE AND CAPILLARY THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | SG | 122419 | IMMERSION LITHOGRAPHY TECHNIQUE AND PRODUCT USING A PROTECTION LAYER COVERING THE RESIST |
| FREESCALE SEMICONDUCTOR, INC. | SG | 123159 | LAND GRID ARRAY PACKAGED DEVICE AND METHOD OF |

FORMING SAME

| SG | 124223 | INTEGRATED CIRCUIT MEMORY HAVING A FUSE DETECT CIRCUIT AND METHOD THEREFOR |
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| SG | 126214 | METHOD AND APPARATUS FOR DOHERTY AMPLIFIER BIASING |
| SG | 127587 | LEAD SOLDER INDICATOR AND METHOD |
| SG | 127590 | METHOD FOR ASSEMBLING A SEMICONDUCTOR COMPONENT AND APPARATUS THEREFOR |
| TW | 128143 | FAST START-UP CIRCUIT |
| CN | 00128673 | A SIGNAL PROCESSING CIRCUIT |
| SG | 130855 | METHOD OF INTEGRATING OPTICAL DEVICES AND ELECTRONIC DEVICES ON AN INTEGRATED CIRCUIT |
| SG | 131559 | PACKAGED DEVICE AND METHOD OF FORMING SAME |
| SG | 131913 | METHOD FOR FORMING MULTI-LAYER BUMPS ON A SUBSTRATE |
| SG | 132619 | METHOD FOR PACKAGING A SEMICONDUCTOR DEVICE |
| SG | 133486 | METHOD OF MAKING EXPOSED PAD BALL GRID ARRAY PACKAGE |
| SG | 133747 | METHODS AND APPARATUS HAVING WAFER LEVEL CHIP SCALE PACKAGE FOR SENSING ELEMENTS |
| SG | 134715 | METHOD OF MAKING REINFORCED SEMICONDUCTOR PACKAGE |
| SG | 135133 | METHOD OF TESTING FOR POWER AND GROUND CONTINUITY OF A SEMICONDUCTOR DEVICE |
| SG | 135172 | METHOD FOR FORMING REINFORCED INTERCONNECTS ON A SUBSTRATE |
| KR | 144805 | PROCESS FOR FORMING TIN- BISMUTH SOLDER CONNECTION HAVING IMPROVED HIGH TEMPERATURE PROPERTIES |
| SG | 144997 | METHOD AND APPARATUS FOR A STEPPED-DRIFT MOSFET |
| SG | 145015 | INTEGRATED CIRCUIT WITH MEMORY AND METHOD OF CONFIGURING A MEMORY |
| SG | 145843 | METHOD OF MAKING A MULTIPLE CRYSTAL ORIENTATION SEMICONDUCTOR DEVICE |
| SG | 151356 | METHODS AND APPARATUS FOR A QUAD FLAT NO-LEAD (QFN) PACKAGE |
| KR | 175973 | METHOD AND APPARATUS FOR PROVI DING A VIDEO SYNCHRONISING SIG NAL OF A PREDETERMINED POLARIT Y |
| KR | 182291 | SEMICONDUCTOR PRESSURE SENSOR MEANS AND METHOD |
| TW | 187523 | A HIGH FREQUENCY (HF) DEVICE AND IT'S METHOD OF MANUFACTURE. |
| IN | 190560 | FREQUENCY INVERSION SCRAMBLER WITH INTEGRATED HIGH-PASS FILTER |
| KR | 194848 | FLAGLESS SEMICONDUCTOR PACKAGE |
| MX | 195558 | METHOD FOR MAKING AN ELECTRONI C COMPONENT HAVING AN ORGANIC SUBSTRATE |
| KR | 198911 | EEPROM CELL WITH ISOLATION TRA NSISTOR AND METHODS FOR MAKING AND OPERATING THE SAME |
| KR | 204199 | NITRIDE REMOVAL METHOD |
| | SG S | SG 127587 SG 127590 TW 128143 CN 00128673 SG 130855 SG 131559 SG 131913 SG 132619 SG 133486 SG 133747 SG 134715 SG 135133 SG 135172 KR 144805 SG 144997 SG 145015 SG 145843 SG 151356 KR 175973 KR 182291 TW 187523 IN 190560 KR 194848 MX 195558 KR 198911 |

| FREESCALE SEMICONDUCTOR, INC. | MX | 206431 | PROCESS FOR DEPOSITING A LAYER OF MATERIAL ON A SUBSTRATE AN D A PLATING SYSTEM |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 217450 | PROCESS FOR FORMING A SEMICOND UCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 219772 | SEMICONDUCTOR DEVICE HAVING X- SHAPED DIE SUPPORT MEMBER AND METHOD FOR MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | IN | 226855 | INTEGRATED CIRCUIT DIE I/O CELLS |
| FREESCALE SEMICONDUCTOR, INC. | IN | 227878 | MULTI-DIE SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 232939 | METHOD FOR PLATING USING NESTE D PLATING BUSES AND SEMICONDUC TOR DEVICE HAVING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | IN | 236528 | SIGNAL GENERATION POWER MANAGEMENT CONTROL SYSTEM FOR PORTABLE COMMUNICATIONS DEVICE AND METHOD OF USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | IN | 237654 | INTEGRATED CIRCUIT POWER MANAGEMENT FOR REDUCING LEAKAGE CURRENT IN CIRCUIT ARRAYS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | IN | 238056 | DIE ENCAPSULATION USING A POROUS CARRIER |
| FREESCALE SEMICONDUCTOR, INC. | IN | 238717 | CELLULAR MODEM PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | IN | 239828 | PREFETCH CONTROL IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | IN | 240630 | NON-VOLATILE MEMORY HAVING A BIAS ON THE SOURCE ELECTRODE FOR HCI PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | IN | 243471 | METHOD TO PASSIVATE CONDUCTIVE SURFACES DURING SEMICONDUCTOR PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | IN | 244610 | MULTIPLE BURST PROTOCOL DEVICE CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | IN | 246001 | METHOD AND APPARATUS FOR ENDIANNESS CONTROL IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | IN | 249366 | AUTOMATIC HIDDEN REFRESH IN A DRAM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | IN | 249921 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING A SILICIDE LAYER |
| FREESCALE SEMICONDUCTOR, INC. | IN | 255421 | MEMORY DEVICE WITH A DATA HOLD LATCH |
| FREESCALE SEMICONDUCTOR, INC. | IN | 255616 | METHOD FOR MAKING A SEMICONDUCTOR STRUCTURE USING SILICON GERMANIUM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 256378 | METHOD AND APPARATUS FOR NOISE BURST DETECTION IN A SIGNAL P ROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | IN | 256521 | MOTION SENSING FOR TIRE PRESSURE MONITORING |
| FREESCALE SEMICONDUCTOR, INC. | IN | 257314 | WIRELESS TRANSCEIVER AND METHOD OF OPERATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 267002 | METHOD AND APPARATUS FOR CONTR OLLING THE DISPLAY OF A VIDEO IMAGE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 275059 | EXTENSIBLE CENTRAL PROCESSING UNIT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 276790 | SIGMA-DELTA MODULATOR WITH IMP ROVED TONE REJECTION AND METHO D THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 283827 | DATA PROCESSOR WITH AN EFFICIE NT BIT MOVE CAPABILITY AND MET HOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 286197 | DATA PROCESSOR INITIALIZATION PROGRAM AND METHOD |

THEREFOR

| FREESCALE SEMICONDUCTOR, INC. | KR | 287600 | DATA PROCESSING SYSTEM PROVIDING AN EXTENSIBLE REGISTER AND METHOD THEREOF |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 289594 | SCAN TEST CIRCUIT FOR USE IN SEMICONDUCTOR INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 292213 | DIGITAL INTEGRATOR WITH REDUCE D CIRCUIT AREA AND ANALOG-TO-D IGITAL CONVERTER USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 298562 | LINEAR ATTENUATOR FOR CURRENT- MODE DIGITAL-TO- ANALOG CONVERT ER (DAC) OR THE LIKE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 298563 | SEMICONDUCTOR PACKAGE AND METH OD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 300257 | LOCALIZED ATD SUMMATION FOR A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | KR | 300258 | METHOD AND STRUCTURE FOR FORMING AN INTEGRATED CIRCUIT PATTE RN ON A SEMICONDUCTOR SUBSTRAT E |
| FREESCALE SEMICONDUCTOR, INC. | KR | 306935 | TRENCH ISOLATION STRUCTURE IN AN INTEGRATED CIRCUIT AND METH OD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 310399 | METHOD AND APPARATUS FOR TRANS FERRING DATA OVER A PROCESSOR INTERFACE BUS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 311168 | N-TYPE HIGFET AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | KR | 311170 | METHOD OF FORMING A UNILATERAL , GRADED-CHANNEL SEMICONDUCTOR DEVICE USING A GATE ELECTRODE DISPOSABLE SPACER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 325278 | A DATA PROCESSOR FOR EXECUTING A FUZZY LOGIC OPERATION AND M ETHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 326693 | POWER MOS TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 326694 | METHOD FOR FABRICATING A SEMIC ONDUCTOR DEVICE USING LATERAL GETTERING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 328160 | MEMORY HAVING BIT LINE LOAD WI TH AUTOMATIC BIT LINE PRECHARG E AND EQUALIZATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 329454 | PROCESS FOR DEPOSITING A LAYER OF MATERIAL ON A SUBSTRATE AN D A PLATING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 330294 | A BUS PROTOCAL AND METHOD FOR CONTROLLING A DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 334184 | METHOD AND APPARATUS FOR TESTI NG A STATIC RAM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 335019 | RESISTOR STRUCTURE AND METHOD OF SETTING A RESISTANCE VALUE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 341943 | A CHARGE PUMP WITH A PROGRAMMA BLE PUMP CURRENT AND SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 341945 | METHOD OF ADHESION TO A POLYMI DE SURFACE BY FORMATION OF COV ALENT BONDS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 346320 | PRESSURE SENSOR WITH STRESS IS OLATION PLATFORM HERMETICALLY SEALED TO PROTECT SENSOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 350005 | FREQUENCY INVERSION SCRAMBLER WITH INTEGRATED HIGH-PASS FILT ER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 350568 | DATA PROCESSING SYSTEM FOR PER FORMING A DEBUG |

FUNCTION AND M ETHOD THEREFOR

| FREESCALE SEMICONDUCTOR, INC. | KR | 350815 | METHOD FOR FORMING A DIELECTRI C HAVING IMPROVED PERFORMANCE |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 351574 | ELECTRONIC DEVICE ENCLOSURE IN CLUDING A CONDUCTIVE CAP AND S UBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 353337 | METHOD AND APPARATAUS FOR SEMI CONDUCTOR DEVICE OPTIMIZATION USING ON-CHIP VERIFICATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 354578 | SEMICONDUCTOR DEVICE HAVING A REDUCING/OXIDIZING CONDUCTIVE MATERIAL AND A PROCESS FOR FOR MING THE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 354932 | DATA PROCESSOR HAVING SHOW CYC LES ON A FAST MULTIPLEXED BUS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 354933 | METHOD AND APPARATUS FOR COMMU NICATING BETWEEN MASTER AND SL AVE ELECTRONIC DEVICES WHERE T HE SLAVE DEVICE MAY BE HAZARDO US |
| FREESCALE SEMICONDUCTOR, INC. | KR | 354934 | METHOD AND APPARATUS FOR IMPLE MENTING A BUS PROTOCOL HAVING IN-ORDER TERMINATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 355691 | III-V SEMICONDUCTOR STRUCTURE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 355692 | SEMICONDUCTOR DEVICE HAVING FI ELD ISOLATION AND A PROCESS FO R FORMING THE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 357803 | METHOD OF FABRICATING MULTI-CH IP PACKAGES |
| FREESCALE SEMICONDUCTOR, INC. | KR | 357806 | A CHEMICAL MECHANICAL POLISHING (CMP) SLURRY FOR COPPER AND METHOD OF USE IN INTEGRATED CIRCUIT MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 359395 | CIRCUIT FOR ELECTROSTATIC DISC HARGE (ESD) PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 361716 | LOW-PROFILE BALL-GRID ARRAY SE MICONDUCTOR PACKAGE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | KR | 362297 | CHEMICAL—MECHANICAL POLISHER AND A PROCESS FOR POLISHING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 365059 | MULTIBIT SHIFTING APPARATUS DA TA PROCESSOR USING SAME AND ME THOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 365060 | COMBINED MULTIPLIER/SHIFTER AN D METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 365061 | SEMICONDUCTOR DEVICE AND A PRO CESS FOR FORMING THE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 368191 | PROCESS FOR POLISHING AND ANAL YZING A LAYER OVER A PATTERNED SEMICONDUCTOR SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 369913 | SEMICONDUCTOR DEVICE HAVING MU LTIPLE OVERLAPPING ROWS OF BON D PADS WITH CONDUCTIVE INTERCO NNECTS AND METHOD OF PAD PLACE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 370308 | METHOD FOR PROBING A SEMICONDU CTOR WAFER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 372467 | A METHOD FOR MANUFACTURING A L OW DIELECTRIC CONSTANT INTERLE VEL INTEGRATED CIRCUIT STRUCTU RE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 374732 | SEMICONDUCTOR WAFER CONTACT SY STEM AND METHOD |

FOR CONTACTING A SEMICONDUCTOR WAFER

| FREESCALE SEMICONDUCTOR, INC. | KR | 375251 | DATA PROCESSING SYSTEM FOR EVA LUATING FUZZY LOGIC RULES AND METHOD THEREFOR |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 375252 | DATA PROCESSING SYSTEM HAVING A MULTI-FUNCTION SCALABLE PARALLEL INPUT/OUTPUT PORT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 376628 | CONDUCTIVE INTERCONNECT STRUCT URE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 376629 | DATA PROCESSOR WITH CIRCUIT FO R REGULATING INSTRUCTION THROU GHPUT AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 380697 | SEMICONDUCTOR DEVICE HAVING A BOND PAD AND A PROCESS FOR FOR MING THE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 381074 | FLEXIBLE PIN CONFIGURATION FOR USE IN A DATA PROCESSING SYST EM DURING A RESET OPERATION AN D METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 381316 | METHOD AND APPARATUS FOR PROCE SSING A SEMICONDUCTOR WAFER ON A ROBOTIC TRACK HAVING ACCESS TO IN SITU WAFER BACKSIDE PAR TICLE DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 381823 | ADJUSTABLE DEPTH/WIDTH FIFO BU FFER FOR VARIABLE WIDTH DATA T RANSFERS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 385383 | DATA PROCESSING SYSTEM FOR ACC ESSING AN EXTERNAL DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 385499 | DATA PROCESSOR WITH TRANSPAREN T OPERATION DURING A BACKGROUN D MODE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 386199 | METHOD AND APPARATUS FOR IMPRO VING UTILIZATION OF LIMITED RE SOURCES |
| FREESCALE SEMICONDUCTOR, INC. | KR | 387189 | PROTECTION CIRCUIT AND A CIRCUIT FOR A SEMICONDUCTOR-ON-INSULATOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 387193 | DATA PROCESSING SYSTEM FOR PER FORMING A TRACE FUNCTION AND M ETHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 387194 | INSULATED GATE FIELD EFFECT TR ANSISTOR HAVING SUBTHRESHOLD S WING AND METHOD FOR FABRICATIN G |
| FREESCALE SEMICONDUCTOR, INC. | KR | 388734 | PROGRAMMABLE CAPACITOR ARRAY A ND METHOD OF PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 389768 | SEMICONDUCTOR DEVICE WITH ESD PROTECTION AND A PROCESS FOR F ORMING THE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 392722 | METHOD FOR GENERICALLY DESCRIB ING MEASURED RESULTS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 393699 | PIEZORESISTIVE SENSOR AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | KR | 394166 | DATA PROCESSING SYSTEM FOR ACC ESSING AN EXTERNAL DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 394517 | METHOD FOR FORMING A TRENCH IS OLATION STRUCTURE IN AN INTEGR ATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 394897 | METHOD AND CIRCUIT FOR INITIAL IZING A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 396926 | METHOD AND APPARATUS FOR CALCU LATING A DIVIDER IN A DIGITAL PHASE LOCK LOOP |
| FREESCALE SEMICONDUCTOR, INC. | KR | 398982 | AUTOMOBILE AIRBAG SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 400949 | MULTI-STRAND SUBSTRATE FOR BAL L-GRID ARRAY |

ASSEMBLIES AND ME THOD

| FREESCALE SEMICONDUCTOR, INC. | KR | 402504 | MONOLITHIC THIN FILM RESONATOR LATTICE FILTER AND METHOD OF FABRICATION |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 402875 | MEDIA COMPATIBLE MICROSENSOR STRUCTURE AND METHODS OF MANUFA CTURING AND USING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 404992 | METHOD FOR PLANARIZING A SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 405843 | METHOD AND APPPARATUS FOR SELECTIVELY CONTROLLING INTERRUPT LATENCY IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 415871 | THIN FILM PIEZOELECTRIC ARRAYS WITH ENHANCED COUPLING AND FA BRICATION METHOD |
| FREESCALE SEMICONDUCTOR, INC. | KR | 417744 | AMPLITUDE ADJUST CIRCUIT AND M ETHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | KR | 418318 | WIREBONDLESS MODULE PACKAGE AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 420893 | MICROWAVE INTEGRATED CIRCUIT PASSIVE ELEMENT STRUCTURE AND METHOD FOR REDUCING SIGNAL PROP AGATION LOSSES |
| FREESCALE SEMICONDUCTOR, INC. | KR | 428526 | METHOD OF FORMING AN ISOLATION OXIDE FOR SILICON-ON-INSULATOR TECHNOLOGY |
| FREESCALE SEMICONDUCTOR, INC. | KR | 429319 | METHOD FOR MAKING AN ELECTRONI C COMPONENT HAVING AN ORGANIC SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 429321 | SEMICONDUCTOR CHEMICAL SENSOR DEVICE AND ETHOD OF FORMING A THERMOCOUPLE FOR A SEMICONDUCT OR CHEMICAL SENSOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 430696 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 436098 | METHOD AND APPARATUS FOR ACCES SING A CHIP- SELECTABLE DEVICE IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 439613 | METHOD FOR MOLDING USING AN IO N IMPLANTED HOLD |
| FREESCALE SEMICONDUCTOR, INC. | KR | 439781 | DATA PROCESSING SYSTEM FOR CON TROLLING EXECUTION OF A DEBUG FUNCTION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 439783 | MEMORY SUITABLE FOR OPERATION AT LOW POWER SUPPLY VOLTAGES A ND SENSE AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 440361 | DATA PROCESSING SYSTEM HAVING A SELF-ALIGNING STACK POINTER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 440651 | METHOD FOR FABRICATING A MONOL ITHIC SEMICONDUCTOR DEVICE WIT H INTEGRATED SURFACE MICROMACH INED STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | KR | 440655 | METHOD AND APPARATUS FOR ACCES SING A REGISTER IN A DATA PROC ESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 446564 | POWER REDUCTION INA A DATA PRO CESSING SYSTEM USING PIPELINE REGISTERS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 446996 | PRECISION CURRENT LIMIT CIRCUI T |
| FREESCALE SEMICONDUCTOR, INC. | KR | 453118 | DRAM REFRESH WHILE NOT A BUS M ASTER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 456649 | PRECONDITIONER FOR A POLISHING PAD AND METHOD FOR USING THE SAME |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 457478 | METHOD FOR ACCESSING MEMORY BY SPECULATIVELY ACTIVATING A CH IP SELECT SIGNAL |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 459738 | INTEGRATED CIRCUIT INPUT-OUTPU T PROCESSOR HAVING IMPROVED TI MER CAPABILITY |
| FREESCALE SEMICONDUCTOR, INC. | KR | 465356 | CONSTANT HIGH Q VOLTAGE CONTRO LLED OSCILLATOR AND METHOD FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 466902 | SINGLE GATE NONVOLATILE MEMORY CELL AND METHOD FOR ACCESSING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 467123 | METHOD FOR REDUCING PARTICLES ON A SUBSTRATE USING CHUCK CLE ANING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 470240 | METHOD FOR MULTIPLEXED JOINING OF SOLDER BUMPS TO VARIOUS SUBSTRATES DURING ASSEMBLY OF AN INTEGRATED CIRCUIT PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 470516 | DISTRIBUTED TAG CACHE MEMORY S YSTEM AND METHOD FOR STORING D ATA IN THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 475324 | SELECTIVELY FILLED ADHESIVE FILM CONTAINING A FLUXING AGENT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 476483 | NON-VOLATILE REGISTER AND METH OD FOR ACCESSING DATA THEREIN |
| FREESCALE SEMICONDUCTOR, INC. | KR | 476484 | PROCESS FOR POLISHING DISSIMIL AR CONDUCTIVE LAYER IN A SEMI CONDUCTOR DEVICE |
| REESCALE SEMICONDUCTOR, INC. | KR | 479243 | METHOD FOR MAKING SEMICONDUCTO R DEVICES HAVING ELECTROPLATED LEADS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 484330 | A SERIAL INTERFACE WITH REGIST ER SELECTION WHICH USES CLOCK COUNTING, CHIP SELECT PULSING, AND NO ADDRESS BITS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 484551 | SEMICONDUCTOR PACKAGE BOND POS T CONFIGURATION AND METHOD OF MANUFACTURING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | KR | 484584 | INTEGRATED CIRCUIT MEMORY USIN G FUSIBLE LINKS IN A SCAN CHAI N |
| FREESCALE SEMICONDUCTOR, INC. | KR | 486396 | METHOD AND APPARATUS FOR TESTI NG A SEMICONDUCTO WAFER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 489157 | SEMICONDUCTOR DEVICE AND METHOD FOR MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 489452 | LED DISPLAY PACKAGING WITH SUB STRATE REMOVAL ANI METHOD OF F ABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 490180 | INTEGRATED CIRCUIT HAVING A DU MMY STRUCTURE AND METHOD OF MA KING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 492041 | DATA PROCESSING SYSTEM HAVING A CACHE AND METHOI THERFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 495457 | INTEGRATED CIRCUIT MEMORY WITH MULTIPLEXED REDUNDANT COLUMN DATA PATH |
| FREESCALE SEMICONDUCTOR, INC. | KR | 495960 | METHOD FOR MAKING A SEMICONDUC TOR DEVICE HAVING ANTI-REFLECT IVE COATING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 498789 | BUFFER CIRCUIT HAVING VARIABLE OUTPUT IMPEDANCE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 501962 | ELECTRICALLY PROGRAMMABLE MEMO RY AND METHOD (PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 503693 | METHOD OF GROWING GALLIUM NITR IDE ON A SPINEL |

SUBSTRATE

| FREESCALE SEMICONDUCTOR, INC. | KR | 504413 | APPARATUS AND METHOD FOR ETCHING A DIELECTRIC LAYER OVER A SEMICONDUCTOR SUBSTRATE |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 504969 | INTEGRATED CIRCUIT HAVING STAN DBY CONTROL FOR MEMORY AND MET HOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | KR | 505513 | PROCESS FOR FORMING A SEMICOND UCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 507516 | CURRENT LIMIT CONTROLLER FOR A N AIR BAG DEPLOYMENT SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 509659 | PROCESS FOR POLISHING A SEMICO NDUCTOR DEVICE SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 511141 | METHOD OF CHEMICAL MECHANICAL PLANARIZATION USING A WATER RI NSE TO PREVENT PARTICLE CONTAM INATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 513409 | APPARATUS AND METHOD FOR PATTERNING A SURFACE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 514701 | SEMICONDUCTOR TILING STRUCTURE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 518096 | CONTROL GATE DRIVER CIRCUIT FO R A NON-VOLATILE MEMORY AND ME MORY USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 519862 | CIRCUIT AND METHOD FOR EVALUAT ING FUZZY LOGIC RULES |
| FREESCALE SEMICONDUCTOR, INC. | KR | 528269 | METHOD AND APPARATUS FOR PERFO RMING MICROPROCESSOR INTEGER DIVISION OPERATIONS USING FLOAT ING POINT HARDWARE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 528553 | OPTICAL SEMICONDUCTOR COMPONEN T AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 528559 | INTERCONNECT STRUCTURE IN A SEMICONDUCTOR DEVICE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 530431 | PROCESS FOR FORMING A SEMICOND UCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 0544245 | APPARATUS FOR RECEIVING AND RECOVERING FREQUENCY SHIFT KEYED SYMBOLS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 544805 | A SYSTEM FOR INITIALIZING A DISTRIBUTED COMPUTER SYSTEM AND A METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | KR | 546227 | FAST START-UP PROCESSOR CLOCK GENERATION METHOD AND SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 546943 | METHOD FOR DEPOSITING A DIFFUSION BARRIER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 548973 | CIRCUIT AND METHOD OF LIMITING LEAKAGE CURRENT IN A MEMORY C IRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 553626 | SURFACE MOUNTABLE FLEXIBLE INTERCONNECT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 559062 | SEMICONDUCTOR COMPONENT AND ME THOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 562695 | METHOD AND APPARATUS FOR IN-LI NE MEASURING BACKSIDE WAFER LE VEL CONTAMINATION OF A SEMICON DUCTOR WAFER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 563009 | METHOD FOR REDUCING PARTICLES DEPOSITED ONTO A SEMICONDUCTOR WAFER DURING PLASMA PROCESSIN G |
| FREESCALE SEMICONDUCTOR, INC. | KR | 563012 | METHOD AND APPARATUS FOR INTER FACING A PROCESSOF TO A COPROC ESSOR |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 563748 | PROCESS FOR FORMING A SEMICOND UCTOR DEVICE |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 564070 | SENSE AMPLIFIER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 565018 | ETCHING APPARATUS AND METHOD OF ETCHING A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 569614 | METHOD FOR MANUFACTURING A SEM ICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 572813 | SEMICONDUCTOR DEVICE HAVING A SUB-CHIP-SCALE PACKAGE STRUCTU RE AND METHOD FOR FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 573175 | METHOD OF FORMING A SEMICONDUC TOR DEVICE HAVING DUAL INLAID STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 573501 | VARIABLE CAPACITOR AND METHOD FOR FABRICATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 574181 | MEMORY DEVICE WITH FAST WRITE RECOVERY AND RELATED WRITE REC OVERY METHOD |
| FREESCALE SEMICONDUCTOR, INC. | KR | 576675 | SEMICONDUCTOR DEVICE AND ALIGNMENT METHOD |
| FREESCALE SEMICONDUCTOR, INC. | KR | 576987 | A METHOD FOR MANUFACTURING AND DESIGNING AN ELECTRONIC DEVICE AND ELECTRONIC APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 577620 | UNIVERSAL TRANSPORT APPARATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | KR | 578259 | ELECTRONIC DEVICE AND METHOD F OR FORMING A MEMBRANNE FOR AN ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 585563 | PROCESS FOR FORMING A SEMICOND UCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 588790 | METHOD AND APPARATUS FOR AFFEC TING SUBSEQUENT INSTRUCTION PR OCESSING IN A DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 589865 | SEMICONDUCTOR DEVICE AND A PRO CESS FOR FORMING THE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 591026 | INTEGRATED CIRCUIT MEMORY HAVI NG A FUSE DETECT CIRCUIT AND M ETHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 596947 | METHOD AND APPARATUS FOR TRANS FERRING DATA ON A SPLIT BUS IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 597325 | POINT OF USE DILUTION TOOL AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | KR | 597328 | DATA PROCESSING SYSTEM HAVING BRANCH CONTROL AND METHOD THER EOF |
| FREESCALE SEMICONDUCTOR, INC. | KR | 599326 | SWITCHED CAPACITOR CIRCUIT AND METHOD FOR REDUCING SAMPLING NOISE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 601745 | COMPUTER INSTRUCTION WHICH GEN ERATES MULTIPLE RESULTS OF DIF FERENT DATA TYPES TO IMPROVE S OFTWARE EMULATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 605051 | METHOD AND APPARATUS FOR VISUALLY INSPECTING AN OBJECT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 606578 | CHEMICAL MECHANICAL PLANARIZATION SYSTEM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 616767 | RECEIVER WITH IMPROVED DIGITAL INTERMEDIATE TO BASE BAND DEMODULATOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 617884 | PULSE WIDTH MODULATOR (PWM) SY STEM WITH LOW COST DEAD TIME D ISTORTION CORRECTION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 620258 | MULTI-WAY CACHE APPARATUS AND METHOD |

| FREESCALE SEMICONDUCTOR, INC. | KR | 621814 | INTEGRATED CIRCUIT INTERCONNEC T METHOD AND APPARATUS |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 627986 | SYNCHRONOUS PIPELINED BURST ME MORY AND METHOD FOR OPERATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 630247 | METHOD OF PROBING A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 632198 | METHOD AND APPARATUS FOR EXTEN DING FATIGUE LIFE OF SOLDER JO INTS IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 632712 | METHOD FOR FORMING INTERCONNEC T BUMPS ON A SEMICONDUCTOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 634030 | QUANTUM RANDOM ADDRESS MEMORY WITH MAGNETIC READOUT AND/OR N ANO-MEMORY ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 639049 | A MEMORY DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | KR | 647446 | CIRCUIT AND METHOD FOR INTERLEAVING A DATA STREAM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 647995 | METHOD FOR FORMING A SEMICONDU CTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 647996 | PROCESS FOR FORMING A CONDUCTI VE STRUCTURE AND A SEMICONDUCT OR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 659918 | METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING A LAYER DEPOSITED BY VARYING FLOW OF REACTANTS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 665484 | PROGRAMMABLE DELAY CONTROL IN A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | KR | 675494 | SEMICONDUCTOR DEVICE AND PROCESS FOR MANUFACTURING AND PACAKAGING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 676213 | METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE HAVING A STABLE CRYSTALLINE INTERFACE WITH SILICON |
| FREESCALE SEMICONDUCTOR, INC. | KR | 678354 | METHOD AND DATA PROCESSING SYS TEM FOR USING QUICK DECODE INS TRUCTIONS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 678877 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 680519 | MEMORY UTILIZING A PROGRAMMABLE DELAY TO CONTROL ADDRESS BUFFERS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 682286 | LINEAR CAPACITOR STRUCTURE IN A CMOS PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 682818 | REFERENCE CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | KR | 688041 | VOLTAGE VARIABLE CAPACITOR WITH IMPROVED C-V LINEARITY |
| FREESCALE SEMICONDUCTOR, INC. | KR | 688311 | CIRCUIT AND METHOD OF FREQUENC Y SYNTHESIZER CONTROL WITH A S ERIAL PERIPHERAL INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 690225 | DATA PROCESSOR SYSTEM AND INST RUCTION SYSTEM USING GROUPING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 695662 | A PROCESS FOR FORMING A SEMICONDUCTOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 697714 | METHOD OF PREPARING CRYSTALLIN E ALKALINE EARTH METAL OXIDES ON A SI SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 705301 | MEMORY CELL, METHOD OF FORMATION, AND OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 707120 | METHOD OF FORMING A COPPER LAY ER OVER A SEMICONDUCTOR LAYER |
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FREESCALE SEMICONDUCTOR, INC.

| FREESCALE SEMICONDUCTOR, INC. | KR | 711956 | GAIN CONTROLLER FOR CIRCUIT HAVING IN-PHASE AND QUADRATURE CHANNELS, AND METHOD |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 714661 | PROCESS FOR FORMING A SEMICOND UCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 714668 | LOAD CAPACITANCE COMPENSATED BUFFER AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | KR | 717973 | CIRCUIT AND METHOD FOR REDUCIN G PARASITIC BIPOLAR EFFECTS DU RING ELECTROSTATIC DISCHARGES |
| FREESCALE SEMICONDUCTOR, INC. | KR | 718821 | STRESS COMPENSATION COMPOSITION AND SEMICONDUCTOR COMPONENT FORMED USING THE STRESS COMPENSATION COMPOSITION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 719384 | LOW PROFILE INTERCONNECT STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 722177 | SEMICONDUCTOR DEVICE AND A PROCESS FOR DESIGNING A MASK |
| FREESCALE SEMICONDUCTOR, INC. | KR | 733733 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 733736 | DUAL METAL GATE TRANSISTORS FOR CMOS PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 734158 | FLEXIBLE INTERRUPT CONTROLLER THAT INCLUDES AN INTERRUPT FORCE REGISTER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 736057 | DUAL DIGITAL LOW IF COMPLEX RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 737174 | SEMICONDUCTOR DEVICE, A PROCESS FOR A SEMICONDUCTOR DEVICE, AND A PROCESS FOR MAKING A MASKING DATABASE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 738242 | METHOD AND APPARATUS FOR A CALIBRATED FREQUENCY MODULATION PHASE LOCKED LOOP |
| FREESCALE SEMICONDUCTOR, INC. | KR | 748070 | PEAK PROGRAM CURRENT REDUCTION APPARATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | KR | 748377 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE AND A CONDUCTIVE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 749290 | UV CURE PROCESS AND TOOL FOR LOW K FILM FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 754759 | CONVERSION BETWEEN OPTICAL AND RADIO FREQUENCY SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 756587 | METHOD OF FORMING A SEMICONDUC TOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 757695 | COMPONENT AND METHOD FOR MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 761226 | METHOD FOR FORMING A BARRIER L AYER FOR USE IN A COPPER INTER CONNECT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 761232 | SEMICONDUCTOR DEVICE USING A BARRIER LAYER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 761671 | EDGE GROWTH HETEROEPITAXY |
| FREESCALE SEMICONDUCTOR, INC. | KR | 762111 | SEMICONDUCTOR DEVICE AND A PROCESS FOR FORMING THE SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 763173 | METHOD AND APPARATUS FOR CONFIGURING A DATA PROCESSING SYSTEM AFTER RESET |
| FREESCALE SEMICONDUCTOR, INC. | KR | 766732 | DEVICE AND METHOD FOR PERFORMING HIGH-SPEED LOW OVERHEAD CONTEXT SWITCH |
| FREESCALE SEMICONDUCTOR, INC. | KR | 767615 | ACCELERATION SENSOR AND METHOD OF MANUFACTURE |

| FREESCALE SEMICONDUCTOR, INC. | KR | 777147 | METHOD OF MANUFACTURING A SEMICONDUCTOR |
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| | | | COMPONENT AND CHEMICAL-MECHANICAL POLISHING SYSTEM THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 779869 | ELECTRONIC COMPONENT AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 785646 | MULTI-MODE RADIO COMMUNICATIONS DEVICE USING A SHARED CLOCK COURCE. |
| FREESCALE SEMICONDUCTOR, INC. | KR | 794155 | SEMICONDUCTOR DEVICE HAVING PASSIVE ELEMENTS AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 794476 | MECHANICALLY ROBUST PAD INTERFACE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 794482 | ULTRA-LATE PROGRAMMING ROM AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 795315 | APPARATUS FOR RECEIVING AND PROCESSING A RADIO FREQUENCY SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | KR | 801863 | ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 809860 | ELECTRO-OPTIC STRUCTURE AND PROCESS FOR FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 810932 | ELECTRIC DRIVER CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | KR | 814270 | INSTRUCTION CACHE AND METHOD FOR REDUCING MEMORY CONFLICTS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 815063 | INTEGRATED CIRCUIT HVING A BALANCED TWIST FOR DIFFERENTIAL SIGNAL LINES |
| FREESCALE SEMICONDUCTOR, INC. | KR | 815068 | METHOD AND APPARATUS FOR DETECTING AND COMPENSATING DIGITAL LOSSES IN A COMMUNICATIONS NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | KR | 818902 | METHOD AND APPARATUS FOR MANUFACTURING AN INTERCONNECT STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 819720 | DATA PROCESSING SYSTEM HAVING AN ON-CHIP BACKGROUND DEBUG SYSTEM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 822228 | SEMICONDUCTOR DEVICE AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 822232 | SEMICONDUCTOR DEVICE AND PROCESS FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 823464 | METHOD FOR UNIFORM POLISH IN MICROELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 826464 | APPARATUS FOR REDUCING DC OFFSET IN A RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 827216 | MICROELECTRONIC PIEZOELECTRIC STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 829403 | METHOD AND APPARATUS FOR ALIGNING A WAVEGUIDE TO A DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 830361 | ACTIVE BIAS CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 835130 | OSCILLATOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 840137 | TRANSMITTER FOR A CONTROLLED- SHAPE SWITCHED SIGNAL ON A COMMUNICTION LINE. |
| FREESCALE SEMICONDUCTOR, INC. | KR | 849377 | LITHOGRAPHIC TEMPLATE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 856336 | REAL-TIME PROCESSOR DEBUG SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 857407 | METHOD FOR UNIFORM POLISH IN MICROELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 864192 | METHOD AND DEVICE FOR CREATING AND USING PRE- INTERNALIZED PROGRAM FILES |
| FREESCALE SEMICONDUCTOR, INC. | KR | 867565 | SEMICONDUCTOR DEVICE AND A METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 869448 | HIGH K DIELECTRIC FILM AND METHOD FOR MAKING |

| FREESCALE SEMICONDUCTOR, INC. | KR | 870259 | AN INTEGRATED CIRCUIT USING A REFLECTIVE MASK |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 879233 | SELECTIVE METAL OXIDE REMOVAL |
| FREESCALE SEMICONDUCTOR, INC. | KR | 888356 | PROCESSOR HAVING SELECTIVE BRANCH PREDICTION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 890346 | SWITCHING AMPLIFIER HAVING DIGITAL CORRECTION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 890716 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND SEMICONDUCTOR COMPONENT THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | KR | 890874 | TEMPERATURE-CONTROLLED CHUCK AND METHOD FOR CONTROLLING THE TEMPERATURE OF A SUBSTANTIALLY FLAT OBJECT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 894427 | METHOD AND APPARATUS FOR A CLOCK CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 895964 | LOW PROFILE INTEGRATED MODULE INTERCONNECTS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 896141 | METHOD OF FORMING A BOND PAD AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | KR | 899951 | SYSTEM AND METHOD FOR CONTROLLING BUS ARBITRATION DURING CACHE MEMORY BURST CYCLES |
| FREESCALE SEMICONDUCTOR, INC. | KR | 0901933 | THREE INPUT SENSE AMPLIFIER AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 902765 | FIRST-IN FIRST-OUT MEMORY SYSTEM AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | KR | 904956 | PACKAGED SEMICONDUCTOR WITH MULTIPLE ROWS OF BOND PADS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 910071 | MODE CONTROLLER FOR SIGNAL ACQUISITION AND TRACKING IN AN ULTRA WIDEBAND COMMUNICATIONS SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 926002 | SEMICONDUCTOR PACKAGE DEVICE AND METHOD OF FORMATION AND TESTING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 926243 | AN OPTO-COUPLING DEVICE STRUCTURE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 926249 | AN OPTO-COUPLING DEVICE STRUCTURE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | NL | 1009157 | PROCESS FOR DEPOSITING A LAYER OF MATERIAL ON A SUBSTRATE AN D A PLATING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | FR | 1069605 | METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE INCLUDING A METAL OXIDE INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | GB | 1069605 | METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE INCLUDING A METAL OXIDE INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | IT | 1069605 | METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE INCLUDING A METAL OXIDE INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | IT | 1299444 | PROCESS FOR DEPOSITING A LAYER OF MATERIAL ON A SUBSTRATE AN D A PLATING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | FR | 1740922 | MOTION SENSING FOR TIRE PRESSURE MONITORING |
| FREESCALE SEMICONDUCTOR, INC. | GB | 1740922 | MOTION SENSING FOR TIRE PRESSURE MONITORING |
| FREESCALE SEMICONDUCTOR, INC. | IT | 1740922 | MOTION SENSING FOR TIRE PRESSURE MONITORING |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 01822793 | DATA PROCESSING SYSTEM HAVING AN ON-CHIP BACKGROUND DEBUG SYSTEM AND METHOD THEREFOR |
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| FREESCALE SEMICONDUCTOR, INC. | FR | 2067255 | METHOD OF CONTROL SLOPE REGULATION AND CONTROL SLOPE REGULATION APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | GB | 2067255 | METHOD OF CONTROL SLOPE REGULATION AND CONTROL SLOPE REGULATION APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | CA | 2135794 | PROCESS FOR FORMING TIN- BISMUTH SOLDER CONNECTION HAVING IMPROVED HIGH TEMPERATURE PROPERTIES |
| FREESCALE SEMICONDUCTOR, INC. | GB | 2289188 | TELEPHONE LINE INTERFACE CIRCU IT |
| FREESCALE SEMICONDUCTOR, INC. | GB | 2295829 | METHOD AND APPARATUS FOR PLATI NG METALS |
| FREESCALE SEMICONDUCTOR, INC. | GB | 2313724 | VOLTAGE DETECTOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | GB | 2325546 | ELECTRICALLY PROGRAMMABLE MEMO RY AND METHOD O PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | GB | 2338827 | ELECTRONIC ASSEMBLY PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | GB | 2411059 | AN APPARATUS FOR VOLTAGE LEVEL SHIFTING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 02819149.8 | MULTI-RATE ANALOG-TO-DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2838160 | SEMICONDUCTOR DEVICE HAVING X- SHAPED DIE SUPPORT MEMBER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2993446 | APPARATUS AND METHOD FOR DYNAM ICALLY MIXING SLURRY FOR CHEMICAL MECHANICAL POLISHING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2998555 | SIGMA-DELTA MODULATOR WITH IMPROVED TONE REJECTION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3055426 | EEPROM CELL WITH ISOLATION TRANSISTOR AND METHODS FOR MAKING AND OPERATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3183093 | A CONTINUOUS TIME COMMON MODE FEEDBACK AMPLIFIED |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3196203 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3204287 | METHOD AND APPARATUS FOR NOISE BURST DETECTION IN SIGNAL PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3221486 | SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3282090 | PIEZORESISTIVE SENSOR AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3300839 | A SEMICONDUCTOR DEVICE AND METHOD FOR MAKING AND USING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3305664 | SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3308476 | A METHOD FOR POLISHING A SEMICONDUCTOR WAFER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3320565 | AN OUTPUT CIRCUIT AND METHOD O F OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3326112 | PROCESS FOR DEPOSITING A LAYER OF MATERIAL ON A SUBSTRATE AND A PLATING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3332516 | THERMALLY ENHANCED SEMICONDUCT OR DEVICE HAVING EXPOSED BACKS IDE AND METHOD FOR MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3342662 | PULSE WIDTH MODULATOR (PWM) SY STEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3376285 | SURFACE MOUNTABLE FLEXIBLE INTERCONNECT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3396579 | N-TYPE HIGFET AND METHOD |
| EDEEGGALE GENTION DISCHOOL INC | | 0.400000 | |

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FREESCALE SEMICONDUCTOR, INC.

| FREESCALE SEMICONDUCTOR, INC. | JP | 3447477 | METHOD FOR POLISHING A SEMICON DUCTOR SUBSTRATE |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 3466785 | SEMICONDUCTOR DEVICE AND METHO D OF FORMING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3493088 | MULTI-STRAND SUBSTRATE FOR BALL-GRID ARRAY ASSEMBLIES AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3498058 | MICRO ELECTRO-MECHANICAL SYSTEM SENSOR WITH SELECTIVE ENCAPSULATION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3506489 | REVERSE BATTERY PROTECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3531983 | RESISTOR STRUCTURE AND METHOD OF SETTING A RESISTANCE VALUE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3559432 | METHOD OF FORMING A SEMICONDUC TOR METALLIZATION SYSTEM AND S TRUCTURE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3576325 | A DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3588275 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3590535 | METHOD AND OUTPUT BUFFER WITH PROGRAMMABLE BIAS TO ACCOMODAT E MULTIPLE SUPPLY VOLTAGES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3616444 | SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3621752 | III-V SEMICONDUCTOR STRUCTURE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3621950 | A METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3626788 | FREQUENCY INVERSION SCRAMBLER WITH INTEGRATED HIGH-PASS FILT ER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3627158 | LOW-PROFILE BALL-GRID ARRAY SEMICONDUCTOR PACKAGE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3629337 | METHOD OF FABRICATING A FLIP C HIP SEMICONDUCTOR DEVICE HAVIN G AN INDUCTOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3630739 | A LOCAL AREA NETWORK SYSTEM AN D METHOD OF SWITCHING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3663039 | MEMORY SUITABLE FOR OPERATION AT LOW POWER SUPPLY VOLTAGES A ND SENSE AMPLIFIER THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3673559 | PROCESS FOR POLISHING A LAYER OVER A PATTERNED SEMICONDUCTOR SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3681182 | EXTENSIBLE CENTRAL PROCESSING UNIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3684295 | METHOD AND APPARATAUS FOR SEMI CONDUCTOR DEVICE OPTIMIZATION USING ON-CHIP VERIFICATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3694394 | A METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3694546 | METHOD FOR PROBING A SEMICONDUCTOR WAFER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3702023 | A PRECONDITIONER FOR A POLISHI NG PAD AND METHOD FOR USING TH E SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3705453 | DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3707581 | A DATA PROCESSING SYSTEM HAVIN G A SELF-ALIGNING STACK POINTE R AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3709508 | MONOLITHIC HIGH FREQUENCY INTEGRATED CIRCUIT STRUCTURE AND METHOD OF MANUFACTURING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3723700 | METHOD AND APPARATUS FOR TRANSFERRING DATA OVER |

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| FREESCALE SEMICONDUCTOR, INC. | JP | 3725607 | ELECTRONIC DIE PACKAGE ASSEMBL Y HAVING A SUPPORT AND METHOD |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 3739431 | AN INTEGRATED CIRCUIT AND A DA TA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3740250 | METHOD AND APPARATUS FOR DETER MINING WAIT STATES ON A PER CY CLE BASIS IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3745824 | PRECISION CURRENT LIMIT CIRCUI T |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3746809 | TELEPHONE LINE INTERFACE CIRCU IT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3755669 | A METHOD FOR ROUTING A NUMBER OF NETS AND ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3759647 | APPARATUS AND METHOD FOR PERFORMING BOTH 24 BIT AND 16 BIT ARITHMETIC |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3768601 | FLUXLESS FLIP-CHIP BOND AND A METHOD FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3769339 | MULTI-RATE DIGITAL FILTER APPA RATUS AND METHOD FOR SIGMA-DEL TA CONVERSION PROCESSES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3778640 | SEMICONDUCTOR HEATER AND METHO D FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3787385 | METHOD AND APPPARATUS FOR SELE CTIVELY CONTROLLING INTERRUPT LATENCY IN A DATA PROCESSING S YSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3790626 | METHOD AND APPARATUS FOR FETCH ING AND ISSUING DUAL-WORD OR M ULTIPLE INSTRUCTIONS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3805820 | METHOD AND APPARATUS FOR A FRE QUENCY DETECTION CIRCUIT FOR U SE IN A PHASE LOCKED LOOP |
| FREESCALE SEMICONDUCTOR, INC. | CN | 03815342.4 | COMMUNICATION APPARATUS INCLUDING DRIVER MEANS FOR APPLYING A SWITCHED SIGNAL TO A COMMUNICATION LINE WITH A CONTROLLED SLEW RATE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3816932 | EXTENSIBLE CENTRAL PROCESSING UNIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3817327 | METHOD AND APPARATUS FOR ACCES SING A CHIP- SELECTABLE DEVICE IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3820375 | DIGITAL-TO-ANALOG CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3827418 | CONTROL GATE DRIVER CIRCUIT FO R A NON-VOLATILE MEMORY AND ME MORY USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3827749 | MEMORY HAVING BIT LINE LOAD WITH AUTOMATIC BIT LINE PRECHARGE AND EQUALIZATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3830236 | METHOD AND DATA PROCESSING SYS TEM FOR USING QUICK DECODE INS TRUCTIONS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3834074 | III-V COMPLEMENTARY HETEROSTRU CTURE DEVICE WITH COMPATIBLE N ON-GOLD OHMIC CONTACTS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3836248 | ANALOG/DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3837194 | CIRCUIT AND METHOD FOR RECONST RUCTING A PHASE CURRENT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3846939 | A DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3850063 | METHOD AND APPARATUS FOR DETER MINING A FEEDBACK DIVIDER IN A PHASE LOCK LOOP |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3853844 | ELECTRICALLY PROGRAMMABLE MEMO RY METHOD OF PROGRAMMING AND M ETHOD OF READING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3853851 | A DATA PROCESSING SYSTEM |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 3854651 | COMPLEMENTARY HETEROJUNCTION S EMICONDUCTOR DEVICE |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 3871381 | BUFFER CIRCUIT HAVING VARIABLE OUTPUT IMPEDANCE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3874816 | TRENCH ISOLATION STRUCTURE IN AN INTEGRATED CIRCUIT AND METH OD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3881401 | METHOD AND APPARATUS OF AN OPE RATIONAL AMPLIFIER WITH A WIDE DYNAMIC RANGE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3881402 | AMPLITUDE ADJUST CIRCUIT AND M ETHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3881409 | VERTICALLY INTEGRATED SENSOR S TRUCTURE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3886167 | A LOCK DETECT CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3896204 | METHOD FOR SELECTING A REGISTE R STORAGE DESTINATION FOR A SE RIALLY-PROVIDED DATA STREAM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3899157 | TUNNEL TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3901759 | DATA PROCESSOR AND METHOD THER EFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3909116 | SINGLE GATE NONVOLATILE MEMORY CELL AND METHOD FOR ACCESSING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3913321 | CURRENT LIMIT CONTROLLER FOR A N AIR BAG DEPLOYMENT SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3917672 | A BUS PROTOCAL AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3917697 | PROCESS FOR UNDERFILLING A FLI P-CHIP SEMICONDUCTOR DEVICE AND A DEVICE MADE THEREBY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3920447 | INSULATOR COMPOUND SEMICONDUCT OR INTERFACE STRUCTURE AND MET HODS OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3920994 | METHOD AND APPARATUS FOR INTER FACING A PROCESSOR TO A COPROC ESSOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3928781 | METHOD OF SELECTING CELL FOR AN INPUT CODE IN DIGITAL-ANALOG CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3928898 | INTEGRATED IMAGE REJECT MIXER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3930990 | COMPUTER SYSTEM WITH AN INTERFACE BETWEEN A MEMORY AND PERIPHERAL DEVICES, AND METHOD TO SELECT A COMMUNICATION PARAMETER SET |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3937191 | SEMICONDUCTOR CHEMICAL SENSOR DEVICE AND METHOD OF FORMING A THERMOCOUPLE FOR A SEMICONDUC TOR CHEMICAL SENSOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3941127 | MICROWAVE INTEGRATED CIRCUIT P ASSIVE ELEMENT STRUCTURE AND M ETHOD FOR REDUCING SIGNAL PROP AGATION LOSSES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3943616 | DATA PROCESSOR WITH TRANSPARENT OPERATION DURING A BACKGROUND MODE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3949771 | SEMICONDUCTOR DEVICE AND METHO D OF FORMING A SEMICONDUCTOR D EVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3953554 | MONOLITHIC THIN FILM RESONATOR LATTICE FILTER AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3953563 | METHOD OF FORMING AN ISOLATION OXIDE FOR SILICON- |

ON-INSULATO R TECHNOLOGY

| FREESCALE SEMICONDUCTOR, INC. | JP | 3953590 | ELECTRONIC CIRCUIT FOR CONVERT ING A DIFFERENTIAL INPUT VOLTA GE TO A SINGLE-ENDED OUTPUT VO LTAGE RESISTOR NETWORK |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 3954141 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3958546 | BUFFER CONTROLLING SYSTEM AND BUFFER CONTROLLABLE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3962449 | METHOD FOR COUPLING SUBSTRATES AND STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3968148 | INTEGRATED CIRCUIT MEMORY USIN G FUSIBLE LINKS IN A SCAN CHAI N |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3968304 | APPARATUS FOR RECEIVING AND RECOVERING FREQUENCY SHIFT KEYED SYMBOLS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3977901 | METHOD FOR FABRICATING A COMPO NENT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3992771 | A METHOD FOR OPERATING A DIGIT AL DATA PROCESSOR TO PERFORM A FUZZY RULE EVALUATION OPERATI ON |
| FREESCALE SEMICONDUCTOR, INC. | JP | 3992855 | CIRCUIT FOR ELECTROSTATIC DISC HARGE (ESD) PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4001960 | METHOD FOR FORMING A SEMICONDU CTOR DEVICE HAVING A NITRIDED OXIDE DIELECTRIC LAYER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4002554 | SYSTEM FOR EXPANDED INSTRUCTION ENCODING AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4002644 | CLAMP DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4008047 | SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4009353 | NON-DESTRUCTIVE METHOD OF DETE RMINING SUBSTRATE TILT WITHIN A PACKAGED SEMICONDUCTOR COMPO NENT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4010591 | METHOD FOR MAKING AN ELECTRONI C COMPONENT HAVING AN ORGANIC SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4017679 | PORTABLE ELECTRONIC DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4020867 | ASYNCHRONOUS SAMPLING RATE CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4022272 | SWITCHED CAPACITOR GAIN STAGE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4024306 | METHODS AND CIRCUITS FOR DYNAM ICALLY ADJUSTING A SUPPLY VOLT AGE AND/OR A FREQUENCY OF A CL OCK SIGNAL IN A DIGITAL CIRCUI T |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4030614 | FULL COLOR LIGHT EMITTING DIOD E DISPLAY ASSEMBLY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4040704 | DATA PROCESSING SYSTEM AND MET HOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4042978 | MULTI-RATE ANALOG-TO-DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4043503 | METHOD AND APPARATUS FOR REDUCED POWE CONSUMPTION ADC/DAC CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4043844 | DRIVER FOR LIGHT EMITTING DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4053611 | SYNCHRONOUS DEMODULATOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4056394 | METHOD OF PREPARING COPPER METALLIZATION DIE FOR WIRE BONDING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4057114 | DATA PROCESSING SYSTEM HAVING A CACHE AND METHOD THERFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4064503 | TYRE PRESSURE MONITORING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4065582 | AUTOMOBILE AIRBAG SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4073980 | CONSTANT HIGH Q VOLTAGE CONTRO LLED OSCILLATOR AND METHOD FOR MAKING |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 4076946 | FIRST-IN FIRST-OUT MEMORY SYSTEM AND METHOD THEREOF |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 4080028 | ACCELERATION SENSING DEVICE AN D METHOD OF OPERATION AND FORM ING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4083116 | LOW LEAKAGE LOCAL OSCILLATOR SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4083835 | NON-VOLATILE MEMORY CELL AND M ETHOD OF PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4083841 | METHOD FOR PACKAGING SEMICONDU CTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4086951 | PROCESS FOR FORMING A SEMICOND UCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4087336 | ACTIVE BIAS CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4088418 | COMPUTER INSTRUCTION WHICH GENERATES MULTIPLE RESULTS OF DIFFERENT DATA TYPES TO IMPROVE SOFTWARE EMULATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4091669 | METHOD OF FABRICATING MULTI-CH IP PACKAGES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4094073 | METHOD FOR FORMING SEMICONDUCT OR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4094075 | WIREBONDLESS MODULE PACKAGE AN D METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4098241 | METHOD AND APPARATUS FOR INTERFACING A PROCESSOR TO A COPROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4108802 | AN AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4117050 | SMARTCARD AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4121454 | METHOD AND APPARATUS FOR A CLOCK CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4121527 | A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4121956 | LOW POWER CYCLIC A/D CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4124508 | III-V EPITAXIAL WAFER PRODUCTI ON |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4138036 | METHOD FOR FABRICATING A MONOL ITHIC SEMICONDUCTOR DEVICE WIT H INTEGRATED SURFACE MICROMACH INED STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4139332 | INCREMENTAL-DELTA ANALOGUE-TO-DIGITAL CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4139771 | SYSTEM AND METHOD FOR CONTROLLING BUS ARBITRATION DURING CACHE MEMORY BURST CYCLES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4145146 | DATA PROCESSING SYSTEM HAVING AN ON-CHIP BACKGROUND DEBUG SYSTEM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4153361 | IMAGE DISPLAY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4159471 | TRANSISTOR METAL GATE STRUCTURE THAT MINIMIZES NON-PLANARITY EFFECTS AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4159651 | INSULATED GATE BIPOLAR TRANSIS TOR WITH REDUCED ELECTRIC FIEL DS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4162272 | METHOD AND APPARATUS FOR PLATI NG METALS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4162656 | APPARATUS AND METHOD FOR POWER MANAGEMENT IN A TIRE PRESSURE MONITORING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4168073 | METHOD FOR FORMING A TRENCH ISOLATION STRUCTURE IN AN INTEGR ATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4169385 | ASSEMBLY AND METHOD OF SEMICON DUCTOR DIE ATTACH STRESS ISOLA TION |
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JP 4170409

METHOD FOR MAKING A FERROELECT RIC DEVICE

FREESCALE SEMICONDUCTOR, INC.

| FREESCALE SEMICONDUCTOR, INC. | JP | 4173858 | INSTRUCTION CACHE AND METHOD FOR REDUCING MEMORY CONFLICTS |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 4180145 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4180151 | ELECTRONIC APPARATUS WITH FAST START-UP CHARACTERISTICS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4181992 | DUAL STEERED FREQUENCY SYNTHESIZER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4191278 | MEMORY DEVICE WITH FAST WRITE RECOVERY AND RELATED WRITE REC OVERY METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4203146 | INTEGRATED CIRCUIT DEVICE AND METHOD OF TESTING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4206137 | SEMICONDUCTOR MEMORY DEVICE AN D MANUFACTURING METHOD THEREFO R |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4206151 | CLOCK GENERATION METHOD AND SY STEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4208207 | METHOD FOR PLANARIZING A SEMIC ONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4210594 | CIRCUITRY FOR CREATING A SPECTRAL NULL IN A DIFFERENTIAL OUTPUT SWITCHING AMPLIFIER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4210698 | METHOD AND APPARATUS FOR SELECTING CACHE WAYS AVAILABLE FOR REPLACEMENT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4213040 | METHOD AND APPARATUS FOR DETECTING A STALL CONDITION IN A STEPPING MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4213666 | RADIO RECEIVER HAVING A VARIABLE BANDWIDTH IF FILTER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4216588 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND SEMICONDUCTOR COMPONENT THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4216732 | METHOD OF USING SUB-RATE SLOTS IN AN ULTRAWIDE BANDWIDTH SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4220582 | METHOD OF FABRICATING A SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4226149 | CMOS SEMICONDUCTOR DEVICES AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4226668 | PERIPHERAL MODULE AND MICROPRO CESSOR SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4227097 | THREE INPUT SENSE AMPLIFIER AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4227682 | INTEGRATED CIRCUIT AMPLIFIER A ND METHOD FOR ADAPTIVE OFFSET |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4230545 | A DATA PROCESSING SYSTEM AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4235047 | MEMORY HAVING HIGH SAFETY OF STORED DATA AND DATA PROCESSOR USING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4235175 | METHOD AND APPARATUS FOR PROCESSING AN AMPLITUDE MODULATED (AM) SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4236586 | LOW DROP-OUT VOLTAGE REGULATOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4236683 | PHASE LOCKED LOOP FILTER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4249309 | RELOCATABLE INSTRUMENTATION TAGS FOR TESTING AND DEBUGGING A COMPUTER PROGRAM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4251708 | RADIO WITH HALTING APPARATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4253046 | APPARATUS FOR DETECTING DIAPHR AGM DISORDER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4256944 | VOLTAGE DETECTOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4256944 | VOLTAGE DETECTOR CIRCUIT |

| FREESCALE SEMICONDUCTOR, INC. | JP | 4262091 | METHOD OF FORMING A PATTERN ON A SEMICONDUCTOR WAFER USING AN ATTENUATED PHASE SHIFTING REFLECTIVE MASK |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 4262327 | SEMICONDUCTOR DEVICE AND METHOD FOR MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4262334 | ETCHING APPARATUS AND METHOD OF ETCHING A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4263290 | CIRCUIT AND METHOD FOR INTERLEAVING A DATA STREAM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4264436 | FLIP FLOP FUNCTION DEVICE, SEMICONDUCTOR INTEGRATED CIRCUIT, AND METHOD AND APPARATUS FOR DESIGNING SEMICONDUCTOR INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4266250 | INTERFACE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4267282 | SYSTEM HAVING USER PROGRAMMABLE ADDRESSING MODES AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4267322 | INTEGRATED CMOS CAPACITIVE PRESSURE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4271741 | SENSOR AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4271751 | ELECTRONIC DEVICE AND METHOD F OR FORMING A MEMBRANE FOR AN ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4271843 | METHOD AND APPARATUS FOR CONFIGURING A DATA PROCESSING SYSTEM AFTER RESET |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4271858 | METHOD AND APPARATUS FOR ACCURATE SYNCHRONIZATION USING SYMBOL DECISION FEEDBACK |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4273000 | METHOD FOR IMPROVED MEDIA QUALITY FEEDBACK |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4276338 | A METHOD FOR INITIALIZING A DISTRIBUTED CONTROL SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4276537 | HIGH PERFORMANCE INTEGRATED CIRCUIT REGULATOR WITH SUBSTRATE TRANSIENT SUPPRESSION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4276681 | METHOD FOR TRANSMITTING SIGNAL S BETWEEN A MICROPORCESSOR AND AN INTERFACE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4286397 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING A CAPACITOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4290983 | SEMICONDUCTOR TILING STRUCTURE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4308671 | SEMICONDUCTOR DEVICE HAVING A WIRE BOND PAD AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4308938 | METHOD OF TESTING A SEMICONDUC TOR DEVICE BY AUTOMATICALLY ME ASURING PROBE TIP PARAMETERS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4313555 | GALOIS MULTIPLIER USING CRC CODER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4313759 | HYBRID STRUCTURE FOR DISTRIBUTED POWER AMPLIFIERS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4313760 | FULL BRIDGE INTEGRAL NOISE SHAPING FOR QUANTIZATION OF PULSE WIDTH MODULATION SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4318457 | ARRANGEMENT AND METHOD FOR IMPEDANCE MATCHING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4319712 | METHOD AND APPARATUS FOR PROVI DING ACCESS PROTECTION IN AN I NTEGRATED CIRCUIT |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 4320122 | POWER AMPLIFIER OUTPUT MODULE FOR DUAL-MODE DIGITAL SYSTEMS |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 4322806 | ELECTRONIC DISCHARGE PROTECTION CIRCUITRY AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4322809 | METHOD AND CIRCUITRY FOR IDENTIFYING WEAK BITS IN AN MRAM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4322810 | LOW VOLTAGE DETECTION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4324290 | CIRCUIT AND METHOD OF FREQUENCY SYNTHESIZER CONTROL WITH A SERIAL PERIPHERAL INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4326609 | SEMICONDUCTOR COMPONENT AND ME THOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4326805 | AN OPTO-COUPLING DEVICE STRUCTURE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4328295 | RECEIVER FOR A SWITCHED SIGNAL ON A COMMUNICATION LINE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4328390 | NON-VOLATILE REGISTER AND METH OD FOR ACCESSING DATA THEREIN |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4334647 | METHOD FOR FORMING INTERCONNEC T BUMPS ON A SEMICONDUCTOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4336309 | COMMUNICATION APPARATUS INCLUDING DRIVER MEANS FOR APPLYING A SWITCHED SIGNAL TO A COMMUNICATION LINE WITH A CONTROLLED SLEW RATE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4336416 | SEMICONDUCTOR DEVICE AND ALIGNMENT METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4343296 | SEMICONDUCTOR DEVICE HAVING A SUB-CHIP-SCALE PACKAGE STRUCTU RE AND METHOD FOR FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4344473 | CIRCUIT AND METHOD FOR REDUCING SAMPLING NOISE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4347812 | SYSTEM, NODE AND METHOD FOR PROVIDING MEDIA ARBITRATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4354183 | HIGH K DIELECTRIC FILM AND METHOD FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4355443 | DUAL DIGITAL LOW IF COMPLEX RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4355658 | OSCILLATOR CIRCUIT HAVING REDUCED LAYOUT AREA AND LOWER POWER SUPPLY TRANSIENTS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4357610 | SINGLE CRYSTAL INGOT AND METHOD AND APPARATUS FOR GROWING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4359359 | AMPLIFIER AND METHOD OF CANCEL ING DISTORTION BY COMBINING HY PERBOLIC TANGENT AND HYPERBOLI C SINE TRANSFER FUNCTIONS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4364330 | METHOD AND CIRCUIT FOR IMAGE REJECTION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4364799 | METHOD OF FORMING NANOCRYSTALS IN A MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4368920 | METHOD AND APPARATUS HAVING A DIGITAL PWM SIGNAL GENERATOR WITH INTEGRAL NOISE SHAPING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4370086 | WAFER MANAGEMENT SYSTEM AND METHODS FOR MANAGING WAFERS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4376322 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4377686 | SELECTIVE METAL OXIDE REMOVAL |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4381983 | CLOSED LOOP CURRENT CONTROL CIRCUIT AND METHOD |

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| FREESCALE SEMICONDUCTOR, INC. | JP | 4382489 | A CHEMISTRY FOR ETCHING QUATERNARY INTERFACE LAYERS ON InGaAsP MOSTLY FORMED BETWEEN GaAs AND InxGa(1-x) P LAYERS |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 4383046 | FREQUENCY MODULATOR USING A WAVEFORM GENERATOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4383878 | SCATTERNET OR MULTI-HOP AD-HOC NETWORKING TOPOLOGY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4388144 | REFERENCE CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4397440 | SEMICONDUCTOR STRUCTURE HAVING A MONOCRYSTALLINE MEMBER OVER LYING A CAVITY IN A SEMICONDUC TOR SUBSTRATE AND PROCESS THER EFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4397443 | IMAGE REJECT TRANSCEIVER AND METHOD OF REJECTING AN IMAGE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4401289 | LOW DROP-OUT VOLTAGE REGULATOR AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4401500 | CIRCUIT AND METHOD FOR REDUCING PARASITIC BIPOLAR EFFECTS DURING ELECTROSTATIC DISCHARGES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4401776 | VARIABLE GAIN AMPLIFIER WITH AUTOBIASING SUPPLY REGULATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4402109 | LOW VOLTAGE NMOS-BASED ELECTROSTATIC DISCHARGE CLAMP |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4402178 | APPARATUS AND METHOD FOR CONCU RRENT SEARCH CONTENT ADDRESSAB LE MEMORY CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4405621 | METHOD AND APPARATUS FOR WRITING AN ERASABLE NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4405910 | METHOD AND APPARATUS FOR DETERMINING AN UPPER DATA RATE FOR A VARIABLE DATA RATE SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4409028 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4409427 | DATA PROCESSING SYSTEM HAVING MULTIPLE REGISTER CONTEXTS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4414221 | PROCESS FOR MAKING A MIM CAPACITOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4416843 | METHOD FOR FORMING A TRENCH IS OLATION STRUCTURE IN AN INTEGR ATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4416854 | UNIVERSAL TRANSPORT APPARATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4416951 | QUANTUM RANDOM ADDRESS MEMORY WITH POLYMER MIXER AND/OR MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4417439 | SEMICONDUCTOR DEVICE STRUCTURE AND METHOD UTILIZING AN ETCH STOP LAYER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4417448 | METHOD AND APPARATUS FOR MEASU RING CONTAMINATION ON A SEMICO NDUCTOR WAFER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4421073 | PROTECTION CIRCUIT AND METHOD FOR PROTECTING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4421294 | SEMICONDUCTOR WAFER INDENTIFICATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4422304 | A SYSTEM FOR INITIALIZING A DISTRIBUTED COMPUTER SYSTEM AND A METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4422411 | MICROELECTRONIC ASSEMBLY WITH DIE SUPPORT AND METHOD |

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FREESCALE SEMICONDUCTOR, INC.

| FREESCALE SEMICONDUCTOR, INC. | JP | 4428537 | NETWORK MESSAGE STASHING WITH FILING USING PATTERN MATCHING |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 4429903 | LITHOGRAPHIC TEMPLATE HAVING A REPAIRED GAP DEFECT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4430669 | SEMICONDUCTOR FABRICATION PROCESS WITH ASYMMETRICAL CONDUCTIVE SPACERS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4431502 | METHOD OF FORMING SEMICONDUCTOR DEVICES THROUGH EPITAXY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4435328 | METHOD OF PROBING A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4436765 | LOW STRESS SEMICONDUCTOR DIE ATTACH |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4440922 | SYSTEM AND METHOD FOR PASSING DATA FRAMES IN A WIRELESS NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4443932 | CONVERSION BETWEEN OPTICAL AND RADIO FREQUENCY SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4444420 | PROCESS FOR FORMING A CONDUCTIVE STRUCTURE AND A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4444660 | SYSTEM AND METHOD FOR HANDLING ASYNCHRONOUS DATA IN A WIRELESS NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4445074 | AN INTEGRATED CIRCUIT USING PROGRAMMABLE DELAY CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4451134 | METHOD OF FORMING A BOND PAD AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4459548 | HBT LINEARIZER AND POWER BOOSTER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4460291 | AN INTEGRATED CIRCUIT USING A REFLECTIVE MASK |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4463334 | SINGLE LEVEL GATE NONVOLATILE MEMORY DEVICE AND METHOD FOR ACCESSING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4463346 | AIRBAG DEPLOYMENT SYSTEM AND METHOD FOR MONITORING SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4463416 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4467983 | ENABLE PROPAGATION CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4476459 | A SIGNAL PROCESSING CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4476622 | TEMPERATURE-CONTROLLED CHUCK AND METHOD FOR CONTROLLING THE TEMPERATURE OF A SUBSTANTIALLY FLAT OBJECT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4481482 | CIRCUIT AND METHOD FOR CONTROLLING AN ALARM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4484271 | METHOD OF MANUFACTURING ELECTRONIC COMPONENTS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4485145 | INTEGRATED CIRCUIT AND METHOD OF FORMING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4485529 | NETWORK MESSAGE PROCESSING USING INVERSE PATTERN MATCHING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4489859 | COMPUTER SYSTEM WITH TRIGGER C ONTROLLED INTERFACE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4493121 | SEMICONDUCTOR DEVICE AND METHOD FOR PACKAGING A SEMICONDUCTOR CHIP |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4503442 | DECISION FEED FORWARD EQUALIZER SYSTEM AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4503924 | LITHOGRAPHY METHOD FOR FORMING SEMICONDUCTOR DEVICES ON A WAFER AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4509181 | ARRANGEMENT AND METHOD FOR DUAL MODE OPERATION |

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| FREESCALE SEMICONDUCTOR, INC. | JP | 4509532 | SENSE AMPLIFIER BIAS CIRCUIT FOR A MEMORY HAVING AT LEAST TWO DISTINCT RESISTANCE STATES |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 4509562 | SEMICONDUCTOR POWER DEVICE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4510808 | AMPLITUDE LEVEL CONTROL CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4514881 | CIRCUIT AND METHOD FOR ATTENUATING NOISE IN A DATA CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4514932 | METHOD AND APPARATUS FOR A CALIBRATED FREQUENCY MODULATION PHASE LOCKED LOOP |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4515258 | SIMPLIFICATION OF BALL ATTACH METHOD USING SUPER- SATURATED FINE CRYSTAL FLUX |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4516640 | INTERCONNECT STRUCTURE IN A SE MICONDUCTOR DEVICE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4521068 | PIPELINED DUAL PORT INTEGRATED CIRCUIT MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4522849 | SIGMA-DELTA ANALOG-TO-DIGITAL CONVERTER AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4532480 | ESD PROTECTION DEVICE AND METHOD OF MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4539977 | CAPACITIVE CHARGE PUMP |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4545745 | MICELLAR TECHNOLOGY FOR POST-ETCH RESIDUES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4545798 | METHOD AND SYSTEM FOR IMPROVING THE DESIGN OF SEMICONDUCTOR INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4545917 | LOW PROFILE INTERCONNECT STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4549448 | METHOD AND APPARATUS FOR VERIF YING AND CHARACTERIZING DATA R ETENTION TIME IN A DRAM USING BUILT-IN TEST CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4549676 | ARTICLE COMPRISING AN OXIDE LAYER ON A GaAs-BASED SEMICONDUCTOR STRUCTURE AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4554706 | SELF-ALIGNING RESONATOR FILTER CIRCUIT AND WIDEBAND TUNER CIRCUIT INCORPORATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4554930 | METHOD OF BONDING AND TRANSFERRING A MATERIAL TO FORM A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4555297 | CELLULAR MODEM PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4555835 | DIE ENCAPSULATION USING A POROUS CARRIER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4563340 | PROCESS FOR FORMING A SEMICOND UCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4563530 | QUANTUM RANDOM ADDRESS MEMORY WITH MAGNETIC READOUT AND/OR NANO-MEMORY ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4566325 | SEMICONDUCTOR DEVICE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4574772 | SENSING CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4575154 | MULTI-TIERED LITHOGRAPHIC TEMPLATE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4575915 | COMMUNICATING CONVERSATIONAL DATA SIGNALS BETWEEN TERMINALS OVER A RADIO LINK |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4579352 | OPTICAL SEMICONDUCTOR COMPONEN T AND METHOD OF FABRICATION |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 4579539 | HIGH FREQUENCY SIGNAL ISOLATION IN A SEMICONDUCTOR DEVICE |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 4583515 | METHOD FOR REDUCING PARTICLES ON A SUBSTRATE USING CHUCK CLE ANING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4583531 | METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING A LAYER DEPOSITED BY VARYING FLOW OF REACTANTS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4589918 | METHOD OF PATTERNING ON A WAFER USING A RELECTIVE MASK WITH A MULTI-LAYER ARC |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4594064 | SURGE CURRENT PREVENTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4598858 | DEVICE AND METHOD FOR ARBITRATING BETWEEN DIRECT MEMORY ACCESS TASK REQUEST |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4598905 | A BONDING STRUCTURE BETWEEN A CHIP AND A SUBSTRATE AND THE M ETHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4602350 | LAND GRID ARRAY PACKAGED DEVICE AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4602352 | LOW IF RADIO RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4602403 | METHOD AND APPARATUS FOR ENDIANNESS CONTROL IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4606525 | SEMICONDUCTOR DEVICE AND A PROCESS FOR FORMING THE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4608494 | METHOD OF FORMING A SEMICONDUCTOR PACKAGE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4608576 | TWISTED PAIR COMMUNICATION SYSTEM, APPARATUS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4610682 | INTEGRATED CIRCUIT INTERCONNEC T METHOD AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4611421 | LOGIC THRESHOLD ACQUISITION CIRCUITS AND METHODS USING REVERSED PEAK DETECTORS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4615078 | INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4620656 | ELECTRONIC COMPONENT AND METHOD OF MANUFACTURNG SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4624516 | A FUSE DETECT CIRCUIT AND INTEGRATED CIRCUIT MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4625012 | SEMICONDUCTOR PACKAGE HAVING OPTIMIZED WIRE BONI POSITIONING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4625550 | ELECTRONIC COMPONENT AND METHOD FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4628521 | METHOD AND APPARATUS FOR PROCESSING INTERRUPTIBLE, MULTI-CYCLE INSTRUCTIONS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4629667 | ACTIVATION PLATE FOR ELECTROLESS AND IMMERSION PLATING OF INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4633740 | FLIPCHIP QFN PACKAGE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4647594 | INTEGRATED CIRCUIT DIE I/O CELLS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4652324 | VARIABLE REFRESH CONTROL FOR A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4652394 | MULTIPLE BURST PROTOCOL DEVICE CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4653383 | PACKAGED SEMICONDUCTOR DEVICE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4653735 | PROCESS FOR FORMING DUAL METAL GATE STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4658039 | NON-VOLATILE MEMORY HAVING A BIAS ON THE SOURCE |

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| FREESCALE SEMICONDUCTOR, INC. | JP | 4659751 | METHOD OF FORMING A LOW K DIELECTRIC IN A SEMICONDUCTOR MANUFACTURING PROCESS |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 4663235 | APPARATUS FOR CONVEYING FLUIDS AND BASE PLATE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4666730 | METHOD FOR TESTING AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4672116 | A MEMORY UTILIZING A PROGRAMMABLE DELAY TO CONTROL ADDRESS BUFFERS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4675897 | MULTIPLEXING OF DIGITAL SIGNALS AT MULTIPLE SUPPLY VOLTAGES IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4680888 | MULTI-DIE SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4684652 | SEMICONDUCTOR DEVICE EXHIBITING ENHANCED PATTER RECOGNITION WHEN ILLUMINATED IN A MACHINE VISION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4685025 | SEMICONDUCTOR DEVICE WITH MAGNETICALLY PERMEABLE HEAT SINK |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4685882 | METAL GATE TRANSISTOR FOR CMOS PROCESS AND METHOD FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4685997 | PIPELINED DUAL PORT INTEGRATED CIRCUIT MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4689053 | METHOD AND APPARATUS FOR ALIGNING A WAVEGUIDE TO A DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4690326 | TEMPLATE LAYER FORMATION |
| REESCALE SEMICONDUCTOR, INC. | JP | 4698826 | SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4699363 | METHOD AND APPARATUS FOR DYNAMIC PREFETCH BUFF. CONFIGURATION AND REPLACEMENT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4700184 | INTEGRATED FILTER WITH IMPROVED I/O MATCHING (AND METHOD OF FABRICATION) |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4700185 | LINEAR CAPACITOR STRUCTURE IN A CMOS PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4703556 | FLIP-CHIP ASSEMBLY WITH THIN UNDERFILL AND THICK SOLDER MASK |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4703808 | SENSOR AND METHOD OF MANUFACTURE |
| REESCALE SEMICONDUCTOR, INC. | JP | 4704679 | SEMICONDUCTOR DEVICE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4707822 | RADIO BACK-END CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4708359 | METHOD AND APPARATUS FOR DYNAMICALLY INSERTING GAIN IN AN ADAPTIVE FILTER SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4708414 | AUTONOMOUS MEMORY CHECKER FOR RUNTIME SECURIT ASSURANCE AND METHOD THEREFORE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4709765 | HIGH K DIELECTRIC FILM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4712519 | HIGH SIDE CHARGE PUMP CIRCUIT FOR WIDE RANGE OF SUPPLY VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4712686 | ARC LAYER FOR SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4717173 | A MEMORY DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4722641 | CONNECTION MANAGEMENT SYSTEM, METHOD AND PROGRAM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4722907 | UNIVERSAL SERIAL BUS TRANSMITTER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4722999 | MICROELECTRONIC ASSEMBLY AND METHOD FOR FORMITTHE SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4724652 | UNDERFILL FILM FOR PRINTED WIRING ASSEMBLIES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4727584 | ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT AND |

METHOD OF OPERATION

| FREESCALE SEMICONDUCTOR, INC. | JP | 4728237 | METHOD AND APPARATUS FOR PROVIDING SECURITY FOR DEBUG CIRCUITRY |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 4728393 | METHOD AND DEVICE FOR PROCESSING IMAGE DATA |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4728741 | DISCHARGE DEVICE AND DC POWER SUPPLY SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4732567 | SEMICONDUCTOR DEVICE AND GUARD-RING LAYOUT METHOD FOR OPTIMIZING LATCH-UP PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4738695 | ACCELERATION SENSOR AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4738945 | DEGLITCH FILTER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4744146 | SEMICONDUCTOR COMPONENT COMPRISING A RESUR TRANSISTOR AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4744435 | SEMICONDUCTOR ALIGNMENT AID |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4744514 | SEPARATELY STRAINED N-CHANNEL AND P-CHANNEL TRANSISTORS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4745023 | RIPPLE FILTER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4748918 | AN APPARATUS AND A METHOD FOR PROVIDING DECODED INFORMATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4749556 | FLEXIBLE INTERRUPT CONTROLLER THAT INCLUDES AN INTERRUPT FORCE REGISTER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4750865 | A METHOD AND APPARATUS FOR AFFECTING SUBSEQUENT INSTRUCTION PROCESSING IN A DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4757867 | METHOD FOR FORMING A GATE ELECTRODE HAVING A METAL |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4768012 | STRUCTURE FOR STACKING AN INTEGRATED CIRCUIT ON ANOTHER INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4769353 | COMPONENT AND METHOD FOR MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4777335 | INTEGRATED CIRCUIT WITH MULTIPLE SPACER INSULATING REGION WIDTHS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4777861 | AUTO BIAS CONTROLLING COMPARATOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4777987 | SEMICONDUCTOR TRANSISTOR HAVING STRUCTURAL ELEMENTS OF DIFFERING MATERIALS AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4778889 | MEMORY HAVING A VARIABLE REFRESH CONTROL AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4782972 | APPARATUS FOR REDUCING DC OFFSET IN A RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4786445 | SERIES REGULATOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4787746 | SINGLE PROOF MASS, 3 AXIS MEMS TRANSDUCER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4790192 | PLANAR ULTRA WIDE BAND ANTENNA WITH INTEGRATED ELECTRONICS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4790894 | METHOD OF FORMING A COPPER LAYER OVER A SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4790967 | DUAL METAL GATE TRANSISTORS FOR CMOS PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4791593 | METHOD OF FORMING A COPPER LAYER OVER A SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4791594 | METHOD OF FORMING A COPPER LAYER OVER A SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4794389 | METHOD FOR FORMING A PASSIVATION LAYER FOR AIR GAP |

FORMATION AND STRUCTURE THEREOF

| JP | 4796580 | APPARATUS AND METHOD FOR PROVIDING INFORMATION TO A CACHE MODULE USING FETCH BURSTS |
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| JP | 4799868 | METHOD FOR FORMING A PASSIVATION LAYER FOR AIR GAP FORMATION AND STRUCTURE THEREOF |
| JP | 4804667 | DRIVER CIRCUIT |
| JP | 4805163 | APPARATUS AND METHOD FOR TIME ORDERING EVENTS IN A SYSTEM HAVING MULTIPLE TIME DOMAINS |
| JP | 4808769 | METHODS AND APPARATUS FOR SYNCHRONIZING DATA TRANSFERRED ACROSS A MULTI-PIN ASYNCHRONOUS SERIAL INTERFACE |
| JP | 4809571 | METHOD AND APPARATUS FOR DETECTING AND COMPENSATING DIGITAL LOSSES IN A COMMUNICATIONS NETWORK |
| JP | 4809761 | AREA-ARRAY DEVICE ASSEMBLY WITH PRE-APPLIED UNDERFILL LAYERS ON PRINTED WIRING BOARD |
| JP | 4810050 | CARRIERLESS ULTRA WIDEBAND WIRELESS SIGNALS FOR CONVEYING DATA |
| JP | 4814786 | MEMORY MANAGEMENT IN A DATA PROCESSING SYSTEM |
| JP | 4814791 | LEVEL SHIFTER |
| JP | 4827932 | DYNAMIC TIMING ADJUSTMENT IN A CIRCUIT DEVICE |
| JP | 4833755 | OSCILLATION CIRCUIT |
| JP | 4833972 | METHOD FOR ASSEMBLING A SEMICONDUCTOR COMPONENT AND APPARATUS THEREFOR |
| JP | 4834086 | SPREAD SPECTRUM CLOCK AND METHOD FOR MESSAGE TIMING IN A COMMUNICATION SYSTEM |
| JP | 4837560 | INTEGRATED CIRCUIT WITH TEST PAD STRUCTURE AND METHOD OF TESTING |
| JP | 4842126 | VARIABLE GATE BIAS FOR A REFERENCE TRANSISTOR IN A NON-VOLATILE MEMORY |
| JP | 4848366 | SEMICONDUCTOR PROCESS AND INTEGRATED CIRCUIT HAVING DUAL METAL OXIDE GATE DIELECTRIC WITH SINGLE METAL GATE ELECTRODE |
| JP | 4848375 | DATA PROCESSING SYSTEM WITH BUS ACCESS RETRACTION |
| JP | 4850669 | LOW VOLTAGE LOW POWER CLASS A/B OUTPUT STAGE |
| JP | 4851532 | LOW NOISE REFERENCE OSCILLATOR WITH FAST START-UP |
| JP | 4855116 | SERIES REGULATOR WITH UNDER VOLTAGE DETECTOR |
| JP | 4855197 | HIGH AND LOW CURRENT MODE SERIES REGULATOR |
| JP | 4856803 | SEMICONDUCTOR DEVICE FOR SUBST RATE TRIGGERED ELECTROSTATIC D ISCHARGE PROTECTION AND METHOD OF FORMING SAME |
| JP | 4859835 | MRAM SENSE AMPLIFIER HAVING A PRECHARGE CIRCUIT AND METHOD FOR SENSING |
| JP | 4862045 | A BOUNDED SIGNAL MIXER AND METHOD OF OPERATION |
| | JP J | JP 4804667 JP 4805163 JP 4808769 JP 4809571 JP 4809761 JP 4814786 JP 4814791 JP 4827932 JP 4833755 JP 4833972 JP 4834086 JP 4842126 JP 4848366 JP 4845669 JP 4855116 JP 4855197 JP 4856803 |

| FREESCALE SEMICONDUCTOR, INC. | JP | 4866548 | METHOD FOR ELIMINATING VOIDING IN PLATED SOLDER |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 4869536 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND CHEMICAL-MECHANICAL POLISHING SYSTEM THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4873819 | ULTRA-LATE PROGRAMMING ROM AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4875981 | PREFETCH CONTROL IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4880103 | CIRCUIT AND METHOD OF LIMITING LEAKAGE CURRENT IN A MEMORY C IRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4883824 | A METHOD AND APPARATUS FOR AFFECTING SUBSEQUENT INSTRUCTION PROCESSING IN A DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4885241 | METHOD OF PATTERNING A LAYER USING A PELLICLE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4891224 | METHOD OF MAKING A SEMICONDUCTOR DEVICE, AND SEMICONDUCTOR DEVICE MADE THEREBY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4891906 | METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING A METAL LAYER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4901476 | SEMICONDUCTOR STRUCTURE WITH DIFFERENT LATTICE CONSTANT MATERIALS AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4901729 | METHOD OF FORMING A NANOCLUSTER CHARGE STORAGE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4902353 | SEMICONDUCTOR DEVICE WITH NANOCLUSTERS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4902648 | INTEGRATED RELAXATION VOLTAGE CONTROLLED OSCILLATOR AND METHOD OF VOLTAGE CONTROLLED OSCILLATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4903340 | LOAD CAPACITANCE COMPENSATED BUFFER AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4903847 | AN INTEGRATED CIRCUIT USING PROGRAMMABLE DELAY CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4906869 | SYSTEM AND METHOD FOR CONTROLLING THE TRANSMIT POWER OF A WIRELESS MODULE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4909454 | METHOD FOR FORMING A BARRIER LAYER FOR USE IN A COPPER INTERCONNECT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4909737 | MEMORY WITH CHARGE STORAGE LOCATIONS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4916617 | REAL-TIME PROCESSOR DEBUG SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4917649 | NETWORK AND METHOD FOR SETTING A TIME-BASE OF A NODE IN THE NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4929168 | DECOUPLED COMPLEMENTARY MASK PATTERNING TRANSFER METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4932153 | MULTIPLE THICKNESS SEMICONDUCTOR INTERCONNECT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4932856 | APPARATUS AND METHOD FOR ADJUSTING AN OPERATING PARAMETER OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4937444 | METHOD OF OPERATING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4937489 | SEMICONDUCTOR DEVICE HAVING PASSIVE ELEMENTS AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4938017 | SEMICONDUCTOR STACKED DIE/WAFER CONFIGURATION |

AND PACKAGING AND METHOD THEREOF

| FREESCALE SEMICONDUCTOR, INC. | JP | 4939895 | HIGH VOLTAGE OUTPUT LEVEL-SHIFTER WITH OUTPUT ENABLE |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 4942757 | SEMICONDUCTOR STRUCTURE WITH REDUCED GATE DOPING AND METHODS FOR FORMING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4949377 | SYSTEM AND METHOD FOR HUMAN BODY FALL DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4951631 | METHOD AND APPARATUS FOR ENHANCED DATA RATE ADAPTATION AND LOWER CONTROL IN A SEMICONDUCTOR CHIP |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4954890 | TEMPERATURE BASED DRAM REFRESH |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4955389 | DATA PROCESSING SYSTEM IMPLEMENTING SIMD OPERATIONS AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4960092 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4964128 | CIRCUIT FOR PERFORMING VOLTAGE REGULATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4965462 | METHOD OF MAKING A PLANAR DOUBLE-GATED TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4969724 | SEMICONDUCTOR DEVICE AND PROCESS THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4969746 | VARIABLE SAMPLING DATA OUTPUT CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4975618 | SCHOTTKY DEVICE AND METHOD OF FORMING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4979955 | HIGH INPUT VOLTAGE LEVEL-SHIFTER WITH SCHMITT TRIGGER FUNCTION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4980931 | NON-VOLATILE NANOCRYSTAL MEMORY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4982046 | ONE TRANSISTOR DRAM CELL STRUCTURE AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4982382 | SEMICONDUCTOR FABRICATION PROCESS INCLUDING RECESSED SOURCE/DRAIN REGIONS IN AN SOI WAFER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4987189 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE AND A CONDUCTIVE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4987696 | ISOLATION TRENCH |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4988588 | WORD LINE DRIVER CIRCUIT FOR A STATIC RANDOM ACCESS MEMORY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4990394 | RADIO RECEIVER HAVING IGNITION NOISE DETECTOR AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 4999379 | METHOD AND DEVICE FOR DESIGNING SEMICONDUCTOR INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5009292 | STRESS RELEASE MECHANISM IN MEMS DEVICE AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5014609 | TRIMMING CIRCUIT, ELECTRONIC CIRCUIT AND TRIMMING CONTROL SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5017257 | NICAM ENCODER WITH A FRONT-END |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5025462 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING A NOTCHED CONTROL ELECTRODE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5027154 | IMMERSION LITHOGRAPHY APPARATUS AND METHOD OF PERFORMING IMMERSION LITHOGRAPHY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5030940 | APPARATUS FOR CURRENT SENSING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5031828 | SLEW-RATE CONTROL APPARATUS AND METHODS FOR A POWER TRANSISTOR TO REDUCE VOLTAGE TRANSIENTS |

DURING INDUCTIVE FLYBACK

| FREESCALE SEMICONDUCTOR, INC. | JP | 5042623 | CIRCUIT DEVICE WITH AT LEAST PARTIAL PACKAGING AND METHOD FOR FORMING |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 5048480 | METHOD OF SEMICONDUCTOR FABRICATION INCORPORATING DISPOSABLE SPACER INTO ELEVATED SOURCE/DRAIN PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5049428 | UV CURE PROCESS AND TOOL FOR LOW K FILM FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5049955 | METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING ASYMMETRIC DIELECTRIC REGIONS AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5057606 | ELECTRONIC COMPONENT AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5060296 | METHOD AND APPARATUS FOR MOBILITY ENHANCEMENT IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5064235 | SYSTEM AND METHOD FOR FALL DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5064632 | METHOD AND APPARATUS FOR MANUFACTURING AN INTERCONNECT STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5068074 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING ISOLATION REGIONS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5075630 | SYSTEM AND METHOD FOR ULTRA WIDEBAND COMMUNICATIONS USING MULTIPLE CODE WORDS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5075815 | CHEMICAL DIE SINGULATION TECHNIQUE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5079304 | METHOD FOR FORMING MULTI-LAYER BUMPS ON A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5079493 | LAND GRID ARRAY PACKAGED DEVICE AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5079511 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING A STRAINED CHANNEL AND A HETEROJUNCTION SOURCE/DRAIN |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5081902 | MEMORY WITH LEVEL SHIFTING WORD LINE DRIVER AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5084724 | INTEGRATED CIRCUIT HAVING A NON-VOLATILE MEMORY WITH DISCHARGE RATE CONTROL AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5084733 | SYSTEM AND METHOD OF CODING MODE DECISION FOR VIDEO ENCODING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5090353 | GROOVED PLATEN WITH CHANNELS OR PATHWAY TO AMBIENT AIR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5091387 | METHOD AND APPARATUS FOR AFFECTING A PORTION OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5095184 | LEVELSHIFTER TO AVOID INVALID INPUT SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5101286 | METHOD AND APPARATUS FOR PROTECTING AN INTEGRATED CIRCUIT FROM ERRONEOUS OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5103174 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING A SILICIDE LAYER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5103182 | PROGRAMMING AND ERASING STRUCTURE FOR A FLOATING GATE MEMORY CELL AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5103467 | MEMORY WITH CLOCKED SENSE AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5105688 | MULTI-MODE RADIO COMMUNICATIONS DEVICE USING A SHARED CLOCK COURCE. |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5107049 | METHOD OF INTEGRATING OPTICAL DEVICES AND |

ELECTRONIC DEVICES ON AN INTEGRATED CIRCUIT

| FREESCALE SEMICONDUCTOR, INC. | JP | 5107227 | CONDUCTING METAL OXIDE WITH ADDITIVE AS P-MOS DEVICE ELECTRODE |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 5112290 | INTERLAYER DIELECTRIC UNDER STRESS FOR AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5113974 | METHOD FOR UNIFORM POLISH IN MICROELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5114209 | SRAM HAVING IMPROVED CELL STABILITY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5114470 | CIRCUIT AND METHOD OF LIMITING LEAKAGE CURRENT IN A MEMORY C IRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5117572 | POWER MANAGEMENT ARRANGEMENT AND MOBILE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5117816 | RFC INFORMATION SHARING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5127078 | MRAM TESTING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5128680 | MIXER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5129244 | METHOD AND DEVICE FOR SWITCHING DATA |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5133404 | RADIO RECEIVER HAVING A CHANNEL EQUALIZER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5138611 | SEMICONDUCTOR INTERCONNECT HAVING ADJACENT RESERVOIR FOR BONDING AND METHOD FOR FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5140594 | NICAM PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5147403 | DOUBLE GATE DEVICE HAVING A HETEROJUNCTION SOURCE/DRAIN AND A STRAINED CHANNEL |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5149006 | TRANSISTOR STRUCTURE WITH STRESS MODIFICATION AND CAPACITIVE REDUCTION FEATURE IN A WIDTH DIRECTION AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5149178 | PACKAGED INTEGRATED CIRCUIT WITH ENHANCED THERMAL DISSIPATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5152741 | DUAL PWM GENERATOR FOR LOW VOLTAGE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5153652 | LIN NETWORK, INTEGRATED CIRCUIT AND METHOD OF COMMUNICATING THEREON |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5156001 | MEMORY CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5159306 | LEAD SOLDER INDICATOR AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5160441 | METHOD AND APPARATUS FOR PROGRAMMING/ERASING A NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5161576 | CIRCUIT AND METHOD FOR INTERPOLATIVE DELAY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5162070 | ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5164276 | INTEGRATED CIRCUIT HAVING A MEMORY WITH LOW VOLTAGE READ/WRITE OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5165583 | ESD PROTECTION FOR PASSIVE INTEGRATED DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5166408 | DEVICE AND METHOD FOR TESTING INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5172330 | SEMICONDUCTOR DEVICE AND METHOD OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5179365 | MICROELECTRONIC ASSEMBLY AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5179470 | PROGRAMMABLE CELL |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5179496 | SRAM HAVING VARIABLE POWER SUPPLY AND METHOD THEREFOR |

| FREESCALE SEMICONDUCTOR, INC. | JP | 5180827 | SPLIT GATE STORAGE DEVICE INCLUDING A HORIZONTAL FIRST GATE AND A VERTICAL SECOND GATE IN A TRENCH |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 5187863 | METHOD OF PACKAGING AN INTEGRATED CIRCUIT DIE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5191742 | I/O CELL ESD SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5191885 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5191893 | SEMICONDUCTOR DEVICES AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5198569 | METHOD, INTEGRATED CIRCUIT, AND COMMUNICATION UNIT FOR SCHEDULING A PROCESSING OF PACKET STREAM CHANNELS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5201641 | SIMD DOT PRODUCT OPERATIONS WITH OVERLAPPED OPERANDS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5202089 | METHOD AND CIRCUIT FOR DRIVING H-BRIDGE THAT REDUCES SWITCHING NOISE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5203352 | SEMICONDUCTOR FABRICATION PROCESS USING ETCH STOP LAYER TO OPTIMIZE FORMATION OF SOURCE/DRAIN STRESSOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5205054 | RECESSED SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5208346 | SEMICONDUCTOR DEVICE AND PROCESS FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5208918 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING A FIN AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5208936 | METHOD AND APPARATUS FOR IMPROVEMENTS IN CHIP MANUFACTURE AND DESIGN. |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5213274 | METHOD, DATA STRUCTURE AND COMPUTER SYSTEM FOR PACKING A WORLDWIDE INTEROPERABILITY FOR MICROWAVE ACCESS (WIMAX) FRAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5219324 | SINGLE SUPPLY HFET WITH TEMPERATURE COMPENSATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5225108 | SEMICONDUCTOR PROCESS INTEGRATING SOURCE/DRAIN STRESSORS AND INTERLEVEL DIELECTRIC LAYER STRESSORS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5225186 | CHARGE CONTROL CIRCUIT AND BETTERY CHARGER INCLUDING A CHARGE CONTROL CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5226325 | METHOD AND APPARATUS FOR DYNAMIC DETERMINATION OF FRAMES REQUIRED TO BUILD A COMPLETE PICTURE IN A MPEG VIDEO STREAM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5227501 | METHOD OF MAKING STACKED DIE PACAKGE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5230637 | LOW COST FAULT TOLERANT SLAVE NODE IN AN HETEROGENEOUS NETWORK OF NODES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5230870 | BACK-GATED SEMICONDUCTOR DEVICE WITH A STORAGE LAYER AND METHODS FOR FORMING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5232018 | ERROR CORRECTION DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5234696 | 3-D SEMICONDUCTOR DIE STRUCTURE WITH CONTAINING FEATURE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5248627 | MICROPAD FORMATION FOR A SEMICONDUCTOR |

| FREESCALE SEMICONDUCTOR, INC. | JP | 5249483 | SEMICONDUCTOR DEVICE AND PROCESS FOR DESIGNING A MASK |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 5249757 | ELECTRONIC DEVICE INCLUDING GATE LINES, BIT LINES, OR A COMBINATION THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5254220 | METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING AN INTERLAYER AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5254356 | ELECTRONIC ASSEMBLY MANUFACTURING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5257897 | OUTPUT CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5257954 | TOUCH PANEL DETECTION CIRCUITRY AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5257955 | ANALOG-TO-DIGITAL CONVERTER WITH VARIABLE GAIN AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5263887 | SELF-CALIBRATING OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5268125 | FAULT MANAGEMENT FOR A COMMUNICATION BUS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5273850 | ELECTRONIC DEVICE, METHOD FOR CONTROLLING ELECTRONIC DEVICE, PROGRAM FOR CONTROLLING ELECTRONIC DEVICE, AND CONTROL DEVICE FOR ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5275333 | METHOD AND APPARATUS FOR AFFECTING A PORTION OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5279701 | DATA PROCESSOR HAVING DYNAMIC CONTROL OF INSTRUCTION PREFETCH BUFFER DEPTH AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5280434 | SEPARATE LAYER FORMATION IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5283300 | SEMICONDUCTOR DEVICE HAVING A BOND PAD AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5283507 | MULTIPLE DEVICE TYPES INCLUDING AN INVERTED-T CHANNEL TRANSISTOR AND METHOD THEREFORE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5289968 | METHOD FOR FORMING A SEMICONDUCTOR STRUCTURE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5290574 | SCHOTTKY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5294278 | METHOD FOR FORMING A DUAL METAL GATE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5294843 | METHOD AND APPARATUS FACILITATING MULTI MODE INTERFACES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5296043 | METHOD OF FORMING A COPPER LAYER OVER A SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5296672 | STRESSOR INTEGRATION AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5300035 | OSCILLATOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5300158 | LEADFRAME FOR PACKAGED ELECTRONIC DEVICE WITH ENHANCED MOLD LOCKING CAPABILITY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5300470 | SEMICONDUCTOR PACKAGE AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5301279 | ELECTRONIC DEVICE INCLUDING A TRANSISTOR STRUCTURE HAVING AN ACTIVE REGION ADJACENT TO A STRESSOR LAYER AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5301290 | NOISE ISOLATION BETWEEN CIRCUIT BLOCKS IN AN |

INTEGRATED CIRCUIT CHIP

| FREESCALE SEMICONDUCTOR, INC. | JP | 5311428 | DISPLAY CONTROLLER, IMAGE PROCESSING SYSTEM, DISPLAY SYSTEM, APPARATUS AND COMPUTER PROGRAM PRODUCT |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 5312052 | RF POWER TRANSISTOR DEVICE WITH METAL ELECTROMIGRATION DESIGN AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5312478 | DATA PROCESSOR PERFORMANCE PREDICTION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5317353 | ONE TRANSISTOR DRAM CELL STRUCTURE AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5318597 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5334138 | INTEGRATED CIRCUIT MEMORY HAVING DYNAMICALLY ADJUSTABLE READ MARGIN AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5335663 | MESSAGE BUFFER FOR A RECEIVER APPARATUS ON A COMMUNICATIONS BUS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5335791 | METHOD AND CIRCUIT FOR PREVENTING HIGH VOLTAGE MEMORY DISTURB |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5335803 | KNOCK SIGNAL DETECTION IN AUTOMOTIVE SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5335887 | QUALIFICATION OF CONDITIONAL DEBUG INSTRUCTIONS BASED ON ADDRESS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5335995 | INTEGRATED CIRCUIT, COMMUNICATION UNIT AND METHOD FOR PHASE ADJUSTMENT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5341087 | STRESS RELIEF OF A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5344636 | SIMPLIFIED DEBLOCK FILTERING FOR REDUCED MEMORY ACCESS AND COMPUTATIONAL COMPLEXITY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5345521 | TRANSISTOR AND METHOD WITH DUAL LAYER PASSIVATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5349953 | SYSTEM AND METHOD FOR PROTECTING LOW VOLTAGE TRANSCEIVER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5350589 | TRANSISTOR WITH INDEPENDENT GATE STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5354692 | METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE TYPES OF SCHOTTKY JUNCTIONS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5354907 | SEMICONDUCTOR DEVICE HAVING NITRIDATED OXIDE LAYER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5356253 | METHOD OF MAKING A NON-VOLATILE MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5356371 | METHOD OF FORMING A SEMICONDUCTOR DEVICE FEATURING A GATE STRESSOR AND SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JР | 5356689 | Z-AXIS ACCELEROMETER WITH AT LEAST TWO GAP SIZES AND TRAVEL STOPS DISPOSED OUTSIDE AN ACTIVE CAPACITOR AREA |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5366797 | ELECTRONIC DEVICE INCLUDING SEMICONDUCTOR ISLANDS OF DIFFERENT THICKNESSES OVER AN INSULATING LAYER AND A PROCESS OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | 5366833 | CONDUCTIVE VIA FORMATION UTILIZING ELECTROPLATING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5366833 | CONDUCTIVE VIA FORMATION UTILIZING ELECTROPLATING |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 5366893 | DATA PROCESSING SYSTEM IMPLEMENTING SIMD OPERATIONS AND METHOD THEREOF |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 5372493 | METHOD OF MAKING A DUAL STRAINED CHANNEL SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 5372602 | BATTERY CHARGING CIRCUIT AND BATTERY CHARGER |
| FREESCALE SEMICONDUCTOR, INC. | FR | 9507903 | SEMICONDUCTOR SENSOR DEVICE AN D METHOD FOR FORMING A SEMICON DUCTOR SENSOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | DE | 19820878.2 | PROCESS FOR DEPOSITING A LAYER OF MATERIAL ON A SUBSTRATE AN D A PLATING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | DE | 19928691.4 | AIRBAG DEPLOYMENT SYSTEM AND M ETHOD FOR MONITORING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 030146066.6 | DUAL GAUGE LEADFRAME |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60025773.8 | METHOD OF FORMING A COPPER LAY ER OVER A SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60031191.0 | METHOD FOR FORMING A BARRIER L AYER FOR USE IN A COPPER INTER CONNECT |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60102609.8 | SOFTWARE ANALYSIS SYSTEM HAVING AN APPARATUS FOR SELECTIVELY COLLECTING ANALYSIS DATA FROM A TARGET SYSTEM EXECUTING SOFTWARE INSTRUMENTED WITH TAG STATEMENTS AND METHOD FOR USE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60108730.5 | EEPROM CIRCUIT, VOLTAGE REFERENCE CIRCUIT AND METHOD FOR PROVIDING A LOW TEMPERATURE-COEFFICIENT VOLTAGE REFERENCE |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60116381.8 | ELECTRO-OPTIC STRUCTURE AND PROCESS FOR FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60124965.8 | UV CURE PROCESS AND TOOL FOR LOW K FILM FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60127932.8 | CHANNEL ESTIMATION IN ORTHOFONAL FREQUENCY DIVISION MULTIPLEXED SYSTEMS. |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60134220.8 | METHOD OF MANUFACTURING A HETEROJUNCTION BICMOS INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60142406.9 | INTEGRATED CMOS CAPACITIVE PRESSURE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60206146.6 | COMMUNICATION APPARATUS INCLUDING DRIVER MEANS FOR APPLYING A SWITCHED SIGNAL TO A COMMUNICATION LINE WITH A CONTROLLED SLEW RATE |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60207087.2 | ODD HARMONICS REDUCTION OF PHASE ANGLE CONTROLLED LOADS |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60215463.4 | ANALOG-TO-DIGITAL CONVERTER ARRANGEMENT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60226141.4 | FIRST-IN FIRST-OUT MEMORY SYSTEM AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60241164.5 | HIGH FREQUENCY SIGNAL ISOLATION IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60241422.9 | METHOD AND APPARATUS FOR DETECTING A STALL CONDITION IN A STEPPING MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60303126.9 | METHOD AND APPARATUS FOR SECURE SCAN TESTING |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60305736.5 | SENSE AMPLIFIER FOR A MEMORY HAVING AT LEAST TWO DISTINCT RESISTANCE STATES |
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| FREESCALE SEMICONDUCTOR, INC. | DE | 60306164.8 | METHOD AND APPARATUS FOR AFFECTING A PORTION OF AN INTEGRATED CIRCUIT |
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| FREESCALE SEMICONDUCTOR, INC. | DE | 60307429.4 | METHOD AND APPARATUS FOR REDUCED POWE CONSUMPTION ADC/DAC CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60307539.8 | MICRO-ELECTRO-MECHANICAL DEVICE AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60308032.4 | POWER AMPLIFIER SATURATION DETECTION AND OPERATION AT MAXIMUM POWER |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60308492.3 | KEYPAD SIGNAL INPUT APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60308539.3 | LOW IF RADIO RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60310096.1 | A POWER AMPLIFIER MODULE AND A TIME DIVISION MULTIPLE ACCESS RADIO |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60314384.9 | PHASE LOCKED LOOP FILTER |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60314754.2 | TRANSCONDUCTANCE AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | DE | 60318643.2 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69419871.4 | DOUBLE IMPLANTED LATERALLY DIF FUSED MOS DEVICE AND METHOD TH EREOF |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69428684.2 | THERMISCH-LEITENDES GEHAEUSE FUER INTEGRIERTE SCHALTUNGEN MIT RADIOFREQUENZ-ABSCHIRMUNG |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69430648.7 | SEMICONDUCTOR DEVICE HAVING X- SHAPED DIE SUPPORT MEMBER AND METHOD FOR MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69431273.8 | REVERSE BATTERY PROTECTION CIR CUIT |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69432068.4 | TRENCH ISOLATION STRUCTURE IN AN INTEGRATED CIRCUIT AND METH OD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69433582.7 | SEMICONDUCTOR DEVICE AND FERRO ELECTRIC CAPACITOR |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69526539.3 | SEMICONDUCTOR DEVICE AND METHO D OF FORMING |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69527388.4 | EEPROM CELL WITH ISOLATION TRA NSISTOR AND METHODS FOR MAKING AND OPERATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69534412.9 | III-V SEMICONDUCTOR STRUCTURE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69615720.9 | PIEZORESISTIVE WANDLER MIT UEBERLAPPENDEN KONTAKTEN |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69623679.6 | METHOD FOR FORMING A TRENCH IS OLATION STRUCTURE IN AN INTEGR ATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69630488.0 | SEMICONDUCTOR SENSOR DEVICE AN D METHOD FOR FORMING A SEMICON DUCTOR SENSOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69631451.7 | MONOLITHIC HIGH FREQUENCY INTE GRATED CIRCUIT STRUCTURE AND M ETHOD OF MANUFACTURING THE SAM E |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69631946.2 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69707169.3 | PROGRAMMIERUNG FUER NICHT-FLUECHTIGE SPEICHERZELLE |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69713550.0 | AUTOMOBILE AIRBAG SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69716349.0 | CURRENT LIMIT CONTROLLER FOR A N AIR BAG DEPLOYMENT SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69724486.5 | SEMICONDUCTOR CHEMICAL SENSOR DEVICE AND ETHOD OF FORMING A THERMOCOUPLE FOR A SEMICONDUCT OR |

CHEMICAL SENSOR DEVICE

| FREESCALE SEMICONDUCTOR, INC. | DE | 69725770.3 | NEW GEOMETRY FOR ALOW RESISTAN T HEATER |
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| FREESCALE SEMICONDUCTOR, INC. | DE | 69727001.7 | SENSOR AND METHOD OF FABRICATI ON |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69727744.5 | MEMORY SUITABLE FOR OPERATION AT LOW POWER SUPPLY VOLTAGES A ND SENSE AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69729017.4 | METHOD OF SENSING A CHEMICAL A ND SENSOR THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69812579.7 | PORTABLE ELECTRONIC DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69823004.3 | METHOF OF ORMING METAL COLLOID S, METAL COLLOIDS AND METHOD O F FORMING A METAL OXIDE SENSIT IVE LAYER FOR A CHEMICAL SENSOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69837965.9 | METHOD AND SENSOR SYSTEM FOR D ETERMING A CONCENTRATION OF A CHEMICAL SPECIES |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69908577.2 | APPARATUS FOR RECEIVING AND PROCESSING A RADIO FREQUENCY SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69942354.6 | PROGRAMMABLE DELAY CONTROL IN A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | DE | 69944481.0 | PROGRAMMABLE DELAY CONTROL IN A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | CN | 94108219.9 | METHOD AND APPARATUS FOR NOISE BURST DETECTION IN A SIGNAL P ROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 94115626.5 | INTEGRATED CIRCUIT AND METHOD OF FORMING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 94117619.3 | DOUBLE IMPLANTED LATERALLY DIF FUSED MOS DEVICE AND METHOD TH EREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 95103566.5 | PROCESS FOR FORMING A SEMICOND UCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 96100693.5 | SEMICONDUCTOR DEVICE HAVING A BOND PAD AND A PROCESS FOR FOR MING THE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 96107995.9 | METHOD AND APPARATUS FOR AMPLI FYING A SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | CN | 940103953 | SIGMA-DELTA MODULATOR WITH IMP ROVED TONE REJECTION AND METHO D THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 940115625 | METHOD AND APPARATUS FOR TESTI NG A STATIC RAM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200380104261.8 | SEMICONDUCTOR DEVICE HAVING A BOND PAD AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200380105049.3 | SYSTEM, NODE AND METHOD FOR PROVIDING MEDIA ARBITRATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200380105458.3 | DECISION FEED FORWARD EQUALIZER SYSTEM AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200380106432.0 | METHOD AND APPARATUS FOR TRANSLATING DETECTED WAFER DEFECT COORDINATES TO RETICLE COORDINATES USING CAD DATA |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200380107421.4 | METHOD OF FORMING SEMICONDUCTOR DEVICES THROUGH EPITAXY |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200410005247.9 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200410012085.1 | METHOD OF FORMING A SEMICONDUCTOR PACKAGE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200410047641.9 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE AND A |

CONDUCTIVE STRUCTURE

| FREESCALE SEMICONDUCTOR, INC. | CN | 200410069611.8 | METHOD AND APPARATUS FOR INTER FACING A PROCESSOR TO A COPROC ESSOR |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 200480002529.1 | ELECTROSTATIC DISCHARGE CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480002663.1 | METHOD AND APPARATUS FOR CONTROLLING A DATA PROCESSING SYSTEM DURING DEBUG |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480002887.2 | UNDERFILL FILM FOR PRINTED WIRING ASSEMBLIES |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480002915.0 | METAL REDUCTION IN WAFER SCRIBE AREA |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480003133.9 | ARC LAYER FOR SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480003835.7 | LOW VOLTAGE NMOS-BASED ELECTROSTATIC DISCHARGE CLAMP |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480004058.8 | SYSTEM AND METHOD FOR COARSE TUNING A PHASE LOCKED LOOP (PLL) SYNTHESIZER USING 2-PI SLIP DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480004373.0 | VARIABLE REFRESH CONTROL FOR A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480004714.4 | WIREBONDING INSULATED WIRE |
| REESCALE SEMICONDUCTOR, INC. | CN | 200480004901.2 | MULTI-DIE SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480005356.9 | SYSTEM AND METHOD FOR PASSING DATA FRAMES IN A WIRELESS NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480005365 | SYSTEM AND METHOD FOR TRANSMITTING ULTRA-WIDE BAND SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480005983.2 | METHOD OF PATTERNING ON A WAFER USING A RELECTIVE MASK WITH A MULTI-LAYER ARC |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480006810.2 | ELECTRONIC COMPONENT AND METHOD OF MANUFACTURNG SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480007566.1 | MULTI-BIT NON-VOLATILE MEMORY DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480008175.1 | COMMUNICATING CONVERSATIONAL DATA SIGNALS BETWEEN TERMINALS OVER A RADIO LINK |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480008378.0 | METHOD FOR FABRICATING DUAL-METAL GATE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480009252.5 | ESD PROTECTION DEVICE AND METHOD OF MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480009496.3 | PROCESS FOR FORMING DUAL METAL GATE STRUCTURES |
| REESCALE SEMICONDUCTOR, INC. | CN | 200480009498.2 | INTEGRATED CIRCUIT DIE I/O CELLS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480011128 | NON-VOLATILE MEMORY HAVING A BIAS ON THE SOURCE ELECTRODE FOR HCI PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480011464.7 | FUSE AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480011500 | METHOD OF ADDING MASS TO MEMS STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480012216.4 | PREFETCH CONTROL IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480014053.3 | MEMORY WITH CHARGE STORAGE LOCATIONS |
| REESCALE SEMICONDUCTOR, INC. | CN | 200480014138.1 | TRANSISTOR WITH INDEPENDENT GATE STRUCTURES |
| REESCALE SEMICONDUCTOR, INC. | CN | 200480014807.5 | HIGH IMPEDANCE RADIO FREQUENCY POWER PLASTIC PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480015830.6 | SEMICONDUCTOR PACKAGE HAVING OPTIMIZED WIRE BONI POSITIONING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480017194.0 | PHASE LOCKED LOOP FILTER |
| | | 200480017269.5 | METHOD AND APPARATUS FOR DYNAMIC PREFETCH BUFFER |

| FREESCALE SEMICONDUCTOR, INC. | CN | 200480018151.4 | VARIABLE GATE BIAS FOR A REFERENCE TRANSISTOR IN A NON-VOLATILE MEMORY |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 200480018362.8 | PREFETCH CONTROL IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480019280.5 | SINGLE PROOF MASS, 3 AXIS MEMS TRANSDUCER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480019583.7 | METHOD AND APPARATUS FOR PROVIDING SECURITY FOR DEBUG CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480019911.3 | INTEGRATED CIRCUIT WITH TEST PAD STRUCTURE AND METHOD OF TESTING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480020002.1 | MICELLAR TECHNOLOGY FOR POST-ETCH RESIDUES |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480020484.0 | SEMICONDUCTOR DEVICE HAVING ELECTRICAL CONTACT FROM OPPOSITE SIDES AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480022951 | LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480023865.4 | SEMICONDUCTOR DEVICE AND MAKING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480024425.0 | DATA PROCESSING SYSTEM IMPLEMENTING SIMD OPERATIONS AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480024637.9 | WIREBONDING INSULATED WIRE AND CAPILLARY THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480024696.6 | SYNCHRONIZATION OF DATA STREAMS OVER A WIRELESS NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480024779.5 | SEMICONDUCTOR DEVICE WITH NANOCLUSTERS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480025064 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING ISOLATION REGIONS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480025241.6 | MULTIPLEXING OF DIGITAL SIGNALS AT MULTIPLE SUPPLY VOLTAGES IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480026568.5 | DEVICE INCLUDING AN AMORPHOUS CARBON LAYER FOR IMPROVED ADHESION OF ORGANIC LAYERS AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480026575.5 | SEMICONDUCTOR STRUCTURE WITH DIFFERENT LATTICE CONSTANT MATERIALS AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480027415.2 | METHOD OF FORMING A SEMICONDUCTOR PACKAGE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480028260.4 | POWER SUPPLY APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480029071.9 | METHOD OF FORMING A LOW K DIELECTRIC IN A SEMICONDUCTOR MANUFACTURING PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480029484 | CELLULAR MODEM PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480029738.5 | TRANSISTOR HAVING THREE ELECTRICALLY ISOLATED ELECTRODES AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480033180.8 | NETWORK MESSAGE PROCESSING USING INVERSE PATTERN MATCHING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480033499.0 | HIGH K DIELECTRIC FILM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480033759.4 | HIGH FRQUENCY THIN FILM ELECTRICAL CIRCUIT ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480033949.6 | APPARATUS AND METHOD FOR TIME ORDERING EVENTS IN A SYSTEM HAVING MULTIPLE TIME DOMAINS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480035312.0 | LOW-POWER COMPILER-PROGRAMMABLE MEMORY WITH FAST ACCESS TIMING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480039244.5 | LOW IF RADIO RECEIVER |

| FREESCALE SEMICONDUCTOR, INC. | CN | 200480039266.1 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT, AND SEMICONDUCTOR COMPONENT FORMED THEREBY |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 200480039842.2 | LAND GRID ARRAY PACKAGED DEVICE AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480043491.2 | ARRANGEMENT AND METHOD FOR DUAL MODE OPERATION IN A COMMUNICATION SYSTEM TERMINAL |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480044103.2 | POWER SUPPLY APPARATUS WITH OVERLOAD PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480044181.2 | REFERENCE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480044253.3 | METHOD FOR FORMING A PHOTORESIST PATTERN |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480044264.1 | APPARATUS AND CONTROL INTERFACE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480044321.6 | MEMORY MANAGEMENT UNIT AND A METHOD FOR MEMORY MANAGEMENT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480044449.2 | INTEGRATED CIRCUIT AND A METHOD FOR TESTING A MULTI-TAP INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480044499 | APPARATUS FOR REDUCING POWER CONSUMPTION USING SELECTIVE POWER GATING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480044507.1 | APPARATUS AND METHOD FOR CONTROLLING VOLTAGE AND FREQUENCY USING MULTIPLE REFERENCE CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480044591.7 | APPARATUS AND METHOD FOR DETECTING AN END POINT OF AN INFORMATION FRAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580004396.6 | DIE ENCAPSULATION USING A POROUS CARRIER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580004804.8 | METHOD OF MAKING A SEMICONDUCTOR DEVICE USING TREATED PHOTORESIST |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580006039.3 | UNIVERSAL SERIAL BUS TRANSMITTER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580006512.8 | MULTIPLE BURST PROTOCOL DEVICE CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580006770.6 | AUTONOMOUS MEMORY CHECKER FOR RUNTIME SECURITY ASSURANCE AND METHOD THEREFORE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580006812.6 | INTEGRATED CIRCUIT WITH MULTIPLE SPACER INSULATING REGION WIDTHS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580007554.3 | METHOD OF MAKING A SEMICONDUCTOR DEVICE, AND SEMICONDUCTOR DEVICE MADE THEREBY |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580008021.7 | MULTIPLE-STAGE FILTERING DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580009120.7 | METHOD AND APPARATUS FOR DOHERTY AMPLIFIER BIASING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580009296.2 | LAND GRID ARRAY PACKAGED DEVICE AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580009302.4 | METHOD AND APPARATUS FOR ENTERING A LOW POWER MODE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580009700.6 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING A NOTCHED CONTROL ELECTRODE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580011642.0 | MOTION SENSING FOR TIRE PRESSURE MONITORING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580011653.9 | METHOD FOR FORMING A GATE ELECTRODE HAVING A METAL |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580011654.3 | METHOD FOR MAKING A SEMICONDUCTOR STRUCTURE |

USING SILICON GERMANIUM

| FREESCALE SEMICONDUCTOR, INC. | CN | 200580013128.0 | SEMICONDUCTOR DEVICE WITH A PROTECTED ACTIVE DIE REGION AND METHOD THEREFOR |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 200580013499.9 | ISOLATION TRENCH |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580013700.3 | MASKING WITHIN A DATA PROCESSING SYSTEM HAVING APPLICABILITY FOR A DEVELOPMENT INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580014114.0 | STATE RETENTION WITHIN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580014355.5 | CIRCUIT FOR PERFORMING VOLTAGE REGULATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580015236.1 | SEPARATELY STRAINED N-CHANNEL AND P-CHANNEL TRANSISTORS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580015533 | METHOD AND APPARATUS HAVING A DIGITAL PWM SIGNAL GENERATOR WITH INTEGRAL NOISE SHAPING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580016632.6 | METHOD AND APPARATUS FOR ENDIANNESS CONTROL IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580016887.2 | AUTOMATIC HIDDEN REFRESH IN A DRAM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580016892.3 | DECOUPLED COMPLEMENTARY MASK PATTERNING TRANSFER METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580017137.7 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING A SILICIDE LAYER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580017337.2 | SCHOTTKY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580017401.7 | MEMORY WITH RECESSED DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580018315.8 | WIRELESS TRANSCEIVER AND METHOD OF OPERATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580018879 | A MEMORY CACHE CONTROL ARRANGMENT AND A METHOD OF PERFORMING A COHERENCY OPERATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580018902.7 | MEMORY DEVICE WITH A DATA HOLD LATCH |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580020377.2 | ULTRA-THIN DIE AND METHOD OF FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580020481.1 | METHOD FOR ASSEMBLING A SEMICONDUCTOR COMPONENT AND APPARATUS THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580020970.7 | METHOD OF FORMING A NANOCLUSTER CHARGE STORAGE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580021085.0 | METHOD OF FORMING A NANOCLUSTER CHARGE STORAGE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580021794.9 | LEAD SOLDER INDICATOR AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580021992.5 | SCHOTTKY DEVICE AND METHOD OF FORMING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580022721.1 | METHOD AND SYSTEM FOR PERFORMING DEBLOCKING FILTERING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580022869.5 | METHOD AND SYSTEM FOR DISPLAYING A SEQUENCE OF IMAGE FRAMES |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580023883.7 | INTERFACIAL LAYER FOR USE WITH HIGH K DIELECTRIC MATERIALS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580024276 | TRANSISTOR STRUCTURE WITH STRESS MODIFICATION AND CAPACITIVE REDUCTION FEATURE IN A WIDTH DIRECTION AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580024860.8 | METHOD AND APPARATUS FOR MOBILITY ENHANCEMENT IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580026056 | MULTYLAYER CAVITY SLOT ANTENNA |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580026474.2 | MEMORY BIT LINE SEGMENT ISOLATION |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 200580027261.1 | METHOD AND APPARATUS FOR PERFORMANCE ENHANCEMENT IN AN ASYMMETRICAL SEMICONDUCTOR DEVICE |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 200580027928.8 | GRADED SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580029056.9 | MRAM SENSE AMPLIFIER HAVING A PRECHARGE CIRCUIT AND METHOD FOR SENSING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580031462.9 | METHOD AND APPARATUS FOR PROTECTING AN INTEGRATED CIRCUIT FROM ERRONEOUS OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580031541 | PROGRAMMING AND ERASING STRUCTURE FOR A FLOATING GATE MEMORY CELL AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580032673.4 | DATA PROCESSING SYSTEM WITH BUS ACCESS RETRACTION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580032682.3 | DATA PROCESSING SYSTEM WITH BUS ACCESS RETRACTION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580034575.4 | TRANSISTOR STRUCTURE WITH DUAL TRENCH FOR OPTIMIZED STRESS EFFECT AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580034886.0 | METHOD AND APPARATUS FOR NON-INTRUSIVE TRACING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580035470.0 | METHOD AND APPARATUS FOR MODIFYING AN INFORMATION UNIT USING AN ATOMIC OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580036220.9 | PACKAGED DEVICE AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580039178.6 | TEMPERATURE BASED DRAM REFRESH |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580040911 | SYSTEM AND METHOD FOR FALL DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580040951.0 | METHOD AND APPARATUS FOR PROVIDING STRUCTURAL SUPPORT FOR INTERCONNECT PAD WHILE ALLOWING SIGNAL CONDUCTANCE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580041161 | METHOD FOR SHARING BANDWIDTH USING REDUCED DUTY CYCLE SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580041206.8 | METAL GATE TRANSISTOR FOR CMOS PROCESS AND METHOD FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580041207.2 | SEMICONDUCTOR DEVICE HAVING NITRIDATED OXIDE LAYER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580042556 | SEMICONDUCTOR FABRICATION PROCESS INCLUDING RECESSED SOURCE/DRAIN REGIONS IN AN SOI WAFER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580047441.6 | NON-HIGH IMPEDENCE DEVICE AND METHOD FOR REDUCING ENERGY CONSUMPTION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580048015 | I/O CELL ESD SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580048555.2 | SMART POWER REGULATION IN LOW COST BATTERY CHARGING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580049940.9 | METHOD AND DEVICE FOR TRANSMITTING A SEQUENCE OF TRANSMISSION BURSTS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580050162.5 | SPREAD SPECTRUM CLOCK AND METHOD FOR MESSAGE TIMING IN A COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580050954.2 | DEVICE AND METHOD FOR ARBITRATING BETWEEN DIRECT MEMORY ACCESS TASK REQUEST |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580050963.1 | DEVICE AND METHOD FOR CONTROLLING AN EXECUTION |

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| FREESCALE SEMICONDUCTOR, INC. | CN | 200580051173.5 | POWER SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING A POWER SEMICONDUCTOR DEVICE |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 200580052356.9 | IMPROVEMENTS IN OR RELATING TO LEAD FRAME BASED SEMICONDUCTOR PACKAGE AND A METHOD OF MANUFACTURING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200610004518.8 | THREE DIMENSIONAL PACKAGE AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200610063937.9 | METHOD OF MAKING SEMICONDUCTOR PACKAGE WITH REDUCED MOISTURE SENSITIVITY |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200610107552 | PACKAGED SEMICONDUCTOR DEVICE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200610109103 | MEMORY ACCESS CONTROL APPARATUS AND METHOD THEREOF, MEMORY ACCESS CONTROLLER AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200610126706.8 | HIGH SPEED MMC/SDCOMBO OTG |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200610163074 | LOW VOLTAGE LOW POWER CLASS A/B OUTPUT STAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200610163075.7 | METHOD FOR PACKAGING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200610164089.0 | METHOD OF MAKING EXPOSED PAD BALL GRID ARRAY PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200610164627 | DIGITAL CLOCK FREQUENCY MULTIPLIER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680001278 | METHOD AND APPARATUS FOR DYNAMIC DETERMINATION OF FRAMES REQUIRED TO BUILD A COMPLETE PICTURE IN A MPEG VIDEO STREAM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680003369.1 | METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING ASYMMETRIC DIELECTRIC REGIONS AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680005812.9 | MULTIPLE REFERENCE CLOCK SYNTHESIZER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680008837.4 | APPARATUS FOR CURRENT SENSING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680008880 | INTERLAYER DIELECTRIC UNDER STRESS FOR AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680010176 | SYSTEM AND METHOD FOR PROTECTING LOW VOLTAGE TRANSCEIVER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680013713 | MEMORY STRUCTURE AND METHOD OF PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680013750.6 | SCHOTTKY DEVICE AND METHOD OF FORMING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680013835.4 | NICAM ENCODER WITH A FRONT-END |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680014629 | LOGIC THRESHOLD ACQUISITION CIRCUITS AND METHODS USING REVERSED PEAK DETECTORS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680014664.7 | VARIABLE INTERPOLATOR FOR NON-UNIFORMLY SAMPLED SIGNALS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680016232 | TRANSLATION INFORMATION RETRIEVAL |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680018192.2 | SELF-ALIGNING RESONATOR FILTER CIRCUIT AND WIDEBAND TUNER CIRCUIT INCORPORATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680018216.4 | SEMICONDUCTOR PACKAGE AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680022503 | CHEMICAL DIE SINGULATION TECHNIQUE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680027319.7 | PROCESS FOR FORMING AN ELECTRONIC DEVICE INCLUDING DISCONTINUOUS STORAGE ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680027480 | STRESS RELEASE MECHANISM IN MEMS DEVICE AND |

METHOD OF MAKING SAME

| FREESCALE SEMICONDUCTOR, INC. | CN | 200680027775.1 | PACKAGED INTEGRATED CIRCUIT WITH ENHANCED THERMAL DISSIPATION |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 200680027834.5 | FABRICATION OF THREE DIMENSIONAL INTEGRATED CIRCUIT EMPLOYING MULTIPLE DIE PANELS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680030445 | A BOUNDED SIGNAL MIXER AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680030563.9 | NONVOLATILE MEMORY CELL PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680031794.1 | MEMORY WITH ROBUST DATA SENSING AND METHOD FOR SENSING DATA |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680032674.3 | GROOVED PLATEN WITH CHANNELS OR PATHWAY TO AMBIENT AIR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680033654.8 | SEMICONDUCTOR STACKED DIE/WAFER CONFIGURATION AND PACKAGING AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680033747.0 | SEMICONDUCTOR FABRICATION PROCESS INCLUDING SILICIDE STRINGER REMOVAL PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680035716.9 | MICROELECTRONIC ASSEMBLY AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680035922 | POWER CONTROL FEEDBACK LOOP FOR ADJUSTING A MAGNITUDE OF AN OUTPUT SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680035940.8 | METHOD AND SYSTEM FOR CONTROLLING A NOTCHING MECHANISM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680036010 | SYSTEM AND METHOD FOR ADJUSTING ACQUISITION PHASE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680036351 | MICROELECTRONIC ASSEMBLY AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680037947 | PROGRAMMABLE FUSE WITH SILICON GERMANIUM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680038211.8 | VOLTAGE CONTROLLED OSCILLATOR WITH A MULTIPLE GATE TRANSISTOR AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680038265.4 | SIGNAL CONVERTERS WITH MULTIPLE GATE DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680039193.5 | SYSTEM AND METHOD OF CODING MODE DECISION FOR VIDEO ENCODING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680039742.9 | SEMICONDUCTOR STRUCTURE AND METHOD OF ASSEMBLY |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680039798.4 | PLASTIC PACKAGED DEVICE WITH DIE INTERFACE LAYER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680040100 | LOW NOISE REFERENCE OSCILLATOR WITH FAST START-UP |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680040315.2 | ELECTRONIC ASSEMBLY HAVING GRADED WIRE BONDING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680041548.4 | FINE PITCH INTERCONNECT AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680041793.5 | ELECTRONIC DEVICE INCLUDING A TRANSISTOR STRUCTURE HAVING AN ACTIVE REGION ADJACENT TO A STRESSOR LAYER AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680043309.2 | LATERALLY GROWN NANOTUBES AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680043572.1 | PERFORMING AN N-BIT WRITE ACCESS TO AN MXN-BIT-ONLY PERIPHERAL |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680044254 | METHOD AND APPARATUS FOR PROGRAMMING/ERASING A |

NON-VOLATILE MEMORY

| FREESCALE SEMICONDUCTOR, INC. | CN | 200680044898 | METHOD AND PROGRAM PRODUCT FOR PROTECTING INFORMATION IN EDA TOOL DESIGN VIEWS |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 200680045057.7 | PLASMA TREATMENT OF A SEMICONDUCTOR SURFACE FOR ENHANCED NUCLEATION OF A METAL-CONTAINING LAYER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680046879.7 | BACK-GATED SEMICONDUCTOR DEVICE WITH A STORAGE LAYER AND METHODS FOR FORMING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680047227 | ESD PROTECTION FOR PASSIVE INTEGRATED DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680047257.6 | SEMICONDUCTOR DEVICE HAVING STRESSORS AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680051775.5 | WARPAGE-REDUCING PACKAGING DESIGN |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680051815.6 | SEMICONDUCTOR INTERCONNECT HAVING ADJACENT RESERVOIR FOR BONDING AND METHOD FOR FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680051880.9 | MEMORY CELL USING A DIELECTRIC HAVING NON-UNIFORM THICKNESS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680051905.5 | SPLIT GATE MEMORY CELL IN A FINFET |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680052189 | GROUND SHIELDS FOR SEMICONDUCTORS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680054962.9 | A METHOD AND DEVICE FOR PROVIDING A SECURITY BREACH INDICATIVE AUDIO ALERT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680055561.5 | REAL TIME CLOCK MONITORING METHOD AND SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200680055897 | SEMI-FLOATING ISLAND MOSFET DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200710001667.3 | METHOD AND APPARATUS FOR INTER FACING A PROCESSOR TO A COPROC ESSOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200710002381 | METHOD AND APPARATUS FOR GEOMETRIC TRANSFORMATION IN VIDEO REPRODUCTION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200710004727.7 | METHOD OF PACKAGING SEMICONDUCTOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200710084392.4 | MULTI-ROW LEAD FRAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200710085084.3 | CAPACITOR ATTACHMENT METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200710103556.3 | METHOD FOR FORMING REINFORCED INTERCONNECTS ON A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200710109596 | STACKED LOOP ANTENNA |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200710180243 | METHOD OF FORMING PREMOLDED LEAD FRAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200710184806 | COATED LEAD FRAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200710196264.9 | NON-VOLATILE MEMORY DEVICE AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780005027.8 | METHOD AND APPARATUS FOR FORMING A SEMICONDUCTOR-ON-INSULATOR (SOI) BODY-CONTACTED DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780006446.3 | NOISE ISOLATION BETWEEN CIRCUIT BLOCKS IN AN INTEGRATED CIRCUIT CHIP |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780006581 | CAP LAYER FOR AN ALUMINUM COPPER BOND PAD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780006591.1 | SEMICONDUCTOR PROCESS INTEGRATING SOURCE/DRAIN STRESSORS AND INTERLEVEL DIELECTRIC LAYER STRESSORS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780006767.3 | PIEZOELECTRIC MEMS SWITCHES AND METHODS OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780006887 | BIT LINE PRECHARGE IN EMBEDDED MEMORY |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 200780008128 | ENHANCED TONE DETECTOR INCLUDING ADAPTIVE MULTI-BANDPASS FILTER FOR TONE DETECTION AND ENHANCEMENT |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 200780008570 | NON-VOLATILE MEMORY WITH CONTROLLED PROGRAM/ERASE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780008572.2 | SILICON DEPOSITION OVER DUAL SURFACE ORIENTATION SUBSTRATES TO PROMOTE UNIFORM POLISHING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780008662.1 | POLISHING PAD, A POLISHING APPARATUS, AND A PROCESS FOR USING THE POLISHING PAD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780008885.8 | SILICIDED NONVOLATILE MEMORY AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780009320 | METHOD OF FORMING A SEMICONDUCTOR DEVICE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780010978 | ERROR CORRECTION DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780011028.3 | METHOD OF SEPARATING STRUCTURE IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780011108.9 | PROGRAMMABLE STRUCTURE INCLUDING CONTROL GATE OVERLYING SELECT GATE FORMED IN A TRENCH |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780011128 | MEMORY WITH CLOCKED SENSE AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780012308.6 | ESD PROTECTION CIRCUIT WITH ISOLATED DIODE ELEMENT AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780013228.2 | TRANSISTOR AND METHOD WITH DUAL LAYER PASSIVATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780013844 | MEMORY CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780014596.9 | CHARGE STORAGE STRUCTURE FORMATION IN TRANSISTOR WITH VERTICAL CHANNEL REGION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780017610 | MEMORY WITH LEVEL SHIFTING WORD LINE DRIVER AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780018478.5 | CONTACT SURROUNDED BY PASSIVATION AND POLYIMIDE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780019293 | METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING AN INTERLAYER AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780019691 | ENGINEERING STRAIN IN THICK STRAINED-SOI SUBSTRATES |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780020417 | DIE LEVEL METAL DENSITY GRADIENT FOR IMPROVED FLIP CHIP PACKAGE RELIABILITY |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780020522 | SLEW-RATE CONTROL APPARATUS AND METHODS FOR A POWER TRANSISTOR TO REDUCE VOLTAGE TRANSIENTS DURING INDUCTIVE FLYBACK |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780021020 | DATA COMMUNICATION FLOW CONTROL DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780024544 | INTEGRATED CIRCUIT HAVING A MEMORY WITH LOW VOLTAGE READ/WRITE OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780024707.4 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780026669 | TRANSISTOR WITH ASYMMETRY FOR DATA STORAGE CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780028190.6 | SRAM HAVING VARIABLE POWER SUPPLY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780028759.9 | METHOD FOR REMOVING NANOCLUSTERS FROM SELECTED REGIONS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780032167 | LEVEL SHIFTING CIRCUIT |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 200780034147 | LOCALIZED CONTENT ADAPTIVE FILTER FOR LOW POWER SCALABLE IMAGE PROCESSING |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 200780036733.9 | SENSOR HAVING FREE FALL SELF-TEST CAPABILITY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780037565.5 | DISTRIBUTED ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT WITH VARYING CLAMP SIZE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780038309.8 | ONE TRANSISTOR DRAM CELL STRUCTURE AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780039169 | TWO-PORT SRAM HAVING IMPROVED WRITE OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780039340 | METHOD OF PACKAGING A SEMICONDUCTOR DEVICE AND A PREFABRICATED CONNECTOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780039476 | METHODS AND APPARATUS FOR A QUAD FLAT NO-LEAD (QFN) PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780039557 | METHOD OF PACKAGING A DEVICE USING A DIELECTRIC LAYER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780039909 | SYSTEM AND METHOD FOR REDUCING EDGE EFFECT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780044600 | FORMING A SEMICONDUCTOR DEVICE HAVING A METAL ELECTRODE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780049096 | WIRELESS COMMUNICATION DEVICE, INTEGRATED CIRCUIT AND METHOD OF TIMING SYNCHRONISATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780049284 | SEMICONDUCTOR DEVICE AND METHOD OF FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780049637 | CALIBRATING A DIGITAL-TO-ANALOG CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780052369 | METHOD AND APPARATUS FOR VARYING A DYNAMIC RANGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780052927 | POWER LEAD-ON-CHIP BALL GRID ARRAY PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780052930 | DIGITAL SQUIB DRIVER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780100205 | MOTOR CONTROLLER FOR DETERMINING A POSITION OF A ROTOR OF AN AC MOTOR, AC MOTOR SYSTEM, AND METHOD OF DETERMINING A POSITION OF A ROTOR OF AN AC MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780100966.0 | MICROPROCESSOR, SYSTEM FOR CONTROLLING A DEVICE AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780101229 | METHOD, INTEGRATED CIRCUIT, AND COMMUNICATION UNIT FOR SCHEDULING A PROCESSING OF PACKET STREAM CHANNELS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200810003247.3 | SEMICONDUCTOR WAFER WITH IMPROVED CRACK PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200810087126 | MOLDING WITH DUAL CAVITY TOOL TO INCREASE xQFN LEADS STAND-OFF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200810098969.1 | METHOD OF FORMING FLIP-CHIP BUMP CARRIER TYPE PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200810130229.1 | OUTPUT CORRECTION CIRCUIT FOR THREE-AXIS ACCELEROMETER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200810144568 | DATA PROCESSING SYSTEM IMPLEMENTING SIMD OPERATIONS AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880001261.8 | METHOD OF MAKING A SEMICONDUCTOR DEVICE HAVING HIGH VOLTAGE TRANSISTORS, NON-VOLATILE MEMORY TRANSISTORS, AND LOGIC TRANSISTORS |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 200880001389.4 | METHOD OF MAKING A NON-VOLATILE MEMORY DEVICE |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 200880001563 | DYNAMIC PAD SIZE TO REDUCE SOLDER FATIGUE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880003292 | MEMORY HAVING A DUMMY BITLINE FOR TIMING CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880004638 | SUCCESSIVE INTERFERENCE CANCELLATION BASED ON THE NUMBER OF RETRANSMISSIONS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880006417.1 | CONDUCTIVE VIA FORMATION UTILIZING ELECTROPLATING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880007878.0 | ELECTRONIC DEVICE INCLUDING CHANNEL REGIONS LYING AT DIFFERENT ELEVATIONS AND PROCESSES OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880008799 | SELF-TEST STRUCTURE AND METHOD OF TESTING A DIGITAL INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880010706 | A FIRST INTER-LAYER DIELECTRIC STACK FOR NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880014713 | METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE TYPES OF SCHOTTKY JUNCTIONS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880015236 | LOW VOLTAGE DATA PATH IN MEMORY ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880016888 | BITCELL WITH VARIABLE-CONDUCTANCE TRANSFER GATE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880018021.9 | MULTIPLE MILLISECOND ANNEALS FOR SEMICONDUCTOR DEVICE FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880018202.1 | METHOD OF FORMING A SEMICONDUCTOR DEVICE FEATURING A GATE STRESSOR AND SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880022723.4 | METHOD FOR FORMING A DUAL METAL GATE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880022833.0 | METHOD FOR FORMING A DUAL METAL GATE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880022994 | HETERO-STRUCTURE FIELD EFFECT TRANSISTOR, INTEGRATED CIRCUIT INCLUDING A HETERO-STRUCTURE FIELD EFFECT TRANSISTOR AND METHOD FOR MANUFACTURING A HETERO-STRUCTURE FIELD EFFECT TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880024566 | TRANSISTOR WITH DIFFERENTLY DOPED STRAINED CURRENT ELECTRODE REGION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880101808 | METHOD AND CIRCUIT FOR PREVENTING HIGH VOLTAGE MEMORY DISTURB |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880102331 | STRESS RELIEF OF A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880103565 | MODE TRANSITIONING IN A DC/DC CONVERTER USING A CONSTANT DUTY CYCLE DIFFERENCE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880104603 | METHOD OF PACKAGING AN INTEGRATED CIRCUIT DIE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880105720 | DUAL GATE OXIDE DEVICE INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880107052 | ELECTROMAGNETIC SHIELD FORMATION FOR INTEGRATED CIRCUIT DIE PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880108954 | SYSTEM AND METHOD FOR MONITORING DEBUG EVENTS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880109855 | PROGRAMMABLE ROM USING TWO BONDED STRATA AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880111918 | TOUCH PANEL DETECTION CIRCUITRY AND METHOD OF |

OPERATION

| FREESCALE SEMICONDUCTOR, INC. | CN | 200880112652 | INTEGRATED CIRCUIT MEMORY HAVING DYNAMICALLY ADJUSTABLE READ MARGIN AND METHOD THEREFOR |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 200880114023 | METHOD FOR INTEGRATING NVM CIRCUITRY WITH LOGIC CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880115226 | KNOCK SIGNAL DETECTION IN AUTOMOTIVE SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880118876 | SEMICONDUCTOR DEVICE AND APPARATUS SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880119243 | METHOD FOR TESTING A SEMICONDUCTOR DEVICE AND A SEMICONDUCTOR DEVICE TESTING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880122037 | ELECTRONIC ASSEMBLY MANUFACTURING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880122050 | LIQUID LEVEL SENSING DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880122700 | 3-D SEMICONDUCTOR DIE STRUCTURE WITH CONTAINING FEATURE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880123823 | MICROPAD FORMATION FOR A SEMICONDUCTOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880125793 | ELECTROSTATIC DISCHARGE PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880128378.2 | MICROPROCESSOR HAVING A LOW-POWER MODE AND A NON-LOW POWER MODE, DATA PROCESSING SYSTEM AND COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200910132108 | METHOD AND APPARATUS FOR PROVIDING STRUCTURAL SUPPORT FOR INTERCONNECT PAD WHILE ALLOWING SIGNAL CONDUCTANCE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980101789.7 | NON-VOLATILE MEMORY WITH REDUCED CHARGE FLUENCE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980105625 | ADJUSTABLE PIPELINE IN A MEMORY CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980112796 | SPRING MEMBER FOR USE IN A MICROELECTROMECHANICAL SYSTEMS SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980115772 | MULTI-VOLTAGE ELECTROSTATIC DISCHARGE PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980119818 | CAPACITIVE SENSOR WITH STRESS RELIEF THAT COMPENSATES FOR PACKAGE STRESS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980120339.2 | SEMICONDUCTOR DEVICE WITH REDUCED SENSITIVITY TO PACKAGE STRESS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980129054 | BURIED ASSYMETRIC JUNCTION ESD PROTECTION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980132363 | TRANSISTOR WITH GAIN VARIATION COMPENSATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980133735 | POWER MOSFET WITH A GATE STRUCTURE OF DIFFERENT MATERIAL |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980133741 | ERROR DETECTION SCHEMES FOR A UNIFIED CACHE IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980144408 | TECHNIQUE FOR INTERCONNECTING INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201010105985 | CIRCUIT AND METHOD FOR INTERPOLATIVE DELAY |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602004004064.9 | UNIVERSAL SERIAL BUS TRANSMITTER |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602004006973.6 | A DRIVE ARRANGEMENT FOR ACTIVATING A CAR SAFETY DEVICE ACTIVATION ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602004012966.6 | SERIAL DATA BUS COMMUNICATION SYSTEM |
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| FREESCALE SEMICONDUCTOR, INC. | DE | 602004013057.5 | APPARATUS AND METHOD FOR DETECTING AN END POINT OF AN INFORMATION FRAME |
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| FREESCALE SEMICONDUCTOR, INC. | DE | 602004013186.5 | A DECODER FOR A WIRELESS COMMUNICATION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602004013917.3 | LOW DROP-OUT DC VOLTAGE REGULATOR |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602004016579.4 | INTEGRATED CIRCUIT AND A METHOD FOR TESTING A MULTI-TAP INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602004016972.2 | DATA CACHE SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602004019827.7 | INTEGRATED CIRCUIT AND A METHOD FOR SECURE TESTING |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602004020015.8 | ANALOG TO DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602004023714.0 | NON-VOLATILE MEMORY HAVING A BIAS ON THE SOURCE ELECTRODE FOR HCI PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602004025556.4 | A MEMORY CACHE CONTROL ARRANGMENT AND A METHOD OF PERFORMING A COHERENCY OPERATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602004034368.4 | METHOD AND SYSTEM FOR IMPROVING THE DESIGN OF SEMICONDUCTOR INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602004034864.3 | SIGNAL GENERATION POWER MANAGEMENT CONTROL SYSTEM FOR PORTABLE COMMUNICATIONS DEVICE AND METHOD OF USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602004035625.5 | A VIRTUAL ADDRESS CACHE AND METHOD FOR SHARING DATA USING A UNIQUE TASK IDENTIFIER |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005007520.8 | NON-HIGH IMPEDENCE DEVICE AND METHOD FOR REDUCING ENERGY CONSUMPTION |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005014021.2 | METHOD FOR TESTING A SLURRY USED TO FORM A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005015632.1 | DEVICE AND METHOD FOR CONTROLLING MULTIPLE DMA TASK |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005016612.2 | TWISTED PAIR COMMUNICATION SYSTEM, APPARATUS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005016615.7 | COMPENSATION FOR PARASITIC COUPLING BETWEEN RF OR MICROWAVE TRANSISTORS IN THE SAME PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005017490.7 | METHOD OF SEMICONDUCTOR FABRICATION INCORPORATING DISPOSABLE SPACER INTO ELEVATED SOURCE/DRAIN PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005017948.8 | DEVICE AND METHOD FOR ARBITRATING BETWEEN DIRECT MEMORY ACCESS TASK REQUEST |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005018114.8 | METHOD FOR NOISE REDUCTION IN A PHASE LOCKED LOOP AND A DEVICE HAVING NOISE REDUCTION CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005019985.3 | MULTIPLE BURST PROTOCOL DEVICE CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005020772.4 | AUTOMATIC HIDDEN REFRESH IN A DRAM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005021549.2 | METHOD AND DEVICE FOR TRANSMITTING A SEQUENCE OF TRANSMISSION BURSTS |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005021994.3 | SELF ADJUSTING REGULATOR AND MONITOR CIRCUITS ON AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005022126.3 | A METHOD FOR MANAGING MULTI-FRAMES AND A DEVICE |

HAVING MULTI-FRAME MANAGEMENT CAPABILITES

| FREESCALE SEMICONDUCTOR, INC. | DE | 602005022229.4 | NON-VOLATILE NANOCRYSTAL MEMORY AND METHOD THEREFOR |
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| FREESCALE SEMICONDUCTOR, INC. | DE | 602005022230.8 | METHOD FOR RACE PREVENTION AND A DEVICE HAVING RACE PREVENTION CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005022370.3 | A METHOD FOR PROCESSING ATM CELLS AND A DEVICE HAVING ATM CELL PROCESSING CAPABILITES |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005023542.6 | DEVICE AND METHOD FOR EXECUTING A DMA TASK |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005024317.8 | CURRENT DRIVER AND METHOD OF OPERATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005025534.6 | METHOD OF FABRICATING A SILICON-ON-INSULATOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005027003.5 | DEVICE AND METHOD FOR CONTROLLING AN EXECUTION OF A DMA TASK |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005027266.6 | POWER SAVING IN A SIGNAL PROCESSING IN RECEIVERS |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005028180.0 | CURRENT DRIVER AND METHOD OF OPERATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005032157.8 | METHOD AND APPARATUS FOR MODIFYING AN INFORMATION UNIT USING AN ATOMIC OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005034225.7 | SYSTEM AND METHOD FOR FALL DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005035288.0 | A DEVICE HAVIING A LOW LATENCY SINGLE PORT MEMORY UNIT AND A METHOD FOR WRITING MULTIPLE DATA SEGMENTS TO A SINGLE PORT MEMORY UNIT |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005036673.3 | MOTION SENSING FOR TIRE PRESSURE MONITORING |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005036882.5 | DECOUPLED COMPLEMENTARY MASK PATTERNING TRANSFER METHOD |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005040051.6 | METHOD FOR FORMING A GATE ELECTRODE HAVING A METAL |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602005041105.4 | METHOD OF MAKING A SEMICONDUCTOR DEVICE, AND SEMICONDUCTOR DEVICE MADE THEREBY |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602006013202.6 | REAL TIME CLOCK MONITORING METHOD AND SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602006014598.5 | APPARATUS FOR DETECTING CLOCK FAILURE AND METHED THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602006016021.6 | LIN NETWORK, INTEGRATED CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602006018075.6 | DEVICE AND METHOD FOR TESTING INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602006019003.4 | AMPLIFIER CIRCUIT AND INTEGRATED CIRCUIT THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602006019920.1 | DATA COMMUNICATION UNIT, INTEGRATED CIRCUIT AND METHOD FOR BUFFERING DATA |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602006020357.8 | RECEIVER FOR RECEIVING AT LEAST TWO TYPES OF SIGNALS, DATA COMMUNICATION SYSTEM AND VEHICLE INCLUDING A RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602006021635.1 | A NON-VOLATILE MEMORY DEVICE AND PROGRAMMABLE VOLTAGE REFERENCE FOR A NON-VOLATILE MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602006022920.8 | LIN NETWORK, INTEGRATED CIRCUIT AND METHOD OF COMMUNICATING THEREON |

| FREESCALE SEMICONDUCTOR, INC. | DE | 602006028343.1 | METHOD OF CONTROL SLOPE REGULATION AND CONTROL SLOPE REGULATION APPARATUS |
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| FREESCALE SEMICONDUCTOR, INC. | DE | 602006029219.8 | SOFTWARE PIPELINING |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602006032980.6 | SEMI-FLOATING ISLAND MOSFET DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602006035629.3 | MICROELECTRONIC ASSEMBLY AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602006035760.5 | MICROELECTRONIC ASSEMBLY AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602007004461.8 | APPARATUS FOR DETECTING CLOCK FAILURE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602007010039.9 | SYSTEM, COMPUTER PROGRAM PRODUCT AND METHOD FOR TESTING A LOGIC CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602007013765.9 | MEMORY CIRCUIT USING A REFERENCE FOR SENSING |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602007013956.2 | POWER MANAGEMENT ARRANGEMENT AND MOBILE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602007014122.2 | DATA PACKET FREQUENCY |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602007014755.7 | IMPROVEMENTS IN OR RELATING TO DIAGNOSTICS OF A CAPACITIVE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602007014756.5 | METHOD AND APPARATUS FOR CONVERTING SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602007016439.7 | DATA PROCESSING SYSTEM, DATA PROCESSING METHOD, AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602007016563.6 | REQUEST CONTROLLER, PROCESSING UNIT, METHOD FOR CONTROLLING REQUESTS AND COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602007021942.6 | DATA PROCESSOR HAVING DYNAMIC CONTROL OF INSTRUCTION PREFETCH BUFFER DEPTH AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602007023633.9 | ADJUSTABLE NOISE SUPPRESSION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602007026566.5 | DATA COMMUNICATION FLOW CONTROL DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602007026753.6 | DIFFERENTIAL CAPACITIVE SENSOR AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602007029676.5 | SEMICONDUCTOR PROCESS INTEGRATING SOURCE/DRAIN STRESSORS AND INTERLEVEL DIELECTRIC LAYER STRESSORS |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602007030065.7 | SEMICONDUCTOR DEVICE AND APPARATUS INCLUDING SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602007031444.5 | MICROPROCESSOR, SYSTEM FOR CONTROLLING A DEVICE AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602007032662.1 | METHOD, DATA STRUCTURE AND COMPUTER SYSTEM FOR PACKING A WORLDWIDE INTEROPERABILITY FOR MICROWAVE ACCESS (WIMAX) FRAME |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602008003776.2 | METHOD AND DEVICE FOR PROGRAMMING ANTI-FUSES |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602008007785.3 | BUFFER MODULE, RECEIVER, DEVICE AND BUFFERING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602008011766.9 | PROGRAMMABLE ROM USING TWO BONDED STRATA AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602008012707.9 | MULTI-FREQUENCY TONE DETECTOR |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602008015055.0 | METHOD FOR INTEGRATING NVM CIRCUITRY WITH LOGIC CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602008016319.9 | A SYSTEM, NETWORK NODE, A METHOD AND A COMMUNICATION CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602008021566.0 | A SYSTEM FOR DISTRIBUTING AVAILABLE MEMORY RESOURCE |
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| FREESCALE SEMICONDUCTOR, INC. | DE | 602008022486.4 | A METHOD FOR PROTECTING A CRYPTOGRAPHIC MODULE AND A DEVICE HAVING CRYPTOGRAPHIC MODULE PROTECTION CAPABILITIES |
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| FREESCALE SEMICONDUCTOR, INC. | DE | 602009004851.1 | CHARGE AMPLIFIER WITH DC FEEDBACK SAMPLING |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602009018297.8 | RECEIVING NODE IN A PACKET COMMUNICATIONS SYSTEM AND METHOD FOR MANAGING A BUFFER IN A RECEIVING NODE IN A PACKET COMMUNICATIONS SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602010007963.5 | CAPACITANCE-TO-VOLTAGE INTERFACE CIRCUIT, AND RELATED OPERATING METHODS |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602011001102.2 | DATA PROCESSING SYSTEM WITH PERIPHAL CONFIGURATION INFORMATION ERROR DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | DE | 602011003020.5 | DIFFERENTIAL EQUALIZERS WITH SOURCE DEGENERATION AND FEEDBACK CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-0617993 | METHOD OF MANUFACTURING ELECTRONIC COMPONENTS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-0624041 | METHOD FOR FORMING AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-0633754 | METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE INCLUDING A METAL OXIDE INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-0633755 | DIGITAL COMMUNICATONS PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-0645080 | POWER AMPLIFIER OUTPUT MODULE FOR DUAL-MODE DIGITAL SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-0652546 | INTEGRATED FILTER WITH IMPROVED I/O MATCHING AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-0909538 | MULTIPHASE VOLTAGE CONTROLLED OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-0954019 | DUAL STEERED FREQUENCY SYNTHESIZER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-0966661 | METHOD AND APPARATUS FOR SECURE SCAN TESTING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-0976890 | OSCILLATOR CIRCUIT HAVING REDUCED LAYOUT AREA AND LOWER POWER SUPPLY TRANSIENTS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-0984394 | METHOD AND APPARATUS FOR DETERMINING AN UPPER DATA RATE FOR A VARIABLE DATA RATE SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-0989215 | DATA PROCESSING SYSTEM HAVING MULTIPLE REGISTER CONTEXTS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1001530 | METAL REDUCTION IN WAFER SCRIBE AREA |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1006825 | ELECTRONIC DISCHARGE PROTECTION CIRCUITRY AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1006827 | LOW VOLTAGE NMOS-BASED ELECTROSTATIC DISCHARGE CLAMP |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1010159 | FLIP-CHIP ASSEMBLY WITH THIN UNDERFILL AND THICK SOLDER MASK |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1017533 | MINIATURE MOLDLOCKS FOR HEATSINK OR FLAG FOR AN OVERMOLDED PLASTIC PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1017536 | NETWORK MESSAGE STASHING WITH FILING USING PATTERN MATCHING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1018519 | MULTI-TIERED LITHOGRAPHIC TEMPLATE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1021046 | METHOD AND APPARATUS FOR DYNAMIC PREFETCH BUFFEI CONFIGURATION AND REPLACEMENT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1022638 | MULTI-DIE SEMICONDUCTOR PACKAGE |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1022639 | METHOD AND APPARATUS FOR PROVIDING SECURITY FOR DEBUG CIRCUITRY |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1030923 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1031117 | LOW VOLTAGE DETECTION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1031158 | DATA PROCESSING SYSTEM IMPLEMENTING SIMD OPERATIONS AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1031986 | HYBRID STRUCTURE FOR DISTRIBUTED POWER AMPLIFIERS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1031990 | METHOD OF FORMING SEMICONDUCTOR DEVICES THROUGH EPITAXY |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1034909 | INTEGRATED CIRCUIT POWER MANAGEMENT FOR REDUCING LEAKAGE CURRENT IN CIRCUIT ARRAYS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1036444 | UNIVERSAL SERIAL BUS TRANSMITTER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1036445 | MULTIPLE BURST PROTOCOL DEVICE CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1037287 | METHOD FOR ELIMINATING VOIDING IN PLATED SOLDER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1039244 | NONVOLATILE MEMORY AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1045472 | METHOD AND APPARATUS FOR DYNAMICALLY INSERTING GAIN IN AN ADAPTIVE FILTER SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1045473 | MULTIPLE THICKNESS SEMICONDUCTOR INTERCONNECT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1048576 | INTEGRATED CIRCUIT WITH TEST PAD STRUCTURE AND METHOD OF TESTING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1050554 | MASKING WITHIN A DATA PROCESSING SYSTEM HAVING APPLICABILITY FOR A DEVELOPMENT INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1054238 | WAFER COATING AND SINGULATION METHOD |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1054239 | UNDERFILL FILM FOR PRINTED WIRING ASSEMBLIES |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1054664 | ESD PROTECTION DEVICE AND METHOD OF MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1054665 | INTEGRATED CIRCUIT DIE I/O CELLS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1054673 | SEMICONDUCTOR DEVICE AND MAKING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1054676 | METHOD OF FORMING A LOW K DIELECTRIC IN A SEMICONDUCTOR MANUFACTURING PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1059006 | METHOD TO PASSIVATE CONDUCTIVE SURFACES DURING SEMICONDUCTOR PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1059720 | AMPLITUDE LEVEL CONTROL CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1060034 | NON-VOLATILE MEMORY HAVING A BIAS ON THE SOURCE ELECTRODE FOR HCI PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1064531 | ELECTRONIC COMPONENT AND METHOD OF MANUFACTURNG SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1067563 | METHOD OF PATTERNING PHOTORESIST ON A WAFER USING AN ATTENUATED PHASE SHIFT MASK |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1069120 | APPARATUS AND METHOD FOR TIME ORDERING EVENTS IN A SYSTEM HAVING MULTIPLE TIME DOMAINS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1073822 | PHASE LOCKED LOOP FILTER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1076964 | CIRCUIT VOLTAGE REGULATION |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1076972 | METHOD OF FORMING A SEMICONDUCTOR PACKAGE AND STRUCTURE THEREOF |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1077813 | WIREBONDING INSULATED WIRE AND CAPILLARY THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1078610 | SEMICONDUCTOR ALIGNMENT AID |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1079562 | TRANSISTOR WITH INDEPENDENT GATE STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1080629 | ACTIVATION PLATE FOR ELECTROLESS AND IMMERSION PLATING OF INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1082724 | SYSTEM AND METHOD FOR COARSE TUNING A PHASE LOCKED LOOP (PLL) SYNTHESIZER USING 2-PI SLIP DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1082772 | SEMICONDUCTOR FABRICATION PROCESS WITH ASYMMETRICAL CONDUCTIVE SPACERS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1085279 | ARC LAYER FOR SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1087397 | LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1088645 | HIGH K DIELECTRIC FILM AND METHOD FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1089052 | METHOD AND APPARATUS FOR ALLOCATING ENTRIES IN A BRANCH TARGET BUFFER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1093317 | PREFETCH CONTROL IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1095292 | SEMICONDUCTOR DEVICE WITH NANOCLUSTERS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1095738 | METHOD AND APPARATUS FOR ENTERING A LOW POWER MODE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1098689 | METHOD AND APPARATUS FOR SELECTING CACHE WAYS AVAILABLE FOR REPLACEMENT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1098747 | NETWORK MESSAGE PROCESSING USING INVERSE PATTERN MATCHING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1102257 | MULTIPLEXING OF DIGITAL SIGNALS AT MULTIPLE SUPPLY VOLTAGES IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1102260 | A VIRTUAL ADDRESS CACHE AND METHOD FOR SHARING DATA USING A UNIQUE TASK IDENTIFIER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1102785 | METHOD OF MAKING A SEMICONDUCTOR DEVICE, AND SEMICONDUCTOR DEVICE MADE THEREBY |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1106412 | SEMICONDUCTOR PACKAGE HAVING OPTIMIZED WIRE BOND POSITIONING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1106811 | CLOSED LOOP CURRENT CONTROL CIRCUIT AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1106832 | SEMICONDUCTOR DEVICE WITH STRAIN RELIEVING BUMP DESIGN |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1110942 | ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1110994 | METHOD AND APPARATUS FOR PROTECTING AN INTEGRATED CIRCUIT FROM ERRONEOUS OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1113009 | METHOD AND APPARATUS FOR FORMING AN SOI BODY-CONTACTED TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1114703 | TRANSISTOR HAVING THREE ELECTRICALLY ISOLATED ELECTRODES AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1114896 | SEMICONDUCTOR PACKAGE WITH CROSSING CONDUCTOR ASSEMBLY AND METHOD OF MANUFACTURE |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1115091 | SEMICONDUCTOR STRUCTURE WITH DIFFERENT LATTICE CONSTANT MATERIALS AND METHOD FOR FORMING THE SAME |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1119708 | LAND GRID ARRAY PACKAGED DEVICE AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1120718 | DUAL GAUGE LEADFRAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1120733 | FLIPCHIP QFN PACKAGE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1120770 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING ISOLATION REGIONS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1122517 | AUTONOMOUS MEMORY CHECKER FOR RUNTIME SECURITY ASSURANCE AND METHOD THEREFORE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1125518 | CELLULAR MODEM PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1128260 | METHOD OF MAKING A SEMICONDUCTOR DEVICE USING TREATED PHOTORESIST |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1129070 | INTEGRATED CIRCUIT WITH MULTIPLE SPACER INSULATING REGION WIDTHS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1129078 | LOW-POWER COMPILER-PROGRAMMABLE MEMORY WITH FAST ACCESS TIMING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1132603 | TEMPLATE LAYER FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1140001 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING A NOTCHED CONTROL ELECTRODE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1142314 | CIRCUIT DEVICE WITH AT LEAST PARTIAL PACKAGING AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1145999 | SINGLE PROOF MASS, 3 AXIS MEMS TRANSDUCER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1148316 | METHOD OF PATTERNING ON A WAFER USING A RELECTIVE MASK WITH A MULTI-LAYER ARC |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1148378 | SEMICONDUCTOR DEVICE WITH MAGNETICALLY PERMEABLE HEAT SINK |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1149134 | SEPARATELY STRAINED N-CHANNEL AND P-CHANNEL TRANSISTORS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1158345 | METHOD AND SYSTEM FOR PERFORMING DEBLOCKING FILTERING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1159339 | PROCESS FOR FORMING DUAL METAL GATE STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1165491 | MULTIPLE REFERENCE CLOCK SYNTHESIZER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1165580 | CIRCUIT DEVICE WITH AT LEAST PARTIAL PACKAGING AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1169920 | SEMICONDUCTOR FABRICATION PROCESS INCLUDING RECESSED SOURCE/DRAIN REGIONS IN AN SOI WAFER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1173973 | VARIABLE INTERPOLATOR FOR NON-UNIFORMLY SAMPLED SIGNALS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1174937 | METHODS AND APPARATUS HAVING WAFER LEVEL CHIP SCALE PACKAGE FOR SENSING ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1174994 | METHOD AND APPARATUS FOR PERFORMANCE ENHANCEMENT IN AN ASYMMETRICAL SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1183297 | METHODS AND APPARATUS FOR SYNCHRONIZING DATA TRANSFERRED ACROSS A MULTI-PIN ASYNCHRONOUS SERIAL INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1185685 | METAL GATE TRANSISTOR FOR CMOS PROCESS AND METHOD |

FOR MAKING

| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1196167 | MRAM SENSE AMPLIFIER HAVING A PRECHARGE CIRCUIT AND METHOD FOR SENSING |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1203220 | METHOD AND APPARATUS FOR PROVIDING STRUCTURAL SUPPORT FOR INTERCONNECT PAD WHILE ALLOWING SIGNAL CONDUCTANCE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1215283 | CIRCUIT DEVICE WITH AT LEAST PARTIAL PACKAGING AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1218841 | METHOD AND APPARATUS FOR MOBILITY ENHANCEMENT IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1219067 | NON-VOLATILE NANOCRYSTAL MEMORY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1221232 | SEMICONDUCTOR STACKED DIE/WAFER CONFIGURATION AND PACKAGING AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1221345 | INTERLAYER DIELECTRIC UNDER STRESS FOR AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1221348 | SIGNAL CONVERTERS WITH MULTIPLE GATE DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1227210 | LEAD SOLDER INDICATOR AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1227291 | WORD LINE DRIVER CIRCUIT FOR A STATIC RANDOM ACCESS MEMORY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1228164 | Z-AXIS ACCELEROMETER WITH AT LEAST TWO GAP SIZES AND TRAVEL STOPS DISPOSED OUTSIDE AN ACTIVE CAPACITOR AREA |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1232664 | GROUND SHIELDS FOR SEMICONDUCTORS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1233953 | SCHOTTKY DEVICE AND METHOD OF FORMING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1234002 | SYSTEM AND METHOD FOR FALL DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1237669 | STRUCTURE FOR STACKING AN INTEGRATED CIRCUIT ON ANOTHER INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1238277 | METHOD AND APPARATUS FOR DYNAMIC DETERMINATION OF FRAMES REQUIRED TO BUILD A COMPLETE PICTURE IN A MPEG VIDEO STREAM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1242809 | TEMPERATURE BASED DRAM REFRESH |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1244010 | MEMORY STRUCTURE AND METHOD OF PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1246640 | CONDUCTING METAL OXIDE WITH ADDITIVE AS P-MOS DEVICE ELECTRODE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1246641 | BRANCH TARGET BUFFER ALLOCATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1251676 | SRAM HAVING IMPROVED CELL STABILITY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1252325 | SEMICONDUCTOR STRUCTURE WITH REDUCED GATE DOPING AND METHODS FOR FORMING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1262066 | I/O CELL ESD SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1279234 | METHOD FOR FORMING MULTI-LAYER BUMPS ON A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1279266 | FLEXIBLE MACROBLOCK ORDERING WITH REDUCED DATA TRAFFIC AND POWER CONSUMPTION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1279343 | MULTI-THREADED PROCESSOR ARCHITECTURE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1281243 | METHOD AND APPARATUS FACILITATING MULTI MODE |

INTERFACES

| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1281486 | MICROELECTRONIC ASSEMBLY AND METHOD FOR FORMING THE SAME |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1285576 | METHOD AND APPARATUS FOR PROGRAMMING/ERASING A NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1286881 | LINEAR VOLTAGE CONTROLLED VARIABLE ATTENUATOR WITH LINEAR DB/V GAIN SLOPE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1287750 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1288794 | A BOUNDED SIGNAL MIXER AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1291520 | SYSTEM AND METHOD FOR PROTECTING LOW VOLTAGE TRANSCEIVER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1291522 | VOLTAGE CONTROLLED OSCILLATOR WITH A MULTIPLE GAT TRANSISTOR AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1291525 | ERROR CORRECTION DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1296701 | SEMICONDUCTOR DEVICE WITH REDUCED PACKAGE CROSSTALK AND LOSS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1298425 | RF POWER TRANSISTOR DEVICE WITH HIGH PERFORMANCE SHUNT CAPACITOR AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1299420 | NICAM PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1299421 | SYSTEM AND METHOD OF CODING MODE DECISION FOR VIDEO ENCODING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-1300935 | STRESS RELEASE MECHANISM IN MEMS DEVICE AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-314798 | INTEGRATED IMAGE REJECT MIXER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-861669 | FREQUENCY MODULATOR USING A WAVEFORM GENERATOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-862874 | ARRANGEMENT AND METHOD FOR IMPEDANCE MATCHING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-871575 | AN APPARATUS AND A METHOD FOR PROVIDING DECODED INFORMATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-875377 | A DEVICE AND METHOD FOR PERFORMING STACK POP AND PUSH OPERATIONS IN A PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-909346 | HIGH FREQUENCY SIGNAL ISOLATION IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-922704 | SEMICONDUCTOR POWER DEVICE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-928406 | INCREMENTAL-DELTA ANALOGUE-TO-DIGITAL CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-930841 | MULTI-ROW LEADFRAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-937344 | RECEIVER FOR A SWITCHED SIGNAL ON A COMMUNICATION LINE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-939447 | CIRCUITRY FOR CREATING A SPECTRAL NULL IN A DIFFERENTIAL OUTPUT SWITCHING AMPLIFIER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-939450 | ARTICLE COMPRISING AN OXIDE LAYER ON A GaAs-BASED SEMICONDUCTOR STRUCTURE AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-941014 | APPARATUS AND METHOD FOR POWER MANAGEMENT IN A TIRE PRESSURE MONITORING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-943402 | LITHOGRAPHIC TEMPLATE HAVING A REPAIRED GAP DEFECT |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 10-949447 | METHOD AND APPARATUS FOR DETECTING A STALL CONDITION IN A STEPPING MOTOR |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 10-958043 | HIGH PERFORMANCE INTEGRATED CIRCUIT REGULATOR WITH SUBSTRATE TRANSIENT SUPPRESSION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-961404 | INTEGRATED CIRCUIT DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-967068 | COMMUNICATION APPARATUS INCLUDING DRIVER MEANS FOR APPLYING A SWITCHED SIGNAL TO A COMMUNICATION LINE WITH A CONTROLLED SLEW RATE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-968058 | HIGH FREQUENCY SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-975792 | FIELD EFFECT TRANSISTOR AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-977675 | INTEGRATED CIRCUIT SECURITY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-979080 | SEMICONDUCTOR DEVICE HAVING A WIRE BOND PAD AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-979081 | SEMICONDUCTOR DEVICE HAVING A BOND PAD AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-979661 | DIELECTRIC STORAGE MEMORY CELL HAVING HIGH PERMITTIVITY TOP DIELECTRIC AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-979896 | VARIABLE GAIN AMPLIFIER WITH AUTOBIASING SUPPLY REGULATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-981033 | METHOD AND APPARATUS FOR INTERFACING A PROCESSOR TO A COPROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-981034 | LOW DROP-OUT VOLTAGE REGULATOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-985004 | SIMPLIFICATION OF BALL ATTACH METHOD USING SUPER- SATURATED FINE CRYSTAL FLUX |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-985008 | CAPACITIVE CHARGE PUMP |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-985400 | METHOD AND CIRCUITRY FOR IDENTIFYING WEAK BITS IN AN MRAM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-988448 | RADIO RECEIVER HAVING A VARIABLE BANDWIDTH IF FILTER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-988450 | METHOD AND APPARATUS FOR PROCESSING AN AMPLITUDE MODULATED (AM) SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-993134 | METHOD AND APPARATUS FOR CONTROLLING A DATA PROCESSING SYSTEM DURING DEBUG |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-995478 | PACKAGED SEMICONDUCTOR DEVICE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-998164 | FULL BRIDGE INTEGRAL NOISE SHAPING FOR QUANTIZATION OF PULSE WIDTH MODULATION SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | PH | 1-1997-57488 | LEADFRAME STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | PH | 1-1997-58683 | METHOD FOR MULTIPLEXED JOINING OF SOLDER BUMPS TO VARIOUS SUBSTRATES DURING ASSEMBLY OF AN INTEGRATED CIRCUIT PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | PH | 1-1998-02708 | SEMICONDUCTOR DEVICE HAVING A SUB-CHIP-SCALE PACKAGE STRUCTU RE AND METHOD FOR FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480003886.X | AMPLITUDE LEVEL CONTROL CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200480004696.X | MEMORY HAVING A VARIABLE REFRESH CONTROL AND |

METHOD THEREFOR

| FREESCALE SEMICONDUCTOR, INC. | CN 20048000536 | 1.X METHOD AND SYSTEM FOR DYNAMIC PACKET AGGREGATION IN A WIRELESS NETWORK |
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| FREESCALE SEMICONDUCTOR, INC. | CN 20048000599 | 6.X METHOD OF PATTERNING PHOTORESIST ON A WAFER USING AN ATTENUATED PHASE SHIFT MASK |
| FREESCALE SEMICONDUCTOR, INC. | CN 20048000798 | 6.X MEMORY MANAGEMENT IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN 20048001040 | 1.X CIRCUIT DEVICE WITH AT LEAST PARTIAL PACKAGING AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | CN 20048001134 | 9.X METHOD AND APPARATUS FOR REDUCED POWE CONSUMPTION ADC/DAC CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | CN 20048001141 | 2.X SEMICONDUCTOR FABRICATION PROCESS WITH ASYMMETRICAL CONDUCTIVE SPACERS |
| FREESCALE SEMICONDUCTOR, INC. | CN 20048001739 | 7.X METHOD AND APPARATUS FOR SELECTING CACHE WAYS AVAILABLE FOR REPLACEMENT |
| FREESCALE SEMICONDUCTOR, INC. | CN 20048002410 | 6.X TEMPLATE LAYER FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | CN 20048002973 | 9.X ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | CN 20048003561 | 0.X SIGNAL GENERATION POWER MANAGEMENT CONTROL SYSTEM FOR PORTABLE COMMUNICATIONS DEVICE AND METHOD OF USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN 20058000394 | 1.X FLIPCHIP QFN PACKAGE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN 20058000612 | 4.X SEMICONDUCTOR PACKAGE WITH CROSSING CONDUCTOR ASSEMBLY AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | CN 20058001434 | 9.X METHOD OF SEMICONDUCTOR FABRICATION INCORPORATING DISPOSABLE SPACER INTO ELEVATED SOURCE/DRAIN PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | CN 20058002078 | 1.X LDMOS TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | CN 20058002401 | 7.X CMOS WITH ONLY A SINGLE IMPLANT |
| FREESCALE SEMICONDUCTOR, INC. | CN 20068002370 | 3.X MIM CAPACITOR IN A SEMICONDUCTOR DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN 20068003372 | 4.X FLOATING POINT NORMALIZATION AND DENORMALIZATION |
| FREESCALE SEMICONDUCTOR, INC. | CN 20068004697 | 9.X SOI ACTIVE-LAYER WITH DIFFERENT SURFACE ORIENTATION |
| FREESCALE SEMICONDUCTOR, INC. | CN 20078001175 | 5.X LEAD FRAME BASED, OVER-MOLDED SEMICONDUCTOR PACKAGE WITH INTEGRATED THROUGH HOLE TECHNOLOGY (THT) HEAT SPREADER PIN(S) AND ASSOCIATED METHOD OF MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | CN 20078001527 | 7.X METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING A FIN AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN 20078003951 | 7.X METHOD OF PACKAGING A DEVICE HAVING A MULTI- CONTACT ELASTOMER CONNECTOR CONTACT AREA AND DEVICE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN 20088002453 | 6.X DYNAMIC VOLTAGE ADJUSTMENT FOR MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | DE 60235172.3-0 | CONVERTER, CIRCUIT AND METHOD FOR COMPENSATION OF NON-IDEALITIES IN CONTINOUS TIME SIGMA DELTA CONVERTERS. |
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| FREESCALE SEMICONDUCTOR, INC. | FR | EP0617464 | SEMICONDUCTOR DEVICE HAVING X- SHAPED DIE SUPPORT MEMBER AND METHOD FOR MAKING THE SAME |
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| FREESCALE SEMICONDUCTOR, INC. | GB | EP0617464 | SEMICONDUCTOR DEVICE HAVING X- SHAPED DIE SUPPORT MEMBER AND METHOD FOR MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP0617464 | SEMICONDUCTOR DEVICE HAVING X- SHAPED DIE SUPPORT MEMBER AND METHOD FOR MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0629002 | SEMICONDUCTOR DEVICE AND FERRO ELECTRIC CAPACITOR |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0629002 | SEMICONDUCTOR DEVICE AND FERRO ELECTRIC CAPACITOR |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP0629002 | SEMICONDUCTOR DEVICE AND FERRO ELECTRIC CAPACITOR |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0629031 | REVERSE BATTERY PROTECTION CIR CUIT |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0629031 | REVERSE BATTERY PROTECTION CIR CUIT |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0643903 | PROCESS FOR FORMING TIN- BISMUTH SOLDER CONNECTION HAVING IMPROVED HIGH TEMPERATURE PROPERTIES |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0643903 | PROCESS FOR FORMING TIN- BISMUTH SOLDER CONNECTION HAVING IMPROVED HIGH TEMPERATURE PROPERTIES |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP0643903 | PROCESS FOR FORMING TIN- BISMUTH SOLDER CONNECTION HAVING IMPROVED HIGH TEMPERATURE PROPERTIES |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0646956 | TRENCH ISOLATION STRUCTURE IN AN INTEGRATED CIRCUIT AND METH OD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0646956 | TRENCH ISOLATION STRUCTURE IN AN INTEGRATED CIRCUIT AND METH OD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP0646956 | TRENCH ISOLATION STRUCTURE IN AN INTEGRATED CIRCUIT AND METH OD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0653795 | DOUBLE IMPLANTED LATERALLY DIF FUSED MOS DEVICE AND METHOD TH EREOF |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0653795 | DOUBLE IMPLANTED LATERALLY DIF FUSED MOS DEVICE AND METHOD TH EREOF |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0676811 | EEPROM CELL WITH ISOLATION TRA NSISTOR AND METHODS FOR MAKING AND OPERATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0676811 | EEPROM CELL WITH ISOLATION TRA NSISTOR AND METHODS FOR MAKING AND OPERATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP0676811 | EEPROM CELL WITH ISOLATION TRA NSISTOR AND METHODS FOR MAKING AND OPERATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0682812 | THERMALLY CONDUCTIVE INTEGRATED CIRCUIT PACKAGE WITH RADIO FREQUENCY SHIELDING |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0682812 | THERMALLY CONDUCTIVE INTEGRATED CIRCUIT PACKAGE WITH RADIO FREQUENCY SHIELDING |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0688044 | III-V SEMICONDUCTOR STRUCTURE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0688044 | III-V SEMICONDUCTOR STRUCTURE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0690497 | SEMICONDUCTOR DEVICE AND METHO D OF FORMING |
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| FREESCALE SEMICONDUCTOR, INC. | GB | EP0690497 | SEMICONDUCTOR DEVICE AND METHO D OF FORMING |
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| FREESCALE SEMICONDUCTOR, INC. | FR | EP0729019 | PIEZORESISTIVE SENSOR AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0729019 | PIEZORESISTIVE SENSOR AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0736897 | METHOD FOR FORMING A TRENCH IS OLATION STRUCTURE IN AN INTEGR ATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0736897 | METHOD FOR FORMING A TRENCH IS OLATION STRUCTURE IN AN INTEGR ATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP0736897 | METHOD FOR FORMING A TRENCH IS OLATION STRUCTURE IN AN INTEGR ATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0741413 | MONOLITHIC HIGH FREQUENCY INTE GRATED CIRCUIT STRUCTURE AND M ETHOD OF MANUFACTURING THE SAM E |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0741413 | MONOLITHIC HIGH FREQUENCY INTE GRATED CIRCUIT STRUCTURE AND M ETHOD OF MANUFACTURING THE SAM E |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0749205 | SWITCHED CAPACITOR GAIN STAGE |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0749205 | SWITCHED CAPACITOR GAIN STAGE |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0751389 | SEMICONDUCTOR SENSOR DEVICE AN D METHOD FOR FORMING A SEMICON DUCTOR SENSOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0757316 | DATA PROCESSING SYSTEM FOR ACC ESSING AN EXTERNAL DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0757316 | DATA PROCESSING SYSTEM FOR ACC ESSING AN EXTERNAL DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP0757316 | DATA PROCESSING SYSTEM FOR ACC ESSING AN EXTERNAL DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0779654 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0779654 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP0779654 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0783153 | PERIPHERAL MODULE AND MICROPRO CESSOR SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0791966 | NON-VOLATILE MEMORY CELL AND M ETHOD OF PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0791966 | NON-VOLATILE MEMORY CELL AND M ETHOD OF PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | NL | EP0791966 | NON-VOLATILE MEMORY CELL AND M ETHOD OF PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0793096 | METHOD OF SENSING A CHEMICAL A ND SENSOR THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | FI | EP0794427 | SEMICONDUCTOR CHEMICAL SENSOR DEVICE AND ETHOD OF FORMING A THERMOCOUPLE FOR A SEMICONDUCT OR CHEMICAL SENSOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0794427 | SEMICONDUCTOR CHEMICAL SENSOR DEVICE AND ETHOD OF FORMING A THERMOCOUPLE FOR A SEMICONDUCT OR CHEMICAL SENSOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0794610 | CONSTANT HIGH Q VOLTAGE CONTRO LLED OSCILLATOR AND METHOD FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0794610 | CONSTANT HIGH Q VOLTAGE CONTRO LLED OSCILLATOR |

AND METHOD FOR MAKING

| FREESCALE SEMICONDUCTOR, INC. | GB | EP0795747 | NEW GEOMETRY FOR ALOW RESISTAN T HEATER |
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| FREESCALE SEMICONDUCTOR, INC. | FR | EP0798554 | SENSOR AND METHOD OF FABRICATI ON |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0798554 | SENSOR AND METHOD OF FABRICATI ON |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0805074 | AUTOMOBILE AIRBAG SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0805074 | AUTOMOBILE AIRBAG SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0806729 | METHOD AND APPARATUS FOR DETER MINING WAIT STATES ON A PER CY CLE BASIS IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0806729 | METHOD AND APPARATUS FOR DETER MINING WAIT STATES ON A PER CY CLE BASIS IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0816186 | CURRENT LIMIT CONTROLLER FOR A N AIR BAG DEPLOYMENT SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0816186 | CURRENT LIMIT CONTROLLER FOR A N AIR BAG DEPLOYMENT SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0828253 | MEMORY SUITABLE FOR OPERATION AT LOW POWER SUPPLY VOLTAGES A ND SENSE AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0828253 | MEMORY SUITABLE FOR OPERATION AT LOW POWER SUPPLY VOLTAGES A ND SENSE AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP0828253 | MEMORY SUITABLE FOR OPERATION AT LOW POWER SUPPLY VOLTAGES A ND SENSE AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | NL | EP0828253 | MEMORY SUITABLE FOR OPERATION AT LOW POWER SUPPLY VOLTAGES A ND SENSE AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0865084 | SENSOR DEVICE HAVING ESD PROTE CTION AND METHOD OF FABRICATIN G SUCH A SENSOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0869544 | METHOD FOR DEPOSITING A DIFFUSION BARRIER |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0869544 | METHOD FOR DEPOSITING A DIFFUSION BARRIER |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0871214 | PROCESS FOR POLISHING DISSIMIL AR CONDUCTIVE LAYERS IN A SEMI CONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0871214 | PROCESS FOR POLISHING DISSIMIL AR CONDUCTIVE LAYERS IN A SEMI CONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0935836 | PORTABLE ELECTRONIC DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0939495 | PORTABLE ELECTRONIC DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0939495 | PORTABLE ELECTRONIC DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP0947245 | METHOF OF ORMING METAL COLLOID S, METAL COLLOIDS AND METHOD O F FORMING A METAL OXIDE SENSIT IVE LAYER FOR A CHEMICAL SENSOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0947245 | METHOF OF ORMING METAL COLLOID S, METAL COLLOIDS AND METHOD O F FORMING A METAL OXIDE SENSIT IVE LAYER FOR A CHEMICAL SENSOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP0981742 | METHOD AND SENSOR SYSTEM FOR D ETERMING A CONCENTRATION OF A CHEMICAL SPECIES |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1033745 | METHOD FOR FORMING A BARRIER L AYER FOR USE IN A COPPER INTER CONNECT |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1033745 | METHOD FOR FORMING A BARRIER L AYER FOR USE IN A |

COPPER INTER CONNECT

| FREESCALE SEMICONDUCTOR, INC. | FR | EP1039370 | MODULO ADDRESS GENERATOR AND A METHOD FOR IMPLEMENTING MODULO ADDRESSING |
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| FREESCALE SEMICONDUCTOR, INC. | GB | EP1039370 | MODULO ADDRESS GENERATOR AND A METHOD FOR IMPLEMENTING MODULO ADDRESSING |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1050902 | METHOD OF FORMING A COPPER LAY ER OVER A SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1050902 | METHOD OF FORMING A COPPER LAY ER OVER A SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | IE | EP1050902 | METHOD OF FORMING A COPPER LAY ER OVER A SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP1050902 | METHOD OF FORMING A COPPER LAY ER OVER A SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | NL | EP1050902 | METHOD OF FORMING A COPPER LAY ER OVER A SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1052765 | METHOD AND APPARATUS FOR ELECT RONICALLY COMMUTATING AN ELECT RIC MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1052765 | METHOD AND APPARATUS FOR ELECT RONICALLY COMMUTATING AN ELECT RIC MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1067674 | APPARATUS FOR RECEIVING AND PROCESSING A RADIO FREQUENCY SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1067674 | APPARATUS FOR RECEIVING AND PROCESSING A RADIO FREQUENCY SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | NL | EP1067674 | APPARATUS FOR RECEIVING AND PROCESSING A RADIO FREQUENCY SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1122333 | UV CURE PROCESS AND TOOL FOR LOW K FILM FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1122333 | UV CURE PROCESS AND TOOL FOR LOW K FILM FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP1122333 | UV CURE PROCESS AND TOOL FOR LOW K FILM FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1130518 | SOFTWARE ANALYSIS SYSTEM HAVING AN APPARATUS FOR SELECTIVELY COLLECTING ANALYSIS DATA FROM A TARGET SYSTEM EXECUTING SOFTWARE INSTRUMENTED WITH TAG STATEMENTS AND METHOD FOR USE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1130518 | SOFTWARE ANALYSIS SYSTEM HAVING AN APPARATUS FOR SELECTIVELY COLLECTING ANALYSIS DATA FROM A TARGET SYSTEM EXECUTING SOFTWARE INSTRUMENTED WITH TAG STATEMENTS AND METHOD FOR USE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1160968 | METHOD AND APPARATUS FOR TRANSMITTING A SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1160968 | METHOD AND APPARATUS FOR TRANSMITTING A SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1235398 | CHANNEL ESTIMATION IN ORTHOFONAL FREQUENCY DIVISION MULTIPLEXED SYSTEMS. |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1235398 | CHANNEL ESTIMATION IN ORTHOFONAL FREQUENCY DIVISION MULTIPLEXED SYSTEMS. |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1273036 | METHOD OF MANUFACTURING A HETEROJUNCTION BICMOS INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP1273036 | METHOD OF MANUFACTURING A HETEROJUNCTION BICMOS INTEGRATED CIRCUIT |

| FREESCALE SEMICONDUCTOR, INC. | DE | EP1277236 | ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUIT |
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| FREESCALE SEMICONDUCTOR, INC. | GB | EP1277236 | ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1344035 | INTEGRATED CMOS CAPACITIVE PRESSURE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1344035 | INTEGRATED CMOS CAPACITIVE PRESSURE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1351286 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1351286 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1354227 | ELECTRO-OPTIC STRUCTURE AND PROCESS FOR FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1354227 | ELECTRO-OPTIC STRUCTURE AND PROCESS FOR FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1365515 | ANALOG-TO-DIGITAL CONVERTER ARRANGEMENT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1365515 | ANALOG-TO-DIGITAL CONVERTER ARRANGEMENT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1367615 | MICRO-ELECTRO-MECHANICAL DEVICE AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1367615 | MICRO-ELECTRO-MECHANICAL DEVICE AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1376962 | COMMUNICATION APPARATUS INCLUDING DRIVER MEANS FOR APPLYING A SWITCHED SIGNAL TO A COMMUNICATION LINE WITH A CONTROLLED SLEW RATE |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1376962 | COMMUNICATION APPARATUS INCLUDING DRIVER MEANS FOR APPLYING A SWITCHED SIGNAL TO A COMMUNICATION LINE WITH A CONTROLLED SLEW RATE |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1388167 | METHOD OF PREPARING COPPER METALLIZATION DIE FOR WIRE BONDING |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1402340 | FIRST-IN FIRST-OUT MEMORY SYSTEM AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1402340 | FIRST-IN FIRST-OUT MEMORY SYSTEM AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1415388 | ODD HARMONICS REDUCTION OF PHASE ANGLE CONTROLLED LOADS |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1418674 | CONVERTER, CIRCUIT AND METHOD FOR COMPENSATION OF NON-IDEALITIES IN CONTINOUS TIME SIGMA DELTA CONVERTERS |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1418674 | CONVERTER, CIRCUIT AND METHOD FOR COMPENSATION OF NON-IDEALITIES IN CONTINOUS TIME SIGMA DELTA CONVERTERS |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1468486 | METHOD AND APPARATUS FOR DETECTING A STALL CONDITION IN A STEPPING MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1468486 | METHOD AND APPARATUS FOR DETECTING A STALL CONDITION IN A STEPPING MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1473837 | METHOD AND APPARATUS FOR REDUCED POWE CONSUMPTION ADC/DAC CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1473837 | METHOD AND APPARATUS FOR REDUCED POWE CONSUMPTION ADC/DAC CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1480342 | ANALOG TO DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1480342 | ANALOG TO DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1487114 | KEYPAD SIGNAL INPUT APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1487114 | KEYPAD SIGNAL INPUT APPARATUS |
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| FREESCALE SEMICONDUCTOR, INC. | FR | EP1492235 | PHASE LOCKED LOOP FILTER |
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| FREESCALE SEMICONDUCTOR, INC. | GB | EP1492235 | PHASE LOCKED LOOP FILTER |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP1492235 | PHASE LOCKED LOOP FILTER |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1497858 | HIGH FREQUENCY SIGNAL ISOLATION IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1497858 | HIGH FREQUENCY SIGNAL ISOLATION IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1499906 | METHOD AND APPARATUS FOR SECURE SCAN TESTING |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1499906 | METHOD AND APPARATUS FOR SECURE SCAN TESTING |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1520182 | METHOD AND APPARATUS FOR AFFECTING A PORTION OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1520182 | METHOD AND APPARATUS FOR AFFECTING A PORTION OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1528670 | TRANSCONDUCTANCE AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1528670 | TRANSCONDUCTANCE AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1528671 | POWER AMPLIFIER SATURATION DETECTION AND OPERATION AT MAXIMUM POWER |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1528671 | POWER AMPLIFIER SATURATION DETECTION AND OPERATION AT MAXIMUM POWER |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP1528671 | POWER AMPLIFIER SATURATION DETECTION AND OPERATION AT MAXIMUM POWER |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1542357 | A POWER AMPLIFIER MODULE AND A TIME DIVISION MULTIPLE ACCESS RADIO |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1542357 | A POWER AMPLIFIER MODULE AND A TIME DIVISION MULTIPLE ACCESS RADIO |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1551099 | LOW IF RADIO RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1551099 | LOW IF RADIO RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP1551099 | LOW IF RADIO RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1569126 | UNIVERSAL SERIAL BUS TRANSMITTER |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1569126 | UNIVERSAL SERIAL BUS TRANSMITTER |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP1569126 | UNIVERSAL SERIAL BUS TRANSMITTER |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1576610 | SENSE AMPLIFIER FOR A MEMORY HAVING AT LEAST TWO DISTINCT RESISTANCE STATES |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1576610 | SENSE AMPLIFIER FOR A MEMORY HAVING AT LEAST TWO DISTINCT RESISTANCE STATES |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1580637 | LOW DROP-OUT DC VOLTAGE REGULATOR |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1580637 | LOW DROP-OUT DC VOLTAGE REGULATOR |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1594253 | SERIAL DATA BUS COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1594253 | SERIAL DATA BUS COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1602532 | A DRIVE ARRANGEMENT FOR ACTIVATING A CAR SAFETY DEVICE ACTIVATION ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1602532 | A DRIVE ARRANGEMENT FOR ACTIVATING A CAR SAFETY DEVICE ACTIVATION ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1605360 | A MEMORY CACHE CONTROL ARRANGMENT AND A METHOD OF PERFORMING A COHERENCY OPERATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1605360 | A MEMORY CACHE CONTROL ARRANGMENT AND A METHOD OF PERFORMING A COHERENCY OPERATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1607869 | DATA CACHE SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1607869 | DATA CACHE SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1623431 | NON-VOLATILE MEMORY HAVING A BIAS ON THE SOURCE |

ELECTRODE FOR HCI PROGRAMMING

| FREESCALE SEMICONDUCTOR, INC. | GB | EP1623431 | NON-VOLATILE MEMORY HAVING A BIAS ON THE SOURCE ELECTRODE FOR HCI PROGRAMMING |
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| FREESCALE SEMICONDUCTOR, INC. | IT | EP1623431 | NON-VOLATILE MEMORY HAVING A BIAS ON THE SOURCE ELECTRODE FOR HCI PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1692770 | A DECODER FOR A WIRELESS COMMUNICATION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1692770 | A DECODER FOR A WIRELESS COMMUNICATION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1702420 | SIGNAL GENERATION POWER MANAGEMENT CONTROL SYSTEM FOR PORTABLE COMMUNICATIONS DEVICE AND METHOD OF USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1702420 | SIGNAL GENERATION POWER MANAGEMENT CONTROL SYSTEM FOR PORTABLE COMMUNICATIONS DEVICE AND METHOD OF USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1723532 | MULTIPLE BURST PROTOCOL DEVICE CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1723532 | MULTIPLE BURST PROTOCOL DEVICE CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP1723532 | MULTIPLE BURST PROTOCOL DEVICE CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1723673 | METHOD OF MAKING A SEMICONDUCTOR DEVICE, AND SEMICONDUCTOR DEVICE MADE THEREBY |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1723673 | METHOD OF MAKING A SEMICONDUCTOR DEVICE, AND SEMICONDUCTOR DEVICE MADE THEREBY |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1749312 | DECOUPLED COMPLEMENTARY MASK PATTERNING TRANSFER METHOD |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1749312 | DECOUPLED COMPLEMENTARY MASK PATTERNING TRANSFER METHOD |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1751762 | AUTOMATIC HIDDEN REFRESH IN A DRAM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1751762 | AUTOMATIC HIDDEN REFRESH IN A DRAM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1756860 | METHOD OF SEMICONDUCTOR FABRICATION INCORPORATING DISPOSABLE SPACER INTO ELEVATED SOURCE/DRAIN PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1756860 | METHOD OF SEMICONDUCTOR FABRICATION INCORPORATING DISPOSABLE SPACER INTO ELEVATED SOURCE/DRAIN PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP1756860 | METHOD OF SEMICONDUCTOR FABRICATION INCORPORATING DISPOSABLE SPACER INTO ELEVATED SOURCE/DRAIN PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1770708 | PROGRAMMABLE DELAY CONTROL IN A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1770708 | PROGRAMMABLE DELAY CONTROL IN A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP1770708 | PROGRAMMABLE DELAY CONTROL IN A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1776715 | METHOD FOR FORMING A GATE ELECTRODE HAVING A METAL |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1776715 | METHOD FOR FORMING A GATE ELECTRODE HAVING A METAL |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP1776715 | METHOD FOR FORMING A GATE ELECTRODE HAVING A METAL |
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| FREESCALE SEMICONDUCTOR, INC. | FR | EP1789876 | METHOD AND APPARATUS FOR MODIFYING AN INFORMATION UNIT USING AN ATOMIC OPERATION |
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| FREESCALE SEMICONDUCTOR, INC. | GB | EP1789876 | METHOD AND APPARATUS FOR MODIFYING AN INFORMATION UNIT USING AN ATOMIC OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1789883 | A VIRTUAL ADDRESS CACHE AND METHOD FOR SHARING DATA USING A UNIQUE TASK IDENTIFIER |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1789883 | A VIRTUAL ADDRESS CACHE AND METHOD FOR SHARING DATA USING A UNIQUE TASK IDENTIFIER |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1817595 | INTEGRATED CIRCUIT AND A METHOD FOR SECURE TESTING |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1817595 | INTEGRATED CIRCUIT AND A METHOD FOR SECURE TESTING |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1817596 | INTEGRATED CIRCUIT AND A METHOD FOR TESTING A MULTITAP INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1817596 | INTEGRATED CIRCUIT AND A METHOD FOR TESTING A MULTITAP INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1820031 | SYSTEM AND METHOD FOR FALL DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1820031 | SYSTEM AND METHOD FOR FALL DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | NL | EP1820031 | SYSTEM AND METHOD FOR FALL DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1820130 | METHOD AND SYSTEM FOR IMPROVING THE DESIGN OF SEMICONDUCTOR INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1820130 | METHOD AND SYSTEM FOR IMPROVING THE DESIGN OF SEMICONDUCTOR INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1829260 | APPARATUS AND METHOD FOR DETECTING AN END POINT OF AN INFORMATION FRAME |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1829260 | APPARATUS AND METHOD FOR DETECTING AN END POINT OF AN INFORMATION FRAME |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1846321 | METHOD OF FABRICATING A SILICON-ON-INSULATOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1846321 | METHOD OF FABRICATING A SILICON-ON-INSULATOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP1846321 | METHOD OF FABRICATING A SILICON-ON-INSULATOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1849084 | NON-HIGH IMPEDENCE DEVICE AND METHOD FOR REDUCING ENERGY CONSUMPTION |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1849084 | NON-HIGH IMPEDENCE DEVICE AND METHOD FOR REDUCING ENERGY CONSUMPTION |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1864379 | METHOD FOR RACE PREVENTION AND A DEVICE HAVING RACE PREVENTION CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1864379 | METHOD FOR RACE PREVENTION AND A DEVICE HAVING RACE PREVENTION CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1867049 | METHOD FOR NOISE REDUCTION IN A PHASE LOCKED LOOP AND A DEVICE HAVING NOISE REDUCTION CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1867049 | METHOD FOR NOISE REDUCTION IN A PHASE LOCKED LOOP AND A DEVICE HAVING NOISE REDUCTION CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1867071 | METHOD AND DEVICE FOR TRANSMITTING A SEQUENCE OF |

TRANSMISSION BURSTS

| FREESCALE SEMICONDUCTOR, INC. | GB | EP1867071 | METHOD AND DEVICE FOR TRANSMITTING A SEQUENCE OF TRANSMISSION BURSTS |
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| FREESCALE SEMICONDUCTOR, INC. | FR | EP1875782 | CURRENT DRIVER AND METHOD OF OPERATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1875782 | CURRENT DRIVER AND METHOD OF OPERATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1875783 | CURRENT DRIVER AND METHOD OF OPERATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1875783 | CURRENT DRIVER AND METHOD OF OPERATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1894374 | TWISTED PAIR COMMUNICATION SYSTEM, APPARATUS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1894374 | TWISTED PAIR COMMUNICATION SYSTEM, APPARATUS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1899825 | DEVICE AND METHOD FOR CONTROLLING MULTIPLE DMA TASK |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1899825 | DEVICE AND METHOD FOR CONTROLLING MULTIPLE DMA TASK |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1899826 | DEVICE AND METHOD FOR CONTROLLING AN EXECUTION OF A DMA TASK |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1899826 | DEVICE AND METHOD FOR CONTROLLING AN EXECUTION OF A DMA TASK |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1899827 | DEVICE AND METHOD FOR EXECUTING A DMA TASK |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1899827 | DEVICE AND METHOD FOR EXECUTING A DMA TASK |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1899828 | DEVICE AND METHOD FOR ARBITRATING BETWEEN DIRECT MEMORY ACCESS TASK REQUEST |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1899828 | DEVICE AND METHOD FOR ARBITRATING BETWEEN DIRECT MEMORY ACCESS TASK REQUEST |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1908167 | COMPENSATION FOR PARASITIC COUPLING BETWEEN RF OR MICROWAVE TRANSISTORS IN THE SAME PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1908167 | COMPENSATION FOR PARASITIC COUPLING BETWEEN RF OR MICROWAVE TRANSISTORS IN THE SAME PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | DE | EP1910905 | VOLTAGE REGULATOR AND METHOD OF OPERATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1910905 | VOLTAGE REGULATOR AND METHOD OF OPERATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1910905 | VOLTAGE REGULATOR AND METHOD OF OPERATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1929391 | SELF ADJUSTING REGULATOR AND MONITOR CIRCUITS ON AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1929391 | SELF ADJUSTING REGULATOR AND MONITOR CIRCUITS ON AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1929403 | A DEVICE HAVIING A LOW LATENCY SINGLE PORT MEMORY UNIT AND A METHOD FOR WRITING MULTIPLE DATA SEGMENTS TO A SINGLE PORT MEMORY UNIT |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1929403 | A DEVICE HAVIING A LOW LATENCY SINGLE PORT MEMORY UNIT AND A METHOD FOR WRITING MULTIPLE DATA SEGMENTS TO A SINGLE PORT MEMORY UNIT |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1935008 | MICROELECTRONIC ASSEMBLY AND METHOD FOR FORMING |

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| FREESCALE SEMICONDUCTOR, INC. | GB | EP1935008 | MICROELECTRONIC ASSEMBLY AND METHOD FOR FORMING THE SAME |
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| FREESCALE SEMICONDUCTOR, INC. | FR | EP1935022 | MICROELECTRONIC ASSEMBLY AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1935022 | MICROELECTRONIC ASSEMBLY AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1943320 | METHOD FOR TESTING A SLURRY USED TO FORM A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1943320 | METHOD FOR TESTING A SLURRY USED TO FORM A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP1943320 | METHOD FOR TESTING A SLURRY USED TO FORM A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1946449 | POWER SAVING IN A SIGNAL PROCESSING IN RECEIVERS |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1946449 | POWER SAVING IN A SIGNAL PROCESSING IN RECEIVERS |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1952568 | A METHOD FOR MANAGING MULTI-FRAMES AND A DEVICE HAVING MULTI-FRAME MANAGEMENT CAPABILITES |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1952568 | A METHOD FOR MANAGING MULTI-FRAMES AND A DEVICE HAVING MULTI-FRAME MANAGEMENT CAPABILITES |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1955493 | A METHOD FOR PROCESSING ATM CELLS AND A DEVICE HAVING ATM CELL PROCESSING CAPABILITES |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1955493 | A METHOD FOR PROCESSING ATM CELLS AND A DEVICE HAVING ATM CELL PROCESSING CAPABILITES |
| FREESCALE SEMICONDUCTOR, INC. | DE | EP1966652 | IMMERSION LITHOGRAPHY APPARATUS AND METHOD OF PERFORMING IMMERSION LITHOGRAPHY |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1966652 | IMMERSION LITHOGRAPHY APPARATUS AND METHOD OF PERFORMING IMMERSION LITHOGRAPHY |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1966652 | IMMERSION LITHOGRAPHY APPARATUS AND METHOD OF PERFORMING IMMERSION LITHOGRAPHY |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP1966652 | IMMERSION LITHOGRAPHY APPARATUS AND METHOD OF PERFORMING IMMERSION LITHOGRAPHY |
| FREESCALE SEMICONDUCTOR, INC. | DE | EP1984467 | BARRIER SLURRY COMPOSITION AND BARRIER CMP METHODS |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1984467 | BARRIER SLURRY COMPOSITION AND BARRIER CMP METHODS |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1984467 | BARRIER SLURRY COMPOSITION AND BARRIER CMP METHODS |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP1984467 | BARRIER SLURRY COMPOSITION AND BARRIER CMP METHODS |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1985079 | LIN NETWORK, INTEGRATED CIRCUIT AND METHOD OF COMMUNICATING THEREON |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1985079 | LIN NETWORK, INTEGRATED CIRCUIT AND METHOD OF COMMUNICATING THEREON |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1989618 | SOFTWARE PIPELINING |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1989618 | SOFTWARE PIPELINING |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP1989729 | SEMICONDUCTOR PROCESS INTEGRATING SOURCE/DRAIN |

STRESSORS AND INTERLEVEL DIELECTRIC LAYER STRESSORS

| FREESCALE SEMICONDUCTOR, INC. | GB | EP1989729 | SEMICONDUCTOR PROCESS INTEGRATING SOURCE/DRAIN STRESSORS AND INTERLEVEL DIELECTRIC LAYER STRESSORS |
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| FREESCALE SEMICONDUCTOR, INC. | FR | EP1999574 | DATA PROCESSOR HAVING DYNAMIC CONTROL OF INSTRUCTION PREFETCH BUFFER DEPTH AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP1999574 | DATA PROCESSOR HAVING DYNAMIC CONTROL OF INSTRUCTION PREFETCH BUFFER DEPTH AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2002271 | APPARATUS FOR DETECTING CLOCK FAILURE AND METHED THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2002271 | APPARATUS FOR DETECTING CLOCK FAILURE AND METHED THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2002272 | APPARATUS FOR DETECTING CLOCK FAILURE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2002272 | APPARATUS FOR DETECTING CLOCK FAILURE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP2002272 | APPARATUS FOR DETECTING CLOCK FAILURE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2002445 | A NON-VOLATILE MEMORY DEVICE AND PROGRAMMABLE VOLTAGE REFERENCE FOR A NON-VOLATILE MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2002445 | A NON-VOLATILE MEMORY DEVICE AND PROGRAMMABLE VOLTAGE REFERENCE FOR A NON-VOLATILE MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2008379 | ADJUSTABLE NOISE SUPPRESSION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2008379 | ADJUSTABLE NOISE SUPPRESSION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2018615 | DATA COMMUNICATION UNIT, INTEGRATED CIRCUIT AND METHOD FOR BUFFERING DATA |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2018615 | DATA COMMUNICATION UNIT, INTEGRATED CIRCUIT AND METHOD FOR BUFFERING DATA |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2022167 | AMPLIFIER CIRCUIT AND INTEGRATED CIRCUIT THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2022167 | AMPLIFIER CIRCUIT AND INTEGRATED CIRCUIT THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2030030 | DEVICE AND METHOD FOR TESTING INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2030030 | DEVICE AND METHOD FOR TESTING INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2030096 | DATA COMMUNICATION FLOW CONTROL DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2030096 | DATA COMMUNICATION FLOW CONTROL DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2030388 | LIN NETWORK, INTEGRATED CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2030388 | LIN NETWORK, INTEGRATED CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2041880 | RECEIVER FOR RECEIVING AT LEAST TWO TYPES OF SIGNALS, DATA COMMUNICATION SYSTEM AND VEHICLE INCLUDING A RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2041880 | RECEIVER FOR RECEIVING AT LEAST TWO TYPES OF SIGNALS, DATA COMMUNICATION SYSTEM AND VEHICLE INCLUDING A RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2050097 | MEMORY CIRCUIT USING A REFERENCE FOR SENSING |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2050097 | MEMORY CIRCUIT USING A REFERENCE FOR SENSING |
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| FREESCALE SEMICONDUCTOR, INC. | FR | EP2052270 | REAL TIME CLOCK MONITORING METHOD AND SYSTEM |
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| FREESCALE SEMICONDUCTOR, INC. | GB | EP2052270 | REAL TIME CLOCK MONITORING METHOD AND SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2067164 | SEMI-FLOATING ISLAND MOSFET DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2067164 | SEMI-FLOATING ISLAND MOSFET DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2106553 | DIFFERENTIAL CAPACITIVE SENSOR AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2106553 | DIFFERENTIAL CAPACITIVE SENSOR AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2111584 | REQUEST CONTROLLER, PROCESSING UNIT, METHOD FOR CONTROLLING REQUESTS AND COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2111584 | REQUEST CONTROLLER, PROCESSING UNIT, METHOD FOR CONTROLLING REQUESTS AND COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2113087 | SYSTEM, COMPUTER PROGRAM PRODUCT AND METHOD FOR TESTING A LOGIC CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2113087 | SYSTEM, COMPUTER PROGRAM PRODUCT AND METHOD FOR TESTING A LOGIC CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2132874 | METHOD AND DEVICE FOR PROGRAMMING ANTI-FUSES |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2132874 | METHOD AND DEVICE FOR PROGRAMMING ANTI-FUSES |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2135052 | IMPROVEMENTS IN OR RELATING TO DIAGNOSTICS OF A CAPACITIVE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2135052 | IMPROVEMENTS IN OR RELATING TO DIAGNOSTICS OF A CAPACITIVE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2137606 | METHOD AND APPARATUS FOR CONVERTING SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2137606 | METHOD AND APPARATUS FOR CONVERTING SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2145442 | METHOD, DATA STRUCTURE AND COMPUTER SYSTEM FOR PACKING A WORLDWIDE INTEROPERABILITY FOR MICROWAVE ACCESS (WIMAX) FRAME |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2145442 | METHOD, DATA STRUCTURE AND COMPUTER SYSTEM FOR PACKING A WORLDWIDE INTEROPERABILITY FOR MICROWAVE ACCESS (WIMAX) FRAME |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2153328 | DATA PROCESSING SYSTEM, DATA PROCESSING METHOD, AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2153328 | DATA PROCESSING SYSTEM, DATA PROCESSING METHOD, AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2188967 | DATA PACKET FREQUENCY |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2188967 | DATA PACKET FREQUENCY |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2195843 | PROGRAMMABLE ROM USING TWO BONDED STRATA AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2195843 | PROGRAMMABLE ROM USING TWO BONDED STRATA AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2198350 | MICROPROCESSOR, SYSTEM FOR CONTROLLING A DEVICE AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2198350 | MICROPROCESSOR, SYSTEM FOR CONTROLLING A DEVICE AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2203964 | POWER MANAGEMENT ARRANGEMENT AND MOBILE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2203964 | POWER MANAGEMENT ARRANGEMENT AND MOBILE DEVICE |
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| FREESCALE SEMICONDUCTOR, INC. | FR | EP2206151 | METHOD FOR INTEGRATING NVM CIRCUITRY WITH LOGIC CIRCUITRY |
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| FREESCALE SEMICONDUCTOR, INC. | GB | EP2206151 | METHOD FOR INTEGRATING NVM CIRCUITRY WITH LOGIC CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2211458 | CHARGE AMPLIFIER WITH DC FEEDBACK SAMPLING |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2229730 | SEMICONDUCTOR DEVICE AND APPARATUS INCLUDING SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2229730 | SEMICONDUCTOR DEVICE AND APPARATUS INCLUDING SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2250775 | BUFFER MODULE, RECEIVER, DEVICE AND BUFFERING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2250775 | BUFFER MODULE, RECEIVER, DEVICE AND BUFFERING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2257906 | A METHOD FOR PROTECTING A CRYPTOGRAPHIC MODULE AND A DEVICE HAVING CRYPTOGRAPHIC MODULE PROTECTION CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2257906 | A METHOD FOR PROTECTING A CRYPTOGRAPHIC MODULE AND A DEVICE HAVING CRYPTOGRAPHIC MODULE PROTECTION CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2294581 | A SYSTEM FOR DISTRIBUTING AVAILABLE MEMORY RESOURCE |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2294581 | A SYSTEM FOR DISTRIBUTING AVAILABLE MEMORY RESOURCE |
| FREESCALE SEMICONDUCTOR, INC. | IT | EP2294581 | A SYSTEM FOR DISTRIBUTING AVAILABLE MEMORY RESOURCE |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2294832 | MULTI-FREQUENCY TONE DETECTOR |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2294832 | MULTI-FREQUENCY TONE DETECTOR |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2359538 | A SYSTEM, NETWORK NODE, A METHOD AND A COMMUNICATION CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2359538 | A SYSTEM, NETWORK NODE, A METHOD AND A COMMUNICATION CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2391898 | CAPACITANCE-TO-VOLTAGE INTERFACE CIRCUIT, AND RELATED OPERATING METHODS |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2391898 | CAPACITANCE-TO-VOLTAGE INTERFACE CIRCUIT, AND RELATED OPERATING METHODS |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2415217 | RECEIVING NODE IN A PACKET COMMUNICATIONS SYSTEM AND METHOD FOR MANAGING A BUFFER IN A RECEIVING NODE IN A PACKET COMMUNICATIONS SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2415217 | RECEIVING NODE IN A PACKET COMMUNICATIONS SYSTEM AND METHOD FOR MANAGING A BUFFER IN A RECEIVING NODE IN A PACKET COMMUNICATIONS SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2416248 | DATA PROCESSING SYSTEM WITH PERIPHAL CONFIGURATION INFORMATION ERROR DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2416248 | DATA PROCESSING SYSTEM WITH PERIPHAL CONFIGURATION INFORMATION ERROR DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | FR | EP2456070 | DIFFERENTIAL EQUALIZERS WITH SOURCE DEGENERATION AND FEEDBACK CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | GB | EP2456070 | DIFFERENTIAL EQUALIZERS WITH SOURCE DEGENERATION AND FEEDBACK CIRCUITS |
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| FREESCALE SEMICONDUCTOR, INC. | FR | FR9602669 | SEMICONDUCTOR CHEMICAL SENSOR DEVICE AND ETHOD OF FORMING A THERMOCOUPLE FOR A SEMICONDUCT OR CHEMICAL SENSOR DEVICE |
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| FREESCALE SEMICONDUCTOR, INC. | FR | FR9603216 | NEW GEOMETRY FOR ALOW RESISTAN T HEATER |
| FREESCALE SEMICONDUCTOR, INC. | FR | FR9705762 | METHOD AND SENSOR SYSTEM FOR D ETERMING A CONCENTRATION OF A CHEMICAL SPECIES |
| FREESCALE SEMICONDUCTOR, INC. | FR | FR9708005 | SENSOR DEVICE AND METHOD FOR F ORMING A SENSOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | FR | FR9710942 | PORTABLE ELECTRONIC DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | FR | FR9806021 | PROCESS FOR DEPOSITING A LAYER OF MATERIAL ON A SUBSTRATE AN D A PLATING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | GB | GB2389433 | BIT EXACTNESS SUPPORT IN DUAL-MAC ARCHITECTURE |
| FREESCALE SEMICONDUCTOR, INC. | GB | GB2391337 | INSTRUCTION CACHE AND METHOD FOR REDUCING MEMORY CONFLICTS |
| FREESCALE SEMICONDUCTOR, INC. | GB | GB2403082 | ARRANGEMENT AND METHOD FOR DIGITAL DELAY LINE |
| FREESCALE SEMICONDUCTOR, INC. | GB | GB2403106 | ARRANGEMENT AND METHOD FOR ITERATIVE DECODING |
| FREESCALE SEMICONDUCTOR, INC. | GB | GB2406984 | METHOD AND ARRANGEMENT FOR I-Q BALANCING AND RADIO RECEIVER INCORPORATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | GB | GB2408356 | METHOD AND DEVICE FOR REGULATING A VOLTAGE SUPPLY TO A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | GB | GB2408398 | CALIBRATION DEVICE FOR A PHASED LOCKED LOOP SYNTHESISER |
| FREESCALE SEMICONDUCTOR, INC. | НК | HK1018123 | METHOD AND APPARATUS FOR PROCESSING A SEMICONDUCTOR WAFER ON A ROBOTIC TRACK HAVING ACCESS TO IN SITU WAFER BACKSIDE PARTICLE DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | НК | HK1019819 | SEMICONDUCTOR DEVICE HAVING A SUB-CHIP-SCALE PACKAGE STRUCTU RE AND METHOD FOR FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | НК | HK1021210 | A CHEMICAL MECHANICAL POLISHING (CMP) SLURRY FOR COPPER AND METHOD OF USE IN INTEGRATED CIRCUIT MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | HK | HK1024110 | PORTABLE ELECTRONIC DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | I221968 | SYSTEM AND METHOD FOR CONTROLLING BUS ARBITRATION DURING CACHE MEMORY BURST CYCLES |
| FREESCALE SEMICONDUCTOR, INC. | TW | I225270 | SEMICONDUCTOR DEVICE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | I225434 | ANTI-SCAVENGING SOLDERS FOR SILVER METALLIZATION AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | I225662 | METHOD OF FORMING STRUCTURES ON A SEMICONDUCTOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I226696 | METHOD OF FORMING AN INTEGRATED CIRCUIT DEVICE USING DUMMY FEATURES AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | I227498 | ELECTRONIC CONTROL APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I228207 | METHOD OF FORMING A RIM PHASE SHIFTING MASK AND USING THE RIM PHASE SHIFTING MASK TO FORM A SEMICONDUCTOR DEVICE |
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| FREESCALE SEMICONDUCTOR, INC. | TW | I228265 | LASER CLEANING PROCESS FOR SEM ICONDUCTOR MATERIAL AND THE LIKE |
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| FREESCALE SEMICONDUCTOR, INC. | TW | I229269 | METHOD AND DEVICE FOR CREATING AND USING PRE- INTERNALIZED PROGRAM FILES |
| FREESCALE SEMICONDUCTOR, INC. | TW | I229345 | FIRST-IN FIRST-OUT MEMORY SYSTEM AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | I231529 | METHOD OF FORMING NANOCRYSTALS IN A MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I233174 | TEMPERATURE-CONTROLLED CHUCK AND METHOD FOR CONTROLLING THE TEMPERATURE OF A SUBSTANTIALLY FLAT OBJECT |
| FREESCALE SEMICONDUCTOR, INC. | TW | I235491 | INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | TW | I235912 | PERFORMANCE MONITOR SYSTEM AND METHOD SUITABLE FOR USE IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | TW | I237878 | MULTI-ROW LEADFRAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | I240332 | HIGH DIELECTRIC FILM AND METHOD FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | TW | I240358 | SEMICONDUCTOR TILING STRUCTURE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | I240484 | CIRCUITRY FOR CREATING A SPECTRAL NULL IN A DIFFERENTIAL OUTPUT SWITCHING AMPLIFIER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I246731 | WIREBONDING INSULATED WIRE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I247568 | LOW PROFILE INTEGRATED MODULE INTERCONNECTS AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | I250745 | SELF-ROUTING, STAR-COUPLER-BASED COMMUNICATION NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | TW | I251345 | TRANSISTOR METAL GATE STRUCTURE THAT MINIMIZES NON-PLANARITY EFFECTS AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | I255020 | STACKED DIE SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I255525 | METHOD OF BONDING AND TRANSFERRING A MATERIAL TO FORM A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I256189 | SWITCHING AMPLIFIER HAVING DIGITAL CORRECTION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I256720 | SEMICONDUCTOR WAFER INDENTIFICATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | I257171 | MEMORY WITH CHARGE STORAGE LOCATIONS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I257658 | SEMICONDUCTOR POWER DEVICE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | I260076 | SEMICONDUCTOR PACKAGE DEVICE AND METHOD OF FORMATION AND TESTING |
| FREESCALE SEMICONDUCTOR, INC. | TW | I261906 | SEMICONDUCTOR DEVICE HAVING A WIRE BOND PAD AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I261917 | NON-VOLATILE MEMORY DEVICE WITH IMPROVED DATA RETENTION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I262560 | METHOD OF FORMING A VERTICAL DOUBLE GATE SEMICONDUCTOR DEVICE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | I263289 | PROCESS AND APPARATUS FOR DISENGAGING SEMICONDUCTOR DIE FROM AN ADHESIVE FILM |
| FREESCALE SEMICONDUCTOR, INC. | TW | I264076 | METHOD FOR PROCESSING MULTIPLE SEMICONDUCTOR |

DEVICES FOR TEST

| FREESCALE SEMICONDUCTOR, INC. | TW | I265584 | METHOD AND APPARATUS FOR TESTING AN INTEGRATED CIRCUIT |
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| FREESCALE SEMICONDUCTOR, INC. | TW | I266364 | BODY-TIED SILICON ON INSULATOR SEMICONDUCTOR DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I266402 | SEMICONDUCTOR DEVICE HAVING A BOND PAD AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I270170 | METHOD OF FORMING A SEMICONDUCTOR DEVICE IN A SEMICONDUCTOR LAYER AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | I270768 | METHOD AND APPARATUS FOR SECURE SCAN TESTING |
| FREESCALE SEMICONDUCTOR, INC. | TW | I271978 | SYSTEM FOR PROVIDING A CALIBRATED CLOCK AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | I274400 | METHOD OF FABRICATING A TIERED STRUCTURE USING A MULTI-LAYERED RESIST STACK AND USE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I274406 | DUAL GAUGE LEADFRAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | I274470 | APPARATUS AND METHOD FOR DIGITAL CONTROL SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I276306 | LOW POWER CYCLIC A/D CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | TW | I278918 | HIGH K DIELECTRIC FILM AND METHOD FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | TW | I279869 | NEW UNDER BUMP METALLURGY STRUCTURAL DESIGN FO HIGH RELIABILITY BUMPED PACKAGES |
| FREESCALE SEMICONDUCTOR, INC. | TW | I280643 | PACKAGED DEVICE AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | I281982 | TONE DETECTOR AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I282161 | ELECTRONIC DISCHARGE PROTECTION CIRCUITRY AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | I282992 | CONDUCTIVE PASTE AND SEMICONDU CTOR COMPONENT HAVING CONDUCTI VE BUMMPS MADE FROM THE CONDUCTIVE PASTE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I283029 | INTEGRATED CIRCUIT DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I284451 | METHOD AND APPARATUS FOR DETECTING A STALL CONDITION IN A STEPPING MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I286802 | SEMICONDUCTOR DEVICE WITH NANOCLUSTERS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I287709 | METHOD AND ARRANGEMENT FOR VIRTUAL DIRECT MEMORY ACCESS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I287864 | THREE DIMENSIONAL PACKAGE AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | I288970 | METHOD OF MAKING REINFORCED SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I289985 | COMMUNICATION NETWORK AND ARRANGEMENT FOR USE THEREIN |
| FREESCALE SEMICONDUCTOR, INC. | TW | I293493 | MULTIPLE THICKNESS SEMICONDUCTOR INTERCONNECT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I294223 | CONVERSION BETWEEN OPTICAL AND RADIO FREQUENCY SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I299870 | METHOD AND CIRCUITRY FOR IDENTIFYING WEAK BITS IN AN MRAM |
| FREESCALE SEMICONDUCTOR, INC. | TW | I299871 | SENSE AMPLIFIER FOR A MEMORY HAVING AT LEAST TWO DISTINCT RESISTANCE STATES |
| FREESCALE SEMICONDUCTOR, INC. | TW | I300982 | SEMICONDUCTOR APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I301234 | METHOD AND APPARATUS FOR AFFECTING A PORTION OF |

AN INTEGRATED CIRCUIT

| FREESCALE SEMICONDUCTOR, INC. | TW | I301272 | METHOD AND APPARATUS FOR SOFT DEFECT DETECTION IN A MEMORY |
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| FREESCALE SEMICONDUCTOR, INC. | TW | I301278 | THREE INPUT SENSE AMPLIFIER AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | I301292 | SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | TW | I303873 | METHOD OF MAKING STACKED DIE PACAKGE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I305676 | DIELECTRIC STORAGE MEMORY CELL HAVING HIGH PERMITTIVITY TOP DIELECTRIC AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I307155 | TRANSIENT DETECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | TW | I307533 | METHOD FOR ELIMINATING VOIDING IN PLATED SOLDER |
| FREESCALE SEMICONDUCTOR, INC. | TW | I309087 | SEMICONDUCTOR DEVICE STRUCTURES WHICH UTILIZE METAL SULFIDES |
| FREESCALE SEMICONDUCTOR, INC. | TW | 1309789 | METHOD AND APPARATUS FOR TRANSLATING DETECTED WAFER DEFECT COORDINATES TO RETICLE COORDINATES USING CAD DATA |
| FREESCALE SEMICONDUCTOR, INC. | TW | I311510 | SIMPLIFICATION OF BALL ATTACH METHOD USING SUPERSATURATED FINE CRYSTAL FLUX |
| FREESCALE SEMICONDUCTOR, INC. | TW | I311813 | FIELD EFFECT TRANSISTOR AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | I312180 | SOI POLYSILICON TRENCH REFILL PERIMETER OXIDE ANCHOR SCHEME |
| FREESCALE SEMICONDUCTOR, INC. | TW | I312517 | SELF-REPAIR OF MEMORY ARRAYS USING PREALLOCATED REDUNDANCY (PAR) ARCHITECTURE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I312909 | METHOD OF PATTERNING PHOTORESIST ON A WAFER USING A TRANSMISSION MASK WITH A CARBON LAYER |
| FREESCALE SEMICONDUCTOR, INC. | TW | I313123 | INTEGRATED CIRCUIT SECURITY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I313498 | WIRE BOND-LESS ELECTRONIC COMPONENT FOR USE WITH AN EXTERNAL CIRCUIT AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I313822 | METHOD AND APPARATUS FOR INTERFACING A PROCESSOR TO A COPROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I313921 | SEMICONDUCTOR DEVICE HAVING A BOND PAD AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I313929 | SEMICONDUCTOR DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I317205 | TAPERED CONSTANT "R" NETWORK FOR USE IN DISTRIBUTED AMPLIFIERS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I317541 | PACKAGED IC USING INSULATED WIRE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I319270 | COMMUNICATION SYSTEM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I319621 | ONE TRANSISTOR DRAM CELL STRUCTURE AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | TW | I320955 | METHOD OF MAKING EXPOSED PAD BALL GRID ARRAY PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I321257 | OPTICAL TO RADIO FREQUENCY DETECTOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I321321 | VARIABLE REFRESH CONTROL FOR A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | TW | I321322 | STORAGE CIRCUIT HAVING SINGLE-ENDED WRITE CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | TW | I321834 | MINIATURE MOLDLOCKS FOR HEATSINK OR FLAG FOR AN OVERMOLDED PLASTIC PACKAGE |
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| FREESCALE SEMICONDUCTOR, INC. | TW | I322498 | NON-VOLATILE MEMORY DEVICE AND METHOD FOR FORMING |
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| FREESCALE SEMICONDUCTOR, INC. | TW | I322501 | LOW VOLTAGE NMOS-BASED ELECTROSTATIC DISCHARGE CLAMP |
| FREESCALE SEMICONDUCTOR, INC. | TW | I322562 | OSCILLATOR CIRCUIT HAVING REDUCED LAYOUT AREA ANI LOWER POWER SUPPLY TRANSIENTS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I322578 | FULL BRIDGE INTEGRAL NOISE SHAPING FOR QUANTIZATION OF PULSE WIDTH MODULATION SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I323847 | DATA PROCESSING SYSTEM HAVING MULTIPLE REGISTER CONTEXTS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I324259 | METHOD OF TESTING FOR POWER AND GROUND CONTINUITY OF A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I324378 | METHOD OF MAKING SEMICONDUCTOR PACKAGE WITH REDUCED MOISTURE SENSITIVITY |
| FREESCALE SEMICONDUCTOR, INC. | TW | I325155 | METAL REDUCTION IN WAFER SCRIBE AREA |
| FREESCALE SEMICONDUCTOR, INC. | TW | I325169 | MULTI-ROW LEAD FRAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | I325626 | METHOD FOR PACKAGING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I326473 | MOUNTING SURFACES FOR ELECTRONIC DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | TW | I327690 | CLOSED LOOP CURRENT CONTROL CIRCUIT AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | I327848 | TRANSMITTER FOR A CONTROLLED-SHAPE SWITCHED SIGNAL ON A COMMUNICATION LINE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 1329350 | CAPACITOR ATTACHMENT METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | I329354 | MULTI-DIE SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 1329359 | METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITH AN AIR GAP FORMED USING A PHOTOSENSITIVE MATERIAL |
| FREESCALE SEMICONDUCTOR, INC. | TW | I329887 | METHOD OF PATTERNING ON A WAFER USING A RELECTIVE MASK WITH A MULTI-LAYER ARC |
| FREESCALE SEMICONDUCTOR, INC. | TW | I330365 | MEMORY HAVING A VARIABLE REFRESH CONTROL AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I330455 | LOW VOLTAGE LOW POWER CLASS A/B OUTPUT STAGE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I330876 | METHOD FOR FORMING MULTI-LAYER BUMPS ON A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I330895 | SEMICONDUCTOR ALIGNMENT AID |
| FREESCALE SEMICONDUCTOR, INC. | TW | I331276 | LOW VOLTAGE DETECTION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | TW | I332373 | METHOD FOR FABRICATING A PCB |
| FREESCALE SEMICONDUCTOR, INC. | TW | I333212 | VARIABLE GATE BIAS FOR A REFERENCE TRANSISTOR IN A NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | TW | I333260 | ENHANCMENT MODE METAL-OXIDE-SEMICONDUCTOR FIELD EFFECT TRANSISTOR AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | I334634 | AREA-ARRAY DEVICE ASSEMBLY WITH PRE-APPLIED UNDERFILL LAYERS ON PRINTED WIRING BOARD |
| FREESCALE SEMICONDUCTOR, INC. | TW | I334702 | RADIO RECEIVER HAVING A VARIABLE BANDWIDTH IF FILTER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I335139 | DIGITAL CLOCK FREQUENCY MULTIPLIER |
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| FREESCALE SEMICONDUCTOR, INC. | TW | I336106 | SEMICONDUCTOR FABRICATION METHOD FOR MAKING SMALL FEATURES |
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| FREESCALE SEMICONDUCTOR, INC. | TW | I336185 | METHOD AND APPARATUS FOR SHARED PROCESSING A PLURALITY OF SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I336476 | STORAGE CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I337377 | METHOD FOR FABRICATING DUAL-METAL GATE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I337384 | SEMICONDUCTOR FABRICATION PROCESS WITH ASYMMETRICAL CONDUCTIVE SPACERS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I337394 | METHOD OF PACKAGING SEMICONDUCTOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I337773 | INTEGRATED CIRCUIT DIE I/O CELLS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I337780 | METHOD OF ADDING MASS TO MEMS STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | TW | I338835 | METHOD AND APPARATUS FOR CONTROLLING A DATA PROCESSING SYSTEM DURING DEBUG |
| FREESCALE SEMICONDUCTOR, INC. | TW | I338940 | SEMICONDUCTOR PACKAGE HAVING OPTIMIZED WIRE BOND POSITIONING |
| FREESCALE SEMICONDUCTOR, INC. | TW | I339423 | MULTI-BIT NON-VOLATILE MEMORY DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I339425 | THIN GAAS WITH COPPER BACK-METAL STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I340442 | FLIP-CHIP ASSEMBLY WITH THIN UNDERFILL AND THICK SOLDER MASK |
| FREESCALE SEMICONDUCTOR, INC. | TW | I340443 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | I340989 | METHOD OF PATTERNING PHOTORESIST ON A WAFER USING AN ATTENUATED PHASE SHIFT MASK |
| FREESCALE SEMICONDUCTOR, INC. | TW | I341964 | CIRCUIT VOLTAGE REGULATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | I342044 | PROCESS FOR FORMING DUAL METAL GATE STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | TW | I342623 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | I344185 | METHOD FOR FORMING REINFORCED INTERCONNECTS ON A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I344191 | SEMICONDUCTOR DEVICE HAVING ELECTRICAL CONTACT FROM OPPOSITE SIDES AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I344688 | MULTIPLEXING OF DIGITAL SIGNALS AT MULTIPLE SUPPLY VOLTAGES IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | TW | I345165 | METHOD AND SYSTEM FOR DIRECT ACCESS TO A NON- MEMORY MAPPED DEVICE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | TW | I345710 | PREFETCH CONTROL IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | TW | I348217 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | I348278 | CAPACITIVE CHARGE PUMP |
| FREESCALE SEMICONDUCTOR, INC. | TW | I348768 | FLIPCHIP QFN PACKAGE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I349317 | LAND GRID ARRAY PACKAGED DEVICE AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | I349367 | SEMICONDUCTOR DEVICE AND MAKING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | I349985 | LAND GRID ARRAY PACKAGED DEVICE AND METHOD OF |

FORMING SAME

| FREESCALE SEMICONDUC | CTOR, INC. | TW | I350000 | CONFINED SPACERS FOR DOUBLE GATE TRANSISTOR SEMICONDUCTOR FABRICATION PROCESS |
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| FREESCALE SEMICONDUC | CTOR, INC. | TW | I351081 | ELECTRONIC COMPONENT AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I352293 | PREFETCH CONTROL IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I353010 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I353018 | MICELLAR TECHNOLOGY FOR POST-ETCH RESIDUES |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I353600 | DECOUPLING TECHNIQUE FOR OPTICAL DISK DRIVE OPTICAL PICKUP UNITS |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I354346 | INTEGRATED CIRCUIT WITH TEST PAD STRUCTURE AND METHOD OF TESTING |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I354362 | SEMICONDUCTOR DEVICE WITH STRAIN RELIEVING BUMP DESIGN |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I356491 | SEMICONDUCTOR STRUCTURE WITH DIFFERENT LATTICE CONSTANT MATERIALS AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I356598 | SIGNAL GENERATION POWER MANAGEMENT CONTROL SYSTEM FOR PORTABLE COMMUNICATIONS DEVICE AND METHOD OF USING SAME |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I358080 | METHOD AND APPARATUS FOR FORMING AN SOI BODY-CONTACTED TRANSISTOR |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I358389 | MICROELECTROMECHANICAL (MEM) DEVICE INCLUDING A SPRING RELEASE BRIDGE AND METHOD OF MAKING THE SAME |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I358633 | METHOD AND APPARATUS FOR AFFECTING A PORTION OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I358636 | APPARATUS AND METHOD FOR TIME ORDERING EVENTS IN A SYSTEM HAVING MULTIPLE TIME DOMAINS |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I358644 | METHOD AND APPARATUS FOR REDUCING INTERRUPT LATENCY BY DYNAMIC BUFFER SIZING |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I358662 | MULTIPLE BURST PROTOCOL DEVICE CONTROLLER |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I358663 | METHOD AND APPARATUS FOR ALLOCATING ENTRIES IN A BRANCH TARGET BUFFER |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I358835 | SCHOTTKY DEVICE AND METHOD OF FORMING |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I358901 | CIRCUIT AND METHOD FOR DETERMINING OPTIMAL POWER AND FREQUENCY METRICS OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I359464 | SEMICONDUCTOR TRANSISTOR HAVING STRUCTURAL ELEMENTS OF DIFFERING MATERIALS AND METHOD OF FORMATION |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I360818 | NONVOLATILE MEMORY AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I360863 | TRANSISTOR HAVING THREE ELECTRICALLY ISOLATED ELECTRODES AND METHOD OF FORMATION |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I360978 | NETWORK MESSAGE PROCESSING USING INVERSE PATTERN MATCHING |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I360991 | METHOD AND APPARATUS FOR PROVIDING SECURITY FOR DEBUG CIRCUITRY |
| FREESCALE SEMICONDUC | CTOR, INC. | TW | I361453 | SEMICONDUCTOR WAFER WITH IMPROVED CRACK PROTECTION |
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| FREESCALE SEMICONDUCTOR, INC. | TW | I361489 | TRANSISTOR WITH INDEPENDENT GATE STRUCTURES |
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| FREESCALE SEMICONDUCTOR, INC. | TW | I362073 | HIGH K DIELECTRIC FILM |
| FREESCALE SEMICONDUCTOR, INC. | TW | I364057 | SEMICONDUCTOR DEVICE AND METHOD OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | I364813 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING ISOLATION REGIONS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I365529 | METHOD OF FORMING A SEMICONDUCTOR PACKAGE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | I366899 | SCRIBE STREET STRUCTURE FOR BACKEND INTERCONNECT SEMICONDUCTOR WAFER INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | I366984 | METHOD AND APPARATUS FOR DYNAMICALLY INSERTING GAIN IN AN ADAPTIVE FILTER SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | TW | I367520 | INTEGRATED CIRCUIT WITH MULTIPLE SPACER INSULATING REGION WIDTHS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I367543 | METHOD FOR FORMING A PASSIVATION LAYER FOR AIR GAP FORMATION AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | I367630 | LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | TW | I368227 | INTEGRATED CIRCUIT POWER MANAGEMENT FOR REDUCING LEAKAGE CURRENT IN CIRCUIT ARRAYS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I369684 | LOW-POWER COMPILER-PROGRAMMABLE MEMORY WITH FAST ACCESS TIMING |
| FREESCALE SEMICONDUCTOR, INC. | TW | I370520 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT, AND SEMICONDUCTOR COMPONENT FORMED THEREBY |
| FREESCALE SEMICONDUCTOR, INC. | TW | I371087 | GRADED SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | TW | I371092 | THERMALLY ENHANCED MOLDED PACKAGE FOR SEMICONDUCTORS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I372470 | SCHOTTKY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I374357 | MASKING WITHIN A DATA PROCESSING SYSTEM HAVING APPLICABILITY FOR A DEVELOPMENT INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I374572 | MULTYLAYER CAVITY SLOT ANTENNA |
| FREESCALE SEMICONDUCTOR, INC. | TW | I375158 | LAYOUT MODIFICATION USING MULTILAYER-BASED CONSTRAINTS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I375303 | METHOD OF DISCHARGING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I375318 | METHOD OF FORMING A NANOCLUSTER CHARGE STORAGE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I375328 | HIGH VOLTAGE FIELD EFFECT DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | I376776 | WIREBONDING INSULATED WIRE AND CAPILLARY THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I377169 | Z-AXIS ACCELEROMETER WITH AT LEAST TWO GAP SIZES AND TRAVEL STOPS DISPOSED OUTSIDE AN ACTIVE CAPACITOR AREA |
| FREESCALE SEMICONDUCTOR, INC. | TW | I377615 | ULTRA-THIN DIE AND METHOD OF FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | I377625 | METHOD OF SEMICONDUCTOR FABRICATION INCORPORATING DISPOSABLE SPACER INTO ELEVATED SOURCE/DRAIN PROCESSING |
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TW I377626 SCHOTTKY DEVICE AND METHOD OF FORMING

FREESCALE SEMICONDUCTOR, INC.

| FREESCALE SEMICONDUCTOR, INC. | TW | I377634 | RADIO FREQUENCY CIRCUIT WITH INTEGRATED ON-CHIP RADIO FREQUENCY SIGNAL COUPLER |
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| FREESCALE SEMICONDUCTOR, INC. | TW | I377649 | SEMICONDUCTOR DEVICE HAVING NITRIDATED OXIDE LAYER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I378622 | I/O CELL ESD SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | TW | I379340 | ISOLATION TRENCH |
| FREESCALE SEMICONDUCTOR, INC. | TW | I379570 | METHOD AND APPARATUS FOR ENDIANNESS CONTROL IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | TW | I380374 | SEMICONDUCTOR FABRICATION PROCESS INCLUDING RECESSED SOURCE/DRAIN REGIONS IN AN SOI WAFER |
| FREESCALE SEMICONDUCTOR, INC. | TW | I380549 | APPARATUS, MOBILE DEVICE AND METHOD FOR HIGH SPEED VOLTAGE REGULATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | I380578 | MULTIPLE REFERENCE CLOCK SYNTHESIZER |
| FREESCALE SEMICONDUCTOR, INC. | TW | I382449 | SEMICONDUCTOR PROCESS AND INTEGRATED CIRCUIT HAVING DUAL METAL OXIDE GATE DIELECTRIC WITH SINGLE METAL GATE ELECTRODE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I383431 | METHOD FOR FORMING A PHOTORESIST PATTERN |
| FREESCALE SEMICONDUCTOR, INC. | TW | I383584 | METHOD OF COMPENSATING PARASITIC COUPLING BETWEEN RF OR MICROWAVE TRANSISTORS IN THE SAME PACKAGE, PACKAGED ELECTRONIC DEVICE, RF AMPLIFIER, AND MICROWAVE AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | TW | I384527 | DECOUPLED COMPLEMENTARY MASK PATTERNING TRANSFER METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | I385733 | METAL GATE TRANSISTOR FOR CMOS PROCESS AND METHOD FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | TW | I387008 | SEMICONDUCTOR FABRICATION PROCESS INCLUDING SILICIDE STRINGER REMOVAL PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | TW | I387848 | TEMPLATE LAYER FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | I388010 | TREATMENT SOLUTION AND METHOD OF APPLYING A PASSIVATING LAYER |
| FREESCALE SEMICONDUCTOR, INC. | TW | I388053 | THIN-FILM CAPACITOR WITH A FIELD MODIFICATION LAYER AND METHODS FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | I389200 | METHOD OF FORMING AN INTERLAYER DIELECTRIC |
| FREESCALE SEMICONDUCTOR, INC. | TW | I389221 | DIE ENCAPSULATION USING A POROUS CARRIER |
| FREESCALE SEMICONDUCTOR, INC. | TW | I389222 | IMPROVEMENTS IN OR RELATING TO LEAD FRAME BASED SEMICONDUCTOR PACKAGE AND A METHOD OF MANUFACTURING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | I389226 | METHOD AND APPARATUS FOR PROVIDING STRUCTURAL SUPPORT FOR INTERCONNECT PAD WHILE ALLOWING SIGNAL CONDUCTANCE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I389258 | METHOD OF MAKING A DUAL STRAINED CHANNEL SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I389281 | METHOD OF FORMING FLIP-CHIP BUMP CARRIER TYPE PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I389297 | MIM CAPACITOR IN A SEMICONDUCTOR DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I389311 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE |
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| FREESCALE SEMICONDUCTOR, INC. | TW | I389313 | TRANSITIONAL DIELECTRIC LAYER TO IMPROVE RELIABILITY AND PERFORMANCE OF HIGH DIELECTRIC CONSTANT TRANSISTORS |
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| FREESCALE SEMICONDUCTOR, INC. | TW | I390674 | SOURCE SIDE INJECTION STORAGE DEVICE WITH CONTROL GATES ADJACENT TO SHARED SOURCE/DRAIN AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I390705 | ESD PROTECTION FOR PASSIVE INTEGRATED DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | TW | I390710 | SPLIT GATE MEMORY CELL IN A FINFET |
| FREESCALE SEMICONDUCTOR, INC. | TW | I390726 | INTERLAYER DIELECTRIC UNDER STRESS FOR AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | TW | I390736 | ELECTRONIC DEVICE INCLUDING SEMICONDUCTOR ISLANDS OF DIFFERENT THICKNESSES OVER AN INSULATING LAYER AND A PROCESS OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | 1391993 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING A SILICIDE LAYER |
| FREESCALE SEMICONDUCTOR, INC. | TW | I392032 | METHODS AND APPARATUS HAVING WAFER LEVEL CHIP SCALE PACKAGE FOR SENSING ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I393176 | IDEA FOR FORMING FUSI GATE WITH HIGH GATE DIELECTRIC |
| FREESCALE SEMICONDUCTOR, INC. | TW | I393190 | SEMICONDUCTOR DEVICES AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | I393228 | FLIP CHIP AND WIRE BOND SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I393255 | LDMOS TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I394233 | SEMICONDUCTOR DEVICE AND METHOD FOR REGIONAL STRESS CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | TW | I394237 | METHOD OF FORMING A SEMICONDUCTOR PACKAGE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | I394283 | ELECTRONIC DEVICE AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I395257 | WIDE AND NARROW TRENCH INFORMATION IN HIGH ASPECT RATIO MEMS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I395297 | SOURCE SIDE INJECTION STORAGE DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I395329 | COMPLEMENTARY METAL-OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 1396238 | METHOD OF FORMING A NANOCLUSTER CHARGE STORAGE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 1396257 | ELECTRONIC DEVICE INCLUDING DISCONTINUOUS STORAGE ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | TW | 1396277 | METHOD OF FORMING A SEMICONDUCTOR DEVICE AND AN OPTICAL DEVICE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | I397128 | METHOD OF MAKING A PLANAR DOUBLE-GATED TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I397129 | A METHOD OF MAKING A METAL GATE SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I397132 | FABRICATION OF THREE DIMENSIONAL INTEGRATED CIRCUIT EMPLOYING MULTIPLE DIE PANELS |
| FREESCALE SEMICONDUCTOR, INC. | TW | 1397961 | PROCESS FOR FORMING AN ELECTRONIC DEVICE INCLUDING A FIN-TYPE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I399536 | PROCESS FOR TESTING A REGION FOR AN ANALYTE AND A PROCESS FOR FORMING AN ELECTRONIC DEVICE. |

PROCESS FOR FORMING AN ELECTRONIC DEVICE

| FREESCALE SEMICONDUCTOR, INC. | TW | 1399793 | SUBSTRATE CONTACT FOR A CAPPED MEMS AND METHOD OF MAKING THE SUBSTRATE CONTACT AT THE WAFER LEVEL |
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| FREESCALE SEMICONDUCTOR, INC. | TW | I399794 | PLASMA TREATMENT OF A SEMICONDUCTOR SURFACE FOR ENHANCED NUCLEATION OF A METAL-CONTAINING LAYER |
| FREESCALE SEMICONDUCTOR, INC. | TW | I399797 | SEMICONDUCTOR DEVICE AND METHOD OF FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I399807 | METHOD FOR CLEANING A SEMICONDUCTOR STRUCTURE AND CHEMISTRY THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I399847 | TUNABLE ANTIFUSE ELEMENT AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I400773 | CIRCUIT DEVICE WITH AT LEAST PARTIAL PACKAGING AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | TW | I401789 | METHOD AND APPARATUS FOR FORMING A NOBLE METAL LAYER NOTABLY ON INLAID METAL FEATURES |
| FREESCALE SEMICONDUCTOR, INC. | TW | I402674 | APPARATUS AND METHOD FOR PROVIDING INFORMATION TO A CACHE MODULE USING FETCH BURSTS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I402888 | LATERALLY GROWN NANOTUBES AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | I402891 | METHOD OF DISTANCING A BUBBLE AND BUBBLE DISPLACEMENT APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I402892 | METHOD OF PATTERNING A LAYER USING A PELLICLE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I402942 | MEMORY WITH RECESSED DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | TW | I402943 | SOI ACTIVE-LAYER WITH DIFFERENT SURFACE ORIENTATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | I402960 | GROUND SHIELDS FOR SEMICONDUCTORS |
| FREESCALE SEMICONDUCTOR, INC. | TW | I402986 | RECESSED SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | I403744 | METHOD AND APPARATUS FOR TESTING A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | TW | I404087 | BALUN SIGNAL TRANSFORMER AND METHOD OF FORMING |
| FREESCALE SEMICONDUCTOR, INC. | TW | I404132 | PLATEN ENDPOINT WINDOW WITH PRESSURE RELIEF |
| FREESCALE SEMICONDUCTOR, INC. | TW | I404172 | ELECTRONIC DEVICE INCLUDING GATE LINES, BIT LINES, OR A COMBINATION THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | I404206 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING A FIN AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | I406409 | TRANSISTOR STRUCTURE WITH STRESS MODIFICATION AND CAPACITIVE REDUCTION FEATURE IN A WIDTH DIRECTION AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | I406422 | METHODS FOR PROGRAMMING A FLOATING BODY NONVOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | TW | I406554 | CELLULAR MODEM PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | TW | I407492 | NON-VOLATILE NANOCRYSTAL MEMORY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | I407514 | LEAD SOLDER INDICATOR AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-110552-A | DC OFFSET REDUCTION IN A ZERO-IF TRANSMITTER |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-110645-A | A SEMICONDUCTOR DEVICE HAVING NO DIE SUPPORTING SURFACE AND METHOD FOR MAKING THE SAME |
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| FREESCALE SEMICONDUCTOR, INC. | MY | MY-111907-A | METHOD FOR PLATING USING NESTE D PLATING BUSES AND |
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| | | | SEMICONDUC TOR DEVICE HAVING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-111992-A | INTERLOCKING AND INVERTIBLE SE MICONDUCTOR DEVICE TRAY AND TE ST CONTACTOR MATING THERETO |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-112223-A | LEADFRAME STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-112466-A | BUMPED SEMICONDUCTOR DEVICE AN D METHOD FOR PROBING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-113012-A | METHOD FOR MAKING AN ELECTRONI C COMPONENT HAVING AN ORGANIC SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-113129-A | SEMICONDUCTOR DEVICE HAVING BU ILT-IN HIGH FREQUENCY BYPASS C APACITOR AND METHOD FOR ITS FA BRICATION |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-117410-A | ELECTRONIC COMPONENT ASSEMBLY HAVING AN ENCAPSULATION MATERIAL AND METHOD OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-118387-A | METHOD FOR TESTING ELECTRONIC DEVICES ATTACHED TO A LEADFRAM E |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-118958-A | METHOD OF MANUFACTURING ELECTRONIC COMPONENTS |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-119257-A | ELECTRONIC COMPONENT PACKAGING STRUCTURE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-119300-A | METHOD OF PACKAGING A SEMICONDUCTOR DIE AND A LEADFRAME STRUCTURE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-119490-A | FEED-IN APPARATUS IN A ROTARY TRIM AND FORM |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-119990-A | MULTI-STRAND SUBSTRATE FOR BAL L-GRID ARRAY ASSEMBLIES AND ME THOD |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-120808-A | METHOD AND APPARATUS FOR VISUALLY INSPECTING AN OBJECT |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-121274-A | A METHOD AND APPARATUS FOR ATT ACHING LEADS TO A PRINTED CIRC UIT BOARD |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-121564-A | LOADING APPARATUS IN A ROTARY TRIM AND FORM |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-121948-A | ROTARY TRIM AND FORM |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-122100-A | PACKAGING APPARATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-122776-A | METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-123164-A | SURFACE MOUNTABLE FLEXIBLE INTERCONNECT |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-123187-A | SEMICONDUCTOR DEVICE HAVING A SUB-CHIP-SCALE PACKAGE STRUCTU RE AND METHOD FOR FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-123665-A | ROUNDED EXTENDED CORNER BOAT |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-123854-A | A METHOD AND AN APPARATUS FOR FORMING SEMICONDUCTOR PACKAGES ON A LEADFRAME |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-124447-A | METHOD AND APPARATUS FOR MOUNT ING A SEMICONDUCTOR WAFER ON A FILM RING |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-125701-A | A METHOD OF SURFACE MOUNTING AN ELECTRICAL COMPONENT ON A PRINTED CIRCUIT BOARD AND APPARATUS THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-125704-A | SEMICONDUCTOR DEVICE HAVING X- SHAPED DIE SUPPORT MEMBER AND METHOD FOR MAKING THE SAME |

| FREESCALE SEMICONDUCTOR, INC. | MY | MY-126026-A | METHOD AND APPARATUS FOR EXTEN DING FATIGUE LIFE OF SOLDER JO INTS IN A SEMICONDUCTOR DEVICE |
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| FREESCALE SEMICONDUCTOR, INC. | MY | MY-126325-A | A METHOD FOR MANUFACTURING A LOW DIELECTRIC CONSTANT INTERLEVEL INTEGRATED CIRCUIT STRUCTU RE |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-126386-A | METHOD FOR MULTIPLEXED JOINING OF SOLDER BUMPS TO VARIOUS SUBSTRATES DURING ASSEMBLY OF AN INTEGRATED CIRCUIT PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-126496-A | WIRE BONDING SUPPORT STRUCTURE AND METHOD FOR COUPLING A SEM ICONDUCTOR CHIP TO A LEADFRAME |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-126502-A | PROCESS FOR DEPOSITING A LAYER OF MATERIAL ON A SUBSTRATE AN D A PLATING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-127428-A | UV CURE PROCESS AND TOOL FOR LOW K FILM FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-129101-A | METHOD AND APPARATUS FOR TESTING AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-131124-A | WIRE BOND-LESS ELECTRONIC COMPONENT FOR USE WITH AN EXTERNAL CIRCUIT AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-131407-A | METHOD FOR UNIFORM POLISH IN MICROELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-132041-A | SWITCH ASSEMBLY AND METHOD OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-135366-A | DISTRIBUTED AMPLIFIER HAVING SEPARATELY BIASED SECTIONS |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-136179-A | PACKAGED DEVICE AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-136290-A | FLIP-CHIP ASSEMBLY WITH THIN UNDERFILL AND THICK SOLDER MASK |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-137055-A | SIMPLIFICATION OF BALL ATTACH METHOD USING SUPER- SATURATED FINE CRYSTAL FLUX |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-137077-A | LOW-PRESSURE LAMINATED CERAMIC DEVICES AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-137390-A | AREA-ARRAY DEVICE ASSEMBLY WITH PRE-APPLIED UNDERFILL LAYERS ON PRINTED WIRING BOARD |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-138000-A | METHOD OF FORMING A SUBSTRATELESS SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-139006-A | LEAD SOLDER INDICATOR AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-139152-A | METHOD OF TESTING FOR POWER AND GROUND CONTINUITY OF A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-139795-A | LEADFRAME FOR A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-140584-A | SEMICONDUCTOR DEVICE WITH A PROTECTED ACTIVE DIE REGION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-146062-A | METHOD OF MAKING EXPOSED PAD BALL GRID ARRAY PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-146202-A | MOUNTING SURFACES FOR ELECTRONIC DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-146897-A | POWER LEAD-ON-CHIP BALL GRID ARRAY PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | MY | MY-147815-A | UNDERFILL DISPENSING FOR INTEGRATED CIRCUITS |

| FREESCALE SEMICONDUCTOR, INC. | TW | NI-070383 | METHOD AND APPARATUS FOR NOISE BURST DETECTION IN A SIGNAL P ROCESSOR |
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| FREESCALE SEMICONDUCTOR, INC. | TW | NI-070433 | METHOD AND APPARATUS FOR TESTI NG A STATIC RAM |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-070648 | CONFIGURABLE LOGIC ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-074585 | EEPROM CELL WITH ISOLATION TRA NSISTOR AND METHODS FOR MAKING AND OPERATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-075183 | METHOD FOR CHEMICAL MECHANICAL POLISHING A SEMICONDUCTOR DEV ICE USING SLURRY |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-076276 | BUMPED SEMICONDUCTOR DEVICE AN D METHOD FOR PROBING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-076476 | PROCESS FOR POLISHING AND ANAL YZING A LAYER OVER A PATTERNED SEMICONDUCTOR SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-078500 | SEMICONDUCTOR DEVICE HAVING A REDUCING/OXIDIZING CONDUCTIVE MATERIAL AND A PROCESS FOR FOR MING THE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-078800 | MULTI-STRAND SUBSTRATE FOR BAL L-GRID ARRAY ASSEMBLIES AND ME THOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-080666 | SEMICONDUCTOR DEVICE HAVING BU ILT-IN HIGH FREQUENCY BYPASS C APACITOR AND METHOD FOR ITS FA BRICATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-081825 | METHOD FOR FORMING A DIELECTRI C HAVING IMPROVED PERFORMANCE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-082173 | SEMICONDUCTOR DEVICE HAVING FI ELD ISOLATION AND A PROCESS FO R FORMING THE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-082451 | SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-084726 | METHOD AND APPARATUS FOR IMPRO VING UTILIZATION OF LIMITED RE SOURCES |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-084954 | PROCESS FOR FORMING A SEMICOND UCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-085624 | CONDUCTIVE INTERCONNECT STRUCT URE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-085748 | FET WITH STABLE THRESHOLD VOLT AGE AND METHOD OF MANUFACTURIN G THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-086947 | NON-VOLATILE REGISTER AND METH OD FOR ACCESSING DATA THEREIN |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-087345 | METHOD AND SYSTEM FOR PERFORMI NG A CONVOLUTION OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI087346 | INTEGRATED CIRCUIT INPUT-OUTPU T PROCESSOR HAVING IMPROVED TI MER CAPABILITY |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-089869 | SYSTEM FOR DATA SYNCHRONIZATIO N |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-089916 | METHOD FOR MAKING A MOISTURE R ESISTANT SEMICONDUCTOR DEVICE HAVING AN ORGANIC SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-090456 | SWITCHABLE LENS/DIFFUSER |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-092121 | METHOD AND APPARATUS FOR ACCES SING A REGISTER IN A DATA PROC ESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-092178 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-092500 | METHOD AND APPARATUS FOR PROVI DING ERASING AND PROGRAMMING P ROTECTION FOR ELECTRICALLY ERA |

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| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 092946 | METHOD FOR REDUCING POWER CONS UMPTION IN A PORTABLE ELECTRON IC DEVICE WITH A LIQUID CRYSTA L DISPLAY SCREEN |
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| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 093230 | INTEGRATED CIRCUIT MEMORY USIN G FUSIBLE LINKS IN A SCAN CHAI N |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 094302 | DYNAMIC MEMORY DEVICE WITH REF RESH METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 094771 | LED DISPLAY PACKAGING WITH SUB STRATE REMOVAL AND METHOD OF F ABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 094822 | METHOD AND APPARATUS FOR TESTI NG A SEMICONDUCTOR WAFER |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 094969 | LOW VOLTAGE REFERENCE CIRCUIT AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 095409 | INTEGRATED CIRCUIT HAVING A DU MMY STRUCTURE AND METHOD OF MA KING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 095799 | MEMORY SUITABLE FOR OPERATION AT LOW POWER SUPPLY VOLTAGES A ND SENSE AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 097741 | METHOD OF FORMING A SEMICONDUC TOR METALLIZATION SYSTEM AND S TRUCTURE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 097886 | METHOD FOR MAKING SEMICONDUCTO R DEVICES HAVING ELECTROPLATED LEADS |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 098348 | CIRCUIT AND METHOD OF COMPENSA TING FOR MEMBRANE STRESS IN A SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 098625 | DATA PROCESSING SYSTEM HAVING A MULTI-FUNCTION SCALABLE PARA LLEL INPUT/OUTPUT PORT |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 099008 | NON-BREAKDOWN TRIGGERED ELECTR OSTATIC DISCHARGE PROTECTION C IRCUIT FOR AN INTEGRATED CIRCU IT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 099089 | METHOD FOR FORMING A TRENCH IS OLATION STRUCTURE IN AN INTEGR ATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 099377 | DATA PROCESSING SYSTEM HAVING A SELF-ALIGNING STACK POINTER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 099406 | METHOD AND APPARATUS FOR TRANS PORTING AND USING A SEMICONDUC TOR SUBSTRATE CARRIER |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 100294 | METHOD AND APPARATAUS FOR SEMI CONDUCTOR DEVICE OPTIMIZATION USING ON-CHIP VERIFICATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 100481 | PROCESS FOR FORMING A SEMICOND UCTOR DEVICE WITH AN ANTIREFLE CTIVE LAYER |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 100646 | METHOD FOR GENERATING A MAPPIN G FOR AN ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 100956 | SEMICONDUCTOR PACKAGE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 102320 | METHOD FOR MAKING AN ELECTRONI C COMPONENT HAVING AN ORGANIC SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 103193 | METHOD FOR DESIGNING AN ARCHIT ECTURAL SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 103219 | SELECTIVELY FILLED ADHESIVE FILM CONTAINING A FLUXING AGENT |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 103221 | METHOD FOR DEPOSITING A DIFFUSION BARRIER |
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| FREESCALE SEMICONDUCTOR, INC. | TW | NI-112457 | INTEGRATED CIRCUIT MEMORY WITH MULTIPLEXED REDUNDANT COLUMN DATA PATH |
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| FREESCALE SEMICONDUCTOR, INC. | TW | NI-112483 | METHOD AND APPARATUS FOR ELECT RONICALLY COMMUTING AN ELECTRI C MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-112719 | METHOD AND APPARATUS FOR INTER FACING A PROCESSOR TO A COPROC ESSOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-112867 | VARIABLE CAPACITOR AND METHOD FOR FABRICATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-113329 | NEURAL NETWORK UTILIZING LOGAR ITHMIC FUNCTION AND METHOD OF USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-113676 | CIRCUIT FOR ELECTROSTATIC DISC HARGE (ESD) PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-113818 | METHOD OF CHEMICAL MECHANICAL PLANARIZATION USING A WATER RI NSE TO PREVENT PARTICLE CONTAM INATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-114688 | PACKAGING APPARATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-115008 | METHOD OF FORMING A SEMICONDUC TOR DEVICE HAVING DUAL INLAID STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-115595 | POINT OF USE DILUTION TOOL AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-116158 | LNS-BASED COMPUTER PROCESSOR A ND METHOD OF USE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-116289 | SENSE AMPLIFIER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-116916 | SEMICONDUCTOR PACKAGE BOND POST CONFIGURATION AND METHOD OF MANUFACTURING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-117457 | REFERENCE CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-118218 | SEMICONDUCTOR DEVICE MEMORY CELL, AND PROCESSES FOR FORMING THEM |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-119203 | INTERCONNECT STRUCTURE IN A SEMICONDUCTOR DEVICE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-119819 | CHEMICAL—MECHANICAL POLISHER AND A PROCESS FOR POLISHING |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-120195 | METHOD OF FORMING A SEMICONDUC TOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-120830 | WIRE BONDING SUPPORT STRUCTURE AND METHOD FOR COUPLING A SEM ICONDUCTOR CHIP TO A LEADFRAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-121412 | INTEGRATED CIRCUIT INTERCONNEC T METHOD AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-121466 | MEMORY DEVICE WITH FAST WRITE RECOVERY AND RELATED WRITE REC OVERY METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-121488 | PROCESS FOR FORMING A SEMICOND UCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-121732 | METHOD OF PROBING A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-122644 | SEMICONDUCTOR DEVICE HAVING MULTIPLE OVERLAPPING ROWS OF BOND PADS WITH CONDUCTIVE INTERCONNECTS AND METHOD OF PAD PLACE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-123415 | METHOD FOR REDUCING PARTICLES ON A SUBSTRATE USING CHUCK CLE ANING |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-123878 | ETCHING APPARATUS AND METHOD OF ETCHING A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-124296 | DUAL BAND MOBILE PHONE HANDSET |
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| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 125600 | METHOD FOR MULTIPLEXED JOINING OF SOLDER BUMPS TO VARIOUS SUBSTRATES DURING ASSEMBLY OF AN INTEGRATED CIRCUIT PACKAGE |
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| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 125837 | METHOD FOR FORMING INTERCONNEC T BUMPS ON A SEMICONDUCTOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 126120 | RADIO WITH HALTING APPARATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 126424 | SEMICONDUCTOR DEVICE FOR SUBST RATE TRIGGERED ELECTROSTATIC D ISCHARGE PROTECTION AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 126721 | SEMICONDUCTOR DEVICE AND ALIGNMENT METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 127236 | METHOD AND APPARATUS FOR PROCE SSING A SEMICONDUCTOR WAFER ON A ROBOTIC TRACK HAVING ACCESS TO IN SITU WAFER BACKSIDE PAR TICLE DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 127542 | SEMICONDUCTOR DEVICE HAVING A SUB-CHIP-SCALE PACKAGE STRUCTU RE AND METHOD FOR FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 128118 | SYNCHRONOUS PIPELINED BURST ME MORY AND METHOD FOR OPERATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 129129 | METHOD FOR FORMING AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 130162 | A CIRCUIT AND METHOD FOR RETAINING DATA IN DRAM IN A PORTABLE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 130800 | CIRCUIT AND METHOD OF FREQUENC Y SYNTHESIZER CONTROL WITH A S ERIAL PERIPHERAL INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 132089 | PROCESS FOR FORMING A SEMICOND UCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 132575 | PROCESS FOR FORMING A CONDUCTI VE STRUCTURE AND A SEMICONDUCT OR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 133678 | MULTI-WAY CACHE APPARATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 133740 | PROGRAMMABLE DELAY CONTROL IN A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 135073 | DATA PROCESSING SYSTEM HAVING BRANCH CONTROL AND METHOD THER EOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 135166 | CLOCK RECOVERY CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 136364 | FAST START-UP PROCESSOR CLOCK GENERATION METHOD AND SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 137073 | COMPUTER INSTRUCTION WHICH GENERATES MULTIPLE RESULTS OF DIFFERENT DATA TYPES TO IMPROVE S OFTWARE EMULATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 137854 | ARRANGEMENT FOR ENCRYPTION DEC RYPTION OF DATA AND DATA CARRI ER INCORPORATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 138887 | PIPELINED DUAL PORT INTEGRATED CIRCUIT MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 138939 | SENSING CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 139705 | A MEMORY DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 139943 | PROCESS FOR FORMING A SEMICOND UCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI- 140216 | CIRCUIT AND METHOD FOR REDUCIN G PARASITIC BIPOLAR EFFECTS DU RING ELECTROSTATIC DISCHARGES |

| FREESCALE SEMICONDUCTOR, INC. | TW | NI-141126 | METHOD FOR FABRICATING A SEMIC ONDUCTOR STRUCTURE HAVING A CR YSTALLINE ALKALINE EARTH METAL OXIDE INTERFACE WITH SILICON |
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| FREESCALE SEMICONDUCTOR, INC. | TW | NI-141399 | SEMICONDUCTOR DEVICE AND PROCESS FOR MANUFACTURING AND PACAKAGING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-142099 | INTEGRATED CIRCUIT MEMORY HAVI NG A FUSE DETECT CIRCUIT AND M ETHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-142131 | INTEGRATED CIRCUIT HAVING STAN DBY CONTROL FOR MEMORY AND MET HOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-142884 | METHOD FOR FORMING A SEMICONDU CTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-142888 | CMOS SEMICONDUCTOR DEVICES AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-144648 | METHOD FOR FORMING A BARRIER L AYER FOR USE IN A COPPER INTER CONNECT |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-145289 | METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE HAVING A STABLE CRYSTALLINE INTERFACE WITH SILICON |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-145744 | DIGITAL COMMUNICATONS PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-146448 | METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE INCLUDING A METAL OXIDE INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-146581 | METHOD FOR PROCESSING A SEMICO NDUCTOR SUBSTRATE HAVING A COP PER SURFACE DISPOSED THEREON A ND STRUCTURE FORMED |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-147768 | SEMICONDUCTOR STRUCTURE HAVING A CRYSTALLINE ALKALINE EARTH METAL SILICON NITRIDE/OXIDE INTERFACI WITH SILICON |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-147847 | SEMICONDUCTOR DEVICE MEMORY CELL AND METHOD FOR SELECTIVELY ERASING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-148695 | METHOD AND APPARATUS FOR TRANS FERRING DATA OVER A PROCESSOR INTERFACE BUS |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-148866 | MEMORY UTILIZING A PROGRAMMABLE DELAY TO CONTROL ADDRESS BUFFERS |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-148882 | SEMICONDUCTOR DEVICE AND A PROCESS FOR FORMING THE SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-148958 | A SIGNAL PROCESSING CIRCUI |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-151023 | METHOD AND APPARATUS FOR A CALIBRATED FREQUENCY MODULATION PHASE LOCKED LOOP |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-151294 | INTEGRATED CIRCUIT HVING A BALANCED TWIST FOR DIFFERENTIAL SIGNAL LINES |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-152854 | MECHANICALLY ROBUST PAD INTERFACE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-152869 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE AND A CONDUCTIVE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-152908 | METHOD OF FORMING A COPPER LAY ER OVER A SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-152921 | SEMICONDUCTOR DEVICE, A PROCESS FOR A SEMICONDUCTOR DEVICE, AND A PROCESS FOR MAKING A |

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| FREESCALE SEMICONDUCTOR, INC. | TW | NI-153338 | LINEAR CAPACITOR STRUCTURE IN A CMOS PROCESS |
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| FREESCALE SEMICONDUCTOR, INC. | TW | NI-153383 | SEMICONDUCTOR STURCTURE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-153858 | REAL-TIME PROCESSOR DEBUG SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-155663 | MICRO ELECTRO-MECHANICAL SYSTEM SENSOR WITH SELECTIVE ENCAPSULATION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-156107 | METHOD OF OPERATING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-156701 | SEMICONDUCTOR DEVICE AND METHO D OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-157025 | METHOD AND APPARATUS FOR MANUFACTURING AN INTERCONNECT STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-158223 | MEMORY CELL, METHOD OF FORMATION, AND OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-158596 | COMMUNICATING DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-158692 | METHOD AND APPARATUS FOR AFFEC TING SUBSEQUENT INSTRUCTION PR OCESSING IN A DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-158792 | HYBRID SEMICONDUCTOR STRUCTURE AND DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-159344 | SELF CALIBRATING VCO CORRECTION CIRCUIT AND METHOL OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-159393 | SEMICONDUCTOR STURCTURE, SEMICONDUCTOR DEVICE, COMMUNICATING DEVICE, INTEGRATED CIRCUIT, AND PROCESS FOR FABRICATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-159780 | DATA PROCESSOR SYSTEM AND INST RUCTION SYSTEM USING GROUPING |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-160662 | CIRCUIT FOR RF BUFFER AND METH OD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-161852 | METHOD AND APPARATUS FOR CONFIGURING A DATA PROCESSING SYSTEM AFTER RESET |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-163252 | SINGLE SUPPLY HFET WITH TEMPERATURE COMPENSATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-163317 | SEMICONDUCTOR DEVICE HAVING PASSIVE ELEMENTSS ANI METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-163677 | METHOD OF MANUFACTURING ELECTRONIC COMPONENTS |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-164050 | PEAK PROGRAM CURRENT REDUCTION APPARATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-164263 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND CHEMICAL-MECHANICAL POLISHING SYSTEM THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-164375 | SEMICONDUCTOR DEVICE AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-164833 | PRECURSORS FOR INCORPORATING NITROGEN INTO A DIELECTRIC LAYER |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-165130 | METHOD FOR UNIFORM POLISH IN MICROELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-165135 | METHOD FOR FORMING AN ELECTRICALLY CONDUCTIVE INTERCONNECTION BETWEEN TWO SEMICONDUCTOR LAYERS, AND MULTILAYER SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-165165 | SEMICONDUCTOR STRUCTURE HAVING HIGH DIELECTRIC CONSTANT MATERIAL |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-165380 | ULTRA-LATE PROGRAMMING ROM AND METHOD OF MANUFACTURE |
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| FREESCALE SEMICONDUCTOR, INC. | TW | NI-165498 | MICROELECTRONIC PIEZOELECTRIC STRUCTURE AND METHOD OF FORMING THE SAME |
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| FREESCALE SEMICONDUCTOR, INC. | TW | NI-165842 | METHOD FOR FORMING A SEMICONDU CTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-166226 | MOCVD-GROWN EMODE HIGFET BUFFER |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-166609 | METHOD OF REDUCING PARTICLE SIZE AND INCREASING UNIFORMITY OF PARTICLES IN A COLLOIDAL SUSPENSION, METHOD OF MANUFACTURING CIRCUITS, AND FILTER HAVING AN INPUT AND AN OUTPUT |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-167706 | LOW NOISE AMPLIFIER HAVING BYPASS CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-168629 | UV CURE PROCESS AND TOOL FOR LOW K FILM FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-168795 | SEMICONDUCTOR DEVICE ADHESIVE LAYER STRUCTURE AND PROCESS FOR FORMING STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-169132 | APPARATUS FOR REDUCING DC OFFSET IN A RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-169205 | SEMICONDUCTOR DEVICE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-170221 | WAFER PROCESSING EQUIPMENT AND METHOD FOR PROCESSING WAFERS |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-170815 | METHOD AND APPARATUS FOR TRANS FERRING DATA ON A SPLIT BUS IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-171846 | DUAL METAL GATE TRANSISTORS FOR CMOS PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-172262 | METHOD AND APPARATUS FOR ALIGNING A WAVEGUIDE TO A DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-172312 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND SEMICONDUCTOR COMPONENT THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-172595 | RADIO RECEIVER HAVING A DYNAMIC BANDWIDTH FILTER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-172642 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND SEMICONDUCTOR COMPONENT THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-172666 | SEMICONDUCTOR DEVICE AND PROCESS FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-172915 | ACOUSTIC WAVE FILTER AND METHOD OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-172944 | WAFER CARRIER AND METHOD OF MATERIAL REMOVAL FROM A SEMICONDUCTOR WAFER |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-172989 | SEMICONDUCTOR DEVICE AND A PROCESS FOR DESIGNING A MASK |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-173117 | METHOD FOR REMOVING ETCH RESIDUE RESULTING FROM A PROCESS FOR FORMING A VIA |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-173381 | LOAD CAPACITANCE COMPENSATED BUFFER AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-173716 | SEMICONDUCTOR DEVICE USING A BARRIER LAYER BETWEEN THE GATE ELECTRODE AND SUBSTRATE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-174287 | PULSE WIDTH MODULATOR (PWM) SY STEM WITH LOW COST DEAD TIME D ISTORTION CORRECTION |
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| FREESCALE SEMICONDUCTOR, INC. | TW | NI-174598 | SEMICONDUCTOR DEVICE AND A PROCESS FOR FORMING |
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| FREESCALE SEMICONDUCTOR, INC. | TW | NI-174330 NI-175171 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-176549 | MULTI-LAYER REGISTRATION CONTROL FOR PHOTOLITHOGRAPHY PROCESSES |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-177137 | METHOD AND APPARATUS FOR MAKING AN INTEGRATED CIRCUIT USING POLARIZATION PROPERTIES OF LIGHT |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-177785 | DATA PROCESSING SYSTEM HAVING AN ON-CHIP BACKGROUND DEBUG SYSTEM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-178565 | A DEVICE AND METHOD FOR PERFORMING STACK POP AND PUSH OPERATIONS IN A PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-178579 | FILTERING DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-178696 | METHOD AND APPARATUS FOR MEASURING A POLISHING CONDITION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-178698 | SWITCHABLE AND TUNABLE COPANAR WAVEGUIDE FILTERS |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-179975 | MULTILAYERED TAPERED TRANSMISSION LINE, DEVICE AND METHOD FOR MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-179980 | LITHOGRAPHIC TEMPLATE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-180559 | OPTICAL DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-181000 | INTEGRATION OF TWO MEMORY TYPES ON THE SAME INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-181004 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-181759 | BONDING PAD |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-183667 | METHOD FOR CHEMICAL MECHANICAL POLISHING (CMP) WITH ALTERING THE CONCENTRATION OF OXIDIZING AGENT IN SLURRY |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-184223 | SELECTIVE METAL OXIDE REMOVAL |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-185009 | LITHOGRAPHY METHOD FOR FORMING SEMICONDUCTOR DEVICES ON A WAFER AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-185878 | EEPROM CIRCUIT, VOLTAGE REFERENCE CIRCUIT AND METHOD FOR PROVIDING A LOW TEMPERATURE-COEFFICIENT VOLTAGE REFERENCE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-186525 | AN OPTO-COUPLING DEVICE STRUCTURE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-186739 | METHOD OF PREPARING CRYSTALLIN E ALKALINE EARTH METAL OXIDES ON A SI SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-187103 | PACKAGE FOR ELECTRONIC COMPONENTS AND METHOD FOR FORMING A PACKAGE FOR ELECTRONIC COMPONENTS. |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-187839 | ELECTRO-OPTIC STRUCTURE AND PROCESS FOR FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-187927 | SEMICONDUCTOR DEVICE AND A METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-188177 | METHOD OF PREPARING COPPER METALLIZATION DIE FOR WIRE BONDING |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-188784 | ENHANCED CERAMIC LAYERS FOR LAMINATED CERAMIC DEVICES AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-188790 | PROCESS FOR MAKING A MIM CAPACITOR |

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| FREESCALE SEMICONDUCTOR, INC. | TW | NI-189402 | METHOD OF FORMING A PATTERN ON A SEMICONDUCTOR WAFER USING AN ATTENUATED PHASE SHIFTING REFLECTIVE MASK |
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| FREESCALE SEMICONDUCTOR, INC. | TW | NI-189406 | METHOD OF FORMING A BOND PAD AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-190060 | HIGH FREQUENCY SIGNAL ISOLATION IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-190158 | STRUCTURE AND METHOD FOR FABRICATING EPITAXIAL SEMICONDUCTOR ON INSULATOR (SOI) STRUCTURES AND DEVICES UTILIZING THE FORMATION OF A COMPLIANT SUBSTRATE FOR MATERIALS USED TO FORM SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-190461 | FLEXIBLE INTERRUPT CONTROLLER THAT INCLUDES AN INTERRUPT FORCE REGISTER |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-190529 | SEMICONDUCTOR DEVICE HAVING A BALL GRID ARRAY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-191727 | A CHEMICAL MECHANICAL POLISHING (CMP) SLURRY FOR COPPER AND METHOD OF USE IN INTEGRATED CIRCUIT MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-191819 | DATA PROCESSING SYSTEM HAVING AN ADAPTIVE PRIORITY CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-191828 | MULTI-RATE ANALOG-TO-DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-192420 | METHOD AND APPARATUS FOR A CLOCK CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-192594 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-193059 | PROCESSOR HAVING SELECTIVE BRANCH PREDICTION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-193106 | RECORDING OF RESULT INFORMATION IN A BUILT-IN SELF- TEST CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-193220 | LITHOGRAPHIC TEMPLATE AND METHOD OF FORMATION AND USE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-193323 | INCREMENTAL-DELTA ANALOGUE-TO-DIGITAL CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-193848 | LOW-PRESSURE LAMINATED CERAMIC DEVICES AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-195937 | COMMUNICATION CONTROLLER AND METHOD OF TRANSFORMING |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-197324 | DISTRIBUTED AMPLIFIER HAVING SEPARATELY BIASED SECTIONS |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-197367 | PACKAGED SEMICONDUCTOR WITH MULTIPLE ROWS OF BOND PADS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-198820 | VARIABLE GAIN AMPLIFIER WITH AUTOBIASING SUPPLY REGULATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-199509 | METHOD AND APPARATUS FOR COMBINING A WIRELESS RECEIVER AND A NON-WIRELESS RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-199535 | AN INTEGRATED CIRCUIT USING A REFLECTIVE MASK |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-200639 | SWITCH ASSEMBLY AND METHOD OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-202306 | DEVICE AND METHOD FOR PERFORMING HIGH-SPEED LOW OVERHEAD CONTEXT SWITCH |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-204569 | ARRANGEMENT AND METHOD FOR IMPEDANCE MATCHING |

| FREESCALE SEMICONDUCTOR, INC. | TW | NI-204631 | METHOD OF MODIFYING THE TEMPERATURE STABILITY OF A LOW TEMPERATURE COFIRED CERAMICS (LTCC) |
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| FREESCALE SEMICONDUCTOR, INC. | TW | NI-204666 | MULTIPHASE VOLTAGE CONTROLLED OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-222193 | STACKED DIE SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-71387 | DATA PROCESSOR WITH TRANSPAREN T OPERATION DURING A BACKGROUN D MODE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | NI-74861 | A SEMICONDUCTOR DEVICE HAVING NO DIE SUPPORTING SURFACE AND METHOD FOR MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | DE | P69404789.9 | PROCESS FOR FORMING TIN- BISMUTH SOLDER CONNECTION HAVING IMPROVED HIGH TEMPERATURE PROPERTIES |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00103662.9 | INTEGRATED CIRCUIT MEMORY HAVI NG A FUSE DETECT CIRCUIT AND M ETHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00103663.7 | METHOD FOR FORMING A BARRIER L AYER FOR USE IN A COPPER INTER CONNECT |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00108203.5 | METHOD OF FORMING A COPPER LAY ER OVER A SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00120186.7 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00120254.5 | METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE INCLUDING A METAL OXIDE INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00120260.X | METHOD FOR FABRICATING A SEMIC ONDUCTOR STRUCTURE HAVING A CR YSTALLINE ALKALINE EARTH METAL OXIDE INTERFACE WITH SILICON |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00121974.X | MEMORY UTILIZING A PROGRAMMABLE DELAY TO CONTROL ADDRESS BUFFERS |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00129033.9 | FILTER APPARATUS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00130960.9 | METHOD AND APPARATUS FOR CONFIGURING A DATA PROCESSING SYSTEM AFTER RESET |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00130967.6 | MECHANICALLY ROBUST PAD INTERFACE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00131408.4 | INTEGRATED CIRCUIT HVING A BALANCED TWIST FOR DIFFERENTIAL SIGNAL LINES |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00131624.9 | METHOD AND APPARATUS FOR A CALIBRATED FREQUENCY MODULATION PHASE LOCKED LOOP |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00132938.3 | INTEGRATED FILTER WITH IMPROVED I/O MATCHING AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00132939.1 | LINEAR CAPACITOR STRUCTURE IN A CMOS PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00134286.X | LOW PROFILE INTERCONNECT STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00135490.6 | SEMICONDUCTOR DEVICE, A PROCESS FOR A SEMICONDUCTOR DEVICE, AND A PROCESS FOR MAKING A MASKING DATABASE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00135554.6 | PEAK PROGRAM CURRENT REDUCTION APPARATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00136603.3 | METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE HAVING A STABLE CRYSTALLINE INTERFACE WITH SILICON |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00137087.1 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE |
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| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00137090.1 | SEMICONDUCTOR DEVICE AND A PROCESS FOR FORMING THE SEMICONDUCTOR DEVICE |
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| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00137568.7 | VOLTAGE VARIABLE CAPACITOR WITH IMPROVED C-V LINEARITY |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00809472.1 | APPARATUS FOR RECEIVING AND PROCESSING A RADIO FREQUENCY SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL00811015.8 | SEMICONDUCTOR DEVICE AND A PROCESS FOR DESIGNING A MASK |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01101251.X | DEVICE AND METHOD FOR PERFORMING HIGH-SPEED LOW OVERHEAD CONTEXT SWITCH |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01101649.3 | PROCESS FOR FORMING A SEMICONDUCTOR DEVICE AND A CONDUCTIVE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01101691.4 | FLEXIBLE INTERRUPT CONTROLLER THAT INCLUDES AN INTERRUPT FORCE REGISTER |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01101738.4 | UV CURE PROCESS AND TOOL FOR LOW K FILM FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01101739.2 | METHOD AND APPARATUS FOR ALIGNING A WAVEGUIDE TO A DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01101744.9 | METHOD AND APPARATUS FOR TESTING AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01103095.X | REAL-TIME PROCESSOR DEBUG SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01805820.5 | SEMICONDUCTOR DEVICE AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01807539.8 | METHOD OF MANUFACTURING A HETEROJUNCTION BICMOS INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01807873.7 | ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01808215.7 | LOAD CAPACITANCE COMPENSATED BUFFER AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01808345.5 | METHOD AND APPARATUS FOR MANUFACTURING AN INTERCONNECT STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01808675.6 | SINGLE SUPPLY HFET WITH TEMPERATURE COMPENSATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01811029.0 | DUAL METAL GATE TRANSISTORS FOR CMOS PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01811030.4 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND SEMICONDUCTOR COMPONENT THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01811410.5 | ULTRA-LATE PROGRAMMING ROM AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01811420.2 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND CHEMICAL-MECHANICAL POLISHING SYSTEM THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01813676.1 | METHOD AND APPARATUS FOR DETECTING AND COMPENSATING DIGITAL LOSSES IN A COMMUNICATIONS NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01813798.9 | FREQUENCY MODULATOR USING A WAVEFORM GENERATOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01814061.0 | ELECTRONIC COMPONENT AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01814495.0 | SEMICONDUCTOR DEVICE HAVING PASSIVE ELEMENTS AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01815204.X | METHOD FOR UNIFORM POLISH IN MICROELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01816323.8 | SEMICONDUCTOR DEVICE AND PROCESS FOR FORMING THE |

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| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01816363.7 | ELECTRO-OPTIC STRUCTURE AND PROCESS FOR FABRICATING SAME |
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| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01816887.6 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND SEMICONDUCTOR COMPONENT THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01816888.4 | MICROMACHINED COMPONENT AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01818248.8 | AMORPHOUS CARBON LAYER FOR IMPROVED ADHESION OF PHOTORESIST |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01818663.7 | APPARATUS FOR RECEIVING AND RECOVERING FREQUENCY SHIFT KEYED SYMBOLS |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01819699.3 | LOW PROFILE INTEGRATED MODULE INTERCONNECTS |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01822934.4 | HIGH K DIELECTRIC FILM AND METHOD FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL01822989.1 | METHOD AND DEVICE FOR CREATING AND USING PRE- INTERNALIZED PROGRAM FILES |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02142437.3 | HIGH K DIELECTRIC FILM AND METHOD FOR MAKING |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02804141.0 | MULTILAYERED TAPERED TRANSMISSION LINE AND DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02805615.9 | ARRANGEMENT AND METHOD FOR IMPEDANCE MATCHING |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02806573.5 | DISTRIBUTED AMPLIFIER HAVING SEPARATELY BIASED SECTIONS |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02806953.6 | LITHOGRAPHIC TEMPLATE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02809126.4 | SEMICONDUCTOR DEVICE AND A METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02809264.3 | METHOD OF FORMING AN INTEGRATED CIRCUIT DEVICE USING DUMMY FEATURES AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02809265.1 | METHOD AND APPARATUS FOR A CLOCK CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02809266.X | AN OPTO-COUPLING DEVICE STRUCTURE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02809465.4 | SYSTEM AND METHOD FOR CONTROLLING BUS ARBITRATION DURING CACHE MEMORY BURST CYCLES |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02809967.2 | FIRST-IN FIRST-OUT MEMORY SYSTEM AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02810199.5 | INTEGRATION OF TWO MEMORY TYPES ON THE SAME INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02812759.5 | LOW LEAKAGE LOCAL OSCILLATOR SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02814146.6 | SEMICONDUCTOR DEVICE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02814531.3 | SELECTIVE METAL OXIDE REMOVAL |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02817383.X | LOW POWER CYCLIC A/D CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02817666.9 | MODE CONTROLLER FOR SIGNAL ACQUISITION AND TRACKING IN AN ULTRA WIDEBAND COMMUNICATIONS SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02817807.6 | DATA PROCESSING SYSTEM HAVING AN ADAPTIVE PRIORITY CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02817825.4 | METHOD OF FORMING A BOND PAD AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02819141.2 | PACKAGED SEMICONDUCTOR WITH MULTIPLE ROWS OF BOND PADS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02819470.5 | MULTIPHASE VOLTAGE CONTROLLED OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02819474.8 | DUAL STEERED FREQUENCY SYNTHESIZER |
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| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02821860.4 | INCREMENTAL-DELTA ANALOGUE-TO-DIGITAL CONVERSION |
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| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02021000.4 ZL02822574.0 | METHOD OF OPERATING A MEDIA ACCESS CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02823290.9 | VARIABLE GAIN AMPLIFIER WITH AUTOBIASING SUPPLY |
| | | | REGULATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02823661.0 | TRANSISTOR METAL GATE STRUCTURE THAT MINIMIZES NON-PLANARITY EFFECTS AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02823683.1 | SEMICONDUCTOR POWER DEVICE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02824143.6 | HIGH FREQUENCY SIGNAL ISOLATION IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02824529.6 | SEMICONDUCTOR PACKAGE DEVICE AND METHOD OF FORMATION AND TESTING |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02826499.1 | METHOD AND APPARATUS FOR INTERFACING A PROCESSOR TO A COPROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02826984.5 | ENABLE PROPAGATION CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02827107.6 | SYSTEM AND METHOD OF COMMUNICATION BETWEEN MULTIPLE POINT-COORDINATED WIRELESS NETWORKS |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02827246.3 | METHOD OF BONDING AND TRANSFERRING A MATERIAL TO FORM A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02827378.8 | METHOD AND APPARATUS FOR DETECTING A STALL CONDITION IN A STEPPING MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02827387.7 | A CHEMISTRY FOR ETCHING QUATERNARY INTERFACE LAYERS ON InGaAsP MOSTLY FORMED BETWEEN GaAs AND InxGa(1-x) P LAYERS |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02827682.5 | ARTICLE COMPRISING AN OXIDE LAYER ON A GaAs-BASED SEMICONDUCTOR STRUCTURE AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL02827843.7 | WIRE BOND-LESS ELECTRONIC COMPONENT FOR USE WITH AN EXTERNAL CIRCUIT AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03102312.6 | PACKAGED SEMICONDUCTOR DEVICE AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03105167.7 | METHOD OF ATTACHING A DIE TO A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03155383.4 | TONE DETECTOR AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03801606.0 | METHOD OF FORMING NANOCRYSTALS IN A MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03801610.9 | SIMPLIFICATION OF BALL ATTACH METHOD USING SUPER- SATURATED FINE CRYSTAL FLUX |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03801747.4 | ELECTRONIC DISCHARGE PROTECTION CIRCUITRY AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03803385.2 | CONVERSION BETWEEN OPTICAL AND RADIO FREQUENCY SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03804117.0 | LOW DROP-OUT VOLTAGE REGULATOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03804521.4 | SEMICONDUCTOR DEVICE HAVING A WIRE BOND PAD AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03804808.6 | STACKED DIE SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03804813.2 | HIGH FREQUENCY SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03804956.2 | INTEGRATED CIRCUIT SECURITY AND METHOD THEREFOR |

CN ZL03805269.5 MULTI-ROW LEADFRAME

FREESCALE SEMICONDUCTOR, INC.

| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03805770.0 | SEMICONDUCTOR DEVICE HAVING A BOND PAD AND METHOD THEREFOR |
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| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03806213.5 | SYSTEM AND METHOD FOR HANDLING ASYNCHRONOUS DATA IN A WIRELESS NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03806299.2 | INTEGRATED CIRCUIT DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03807696.9 | METHOD AND ARRANGEMENT FOR VIRTUAL DIRECT MEMORY ACCESS |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03809405.3 | INSTRUCTION CACHE AND METHOD FOR REDUCING MEMORY CONFLICTS |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03809591.2 | SIGMA-DELTA ANALOG-TO-DIGITAL CONVERTER AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03809935.7 | METHOD AND APPARATUS FOR SECURE SCAN TESTING |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03810166.1 | MONOCRYSTALLINE OXIDE HAVING A SEMICONDUCTOR DEVICE THEREON |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03810494.6 | MULTIPLE THICKNESS SEMICONDUCTOR INTERCONNECT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03812402.5 | METHOD AND APPARATUS FOR AFFECTING A PORTION OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03812624.9 | DATA PROCESSING SYSTEM HAVING MULTIPLE REGISTER CONTEXTS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03814088.8 | METHOD AND APPARATUS FOR SOFT DEFECT DETECTION IN A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03814162.0 | MULTI-TIERED LITHOGRAPHIC TEMPLATE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03814608.8 | LOW DROP-OUT VOLTAGE REGULATOR AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03815344.0 | SENSE AMPLIFIER FOR A MEMORY HAVING AT LEAST TWO DISTINCT RESISTANCE STATES |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03817594.0 | LITHOGRAPHIC TEMPLATE HAVING A REPAIRED GAP DEFECT |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03817780.3 | COMMUNICATION SYSTEM AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03818587.3 | HYBRID STRUCTURE FOR DISTRIBUTED POWER AMPLIFIERS |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03818840.6 | RADIO RECEIVER WITH VARIABLE BANDWIDTH IF FILTER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03819789.8 | CLOSED LOOP CURRENT CONTROL CIRCUIT AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03820615.3 | DIELECTRIC STORAGE MEMORY CELL HAVING HIGH PERMITTIVITY TOP DIELECTRIC AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03820973.X | OSCILLATOR CIRCUIT HAVING REDUCED LAYOUT AREA AND LOWER POWER SUPPLY TRANSIENTS |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03821451.2 | SEMICONDUCTOR DEVICE EXHIBITING ENHANCED PATTERN RECOGNITION WHEN ILLUMINATED IN A MACHINE VISION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03821452.0 | WAFER COATING AND SINGULATION METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03822968.4 | METHOD AND CIRCUITRY FOR IDENTIFYING WEAK BITS IN AN MRAM |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03822969.2 | CURRENT-CARRYING ELECTRONIC COMPONENT AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL03822971.4 | FULL BRIDGE INTEGRAL NOISE SHAPING FOR QUANTIZATION |

OF PULSE WIDTH MODULATION SIGNALS

| FREESCALE SEMICONDUCTOR, INC. | CN ZL03824003.3 | NON-VOLATILE MEMORY DEVICE AND METHOD FOR FORMING |
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| FREESCALE SEMICONDUCTOR, INC. | CN ZL03824015.7 | METHOD FOR ELIMINATING VOIDING IN PLATED SOLDER |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL03824279.6 | APPARATUS AND METHOD FOR POWER MANAGEMENT IN A TIRE PRESSURE MONITORING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL03824815.8 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL03824916.2 | ONE TRANSISTOR DRAM CELL STRUCTURE AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL03825020.9 | LOW VOLTAGE DETECTION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL03825140.X | METHOD AND APPARATUS FOR PROCESSING AN AMPLITUDE MODULATED (AM) SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL03825435.2 | THIN GAAS WITH COPPER BACK-METAL STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL03825611.8 | MINIATURE MOLDLOCKS FOR HEATSINK OR FLAG FOR AN OVERMOLDED PLASTIC PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL03825687.8 | METHOD FOR FORMING A PASSIVATION LAYER FOR AIR GAP FORMATION AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL03825818.8 | POWER MANAGEMENT SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL200680056096.7 | IMAGE PROCESSING APPARATUS AND METHOD OF TRANSFERRING IMAGE DATA |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL201220524796.7 | SEMICONDUCTOR DEVICE PACKAGE WITH CAP ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL94103949.8 | SEMICONDUCTOR DEVICE HAVING X- SHAPED DIE SUPPORT MEMBER AND METHOD FOR MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL94106509.X | SEMICONDUCTOR DEVICE HAVING A REDUCING/OXIDIZING CONDUCTIVE MATERIAL AND A PROCESS FOR FOR MING THE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL95105174.1 | FREQUENCY INVERSION SCRAMBLER WITH INTEGRATED HIGH-PASS FILT ER |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL95106587.4 | III-V SEMICONDUCTOR STRUCTURE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL95118705.8 | CHEMICAL—MECHANICAL POLISHER AND A PROCESS FOR POLISHING |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL95119287.6 | ADJUSTABLE DEPTH/WIDTH FIFO BU FFER FOR VARIABLE WIDTH DATA T RANSFERS |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL95120270.7 | MULTI-STRAND SUBSTRATE FOR BAL L-GRID ARRAY ASSEMBLIES AND ME THOD |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL96105117.5 | METHOD FOR REDUCING POWER CONS UMPTION IN A PORTABLE ELECTRON IC DEVICE WITH A LIQUID CRYSTA L DISPLAY SCREEN |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL96105466.2 | MONOLITHIC HIGH FREQUENCY INTE GRATED CIRCUIT STRUCTURE AND M ETHOD OF MANUFACTURING THE SAM E |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL96105893.5 | DATA PROCESSING SYSTEM HAVING A MULTI-FUNCTION SCALABLE PARA LLEL INPUT/OUTPUT PORT |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL97100387.4 | METHOD FOR MAKING AN ELECTRONI C COMPONENT HAVING AN ORGANIC SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | CN ZL97102640.8 | METHOD AND APPARATUS FOR ACCES SING A CHIP- |

SELECTABLE DEVICE IN A DATA PROCESSING SYSTEM

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| FREESCALE SEMICONDUCTOR, INC. | CN | ZL97110996.6 | BIPOLAR TRANSISTOR AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL97114012.X | CURRENT LIMIT CONTROLLER FOR A N AIR BAG DEPLOYMENT SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL97115320.5 | BALUN TRANSFORMER |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL97117646.9 | MEMORY SUITABLE FOR OPERATION AT LOW POWER SUPPLY VOLTAGES A ND SENSE AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL97120501.9 | METHOD FOR TRANSMITTING SIGNAL S BETWEEN A MICROPORCESSOR AND AN INTERFACE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL98100996.4 | PACKAGING APPARATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL98103715.1 | SELECTIVELY FILLED ADHESIVE FILM CONTAINING A FLUXING AGENT |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL98105911.2 | METHOD FOR DEPOSITING A DIFFUSION BARRIER |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL98106329.2 | PULSE WIDTH MODULATOR (PWM) SY STEM WITH LOW COST DEAD TIME D ISTORTION CORRECTION |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL98108369.2 | PROCESS FOR DEPOSITING A LAYER OF MATERIAL ON A SUBSTRATE AN D A PLATING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL98115555.3 | POINT OF USE DILUTION TOOL AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL98116658.X | SEMICONDUCTOR DEVICE AND METHOD FOR MAKING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL98118373.5 | METHOD AND APPARATUS FOR PROCE SSING A SEMICONDUCTOR WAFER ON A ROBOTIC TRACK HAVING ACCESS TO IN SITU WAFER BACKSIDE PAR TICLE DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL98118581.9 | METHOD AND APPARATUS FOR INTER FACING A PROCESSOR TO A COPROC ESSOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL98120987.4 | A CHEMICAL MECHANICAL POLISHING (CMP) SLURRY FOR COPPER AND METHOD OF USE IN INTEGRATED CIRCUIT MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL98121455.X | METHOD AND APPARATUS FOR AFFEC TING SUBSEQUENT INSTRUCTION PR OCESSING IN A DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL98122812.7 | SEMICONDUCTOR DEVICE HAVING A SUB-CHIP-SCALE PACKAGE STRUCTU RE AND METHOD FOR FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL98123223.X | SEMICONDUCTOR DEVICE MEMORY CE LL, AND PROCESSES FOR FORMING THEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL98801278.2 | PORTABLE ELECTRONIC DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL98812928.0 | SWITCHED CAPACITOR CIRCUIT AND METHOD FOR REDUCING SAMPLING NOISE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL99101606.8 | METHOD FOR FORMING INTERCONNEC T BUMPS ON A SEMICONDUCTOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL99104896.2 | SYNCHRONOUS PIPELINED BURST ME MORY AND METHOD FOR OPERATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL99105292.7 | SEMICONDUCTOR DEVICE FOR SUBST RATE TRIGGERED ELECTROSTATIC D ISCHARGE PROTECTION AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL99108648.1 | DATA PROCESSING SYSTEM HAVING BRANCH CONTROL AND METHOD THER EOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL99108672.4 | PIPELINED DUAL PORT INTEGRATED CIRCUIT MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL99108904.9 | METHOD FOR FORMING A SEMICONDU CTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL99110023.9 | CMOS SEMICONDUCTOR DEVICES AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL99110164.2 | METHOD AND APPARATUS FOR TRANS FERRING DATA OVER A PROCESSOR INTERFACE BUS |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL99110621.0 | METHOD FOR FORMING A SEMICONDU CTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL99111910.X | METHOD AND APPARATUS FOR TRANS FERRING DATA ON A SPLIT BUS IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL99120977.X | CIRCUIT AND METHOD FOR REDUCIN G PARASITIC BIPOLAR EFFECTS DU RING ELECTROSTATIC DISCHARGES |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL99123118.X | PROGRAMMABLE DELAY CONTROL IN A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL99126715.X | A MEMORY DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL99806733.4 | POWER AMPLIFIER OUTPUT MODULE FOR DUAL-MODE DIGITAL SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL99808006.3 | DIGITAL COMMUNICATONS PROCESSOR |

$\label{lem:conductor} Free scale\ Semiconductor,\ Inc.-Patent\ Applications;\ For eign$

| <u>Owner</u> | Country | Application # | Description |
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| FREESCALE SEMICONDUCTOR, INC. | BR | 1020120122332 | CHARGE PUMP CIRCUIT WITH FAST START-UP |
| FREESCALE SEMICONDUCTOR, INC. | BR | 1020120320304 | TOUCH SENSE INTERFACE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | BR | 1020130023531 | MEMS DEVICE ASSEMBLY AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | BR | 1020130135666 | METHODS AND STRUCTURES FOR REDUCING HEAT EXPOSURE OF THERMALLY SENSITIVE SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | BR | 1020130146790 | VRS INTERFACE WITH 1/T ARMING FUNCTION |
| FREESCALE SEMICONDUCTOR, INC. | BR | 1020130221449 | QUIESCENT CURRENT DETERMINATION USING IN- PACKAGE VOLTAGE MEASUREMENTS |
| FREESCALE SEMICONDUCTOR, INC. | BR | 1120120005952 | RECEIVER WITH AUTOMATIC GAIN CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | BR | 1120120120921 | SYSTEMS AND METHODS FOR DELIVERING POWER IN RESPONSE TO A CONNECTION EVENT |
| FREESCALE SEMICONDUCTOR, INC. | BR | 0917905-4 | MEMORY DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | BR | 0918467-8 | INTEGRATED CIRCUIT HAVING BOOSTED ARRAY VOLTAGE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | BR | PCT/US2009/038853 | TOUCH SCREEN DETECTION AND DIAGNOSTICS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580025802.7 | SYSTEM AND METHOD FOR THE MITIGATION OF SPECTRAL LINES IN AN ULTRAWIDE BANDWIDTH TRANSCEIVER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200580034723.2 | WORD LINE DRIVER CIRCUIT FOR A STATIC RANDOM ACCESS MEMORY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200710105012.0 | LEAD FRAME FOR SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780006671.7 | METHOD AND APPARATUS FOR INDICATING DIRECTIONALITY IN INTEGRATED CIRCUIT MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780007004.0 | NON-VOLATILE MEMORY HAVING A MULTIPLE BLOCK ERASE MODE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780045980.5 | SELECTIVE GUARDED MEMORY ACCESS ON A PERINSTRUCTION BASIS |

| FREESCALE SEMICONDUCTOR, INC. | CN | 200780052492.7 | IMPROVEMENTS IN OR RELATING TO DIAGNOSTICS OF A CAPACITIVE SENSOR |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 200780052697.5 | CIRCUIT, INTEGRATED CIRCUIT AND METHOD FOR DISSIPATING HEAT FROM AN INDUCTIVE LOAD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780052758.8 | INTEGRATED CIRCUIT, ELECTRONIC DEVICE AND ESD PROTECTION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200780101320.4 | MRAM TESTING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200810144567.0 | DATA PROCESSING SYSTEM IMPLEMENTING SIMD OPERATIONS AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200810168145.7 | NEW GATE DRIVE METHOD FOR H BRIDGE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200810173862.9 | A PASSIVE CANCELLATION METHOD OF SUBSTRATE NOISE FOR BUCK CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200810179793.2 | METHOD FOR FAST TRACKING AND JITTER IMPROVEMENT IN ASYNCHRONOUR SAMPLE RATE CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880006470.1 | SOURCE/DRAIN STRESSOR AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880006522.5 | MICROELECTRONIC ASSEMBLY WITH IMPROVED ISOLATION VOLTAGE PERFORMANCE AND A METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880015444.5 | THREAD DE-EMPHASIS INSTRUCTION FOR MULTITHREADED PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880106121.7 | SEMICONDUCTOR DEVICE TEST SYSTEM HAVING REDUCED CURRENT LEAKAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880109055.9 | PHASE CHANGE MEMORY STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880130594 | DIE TEMPERATURE ESTIMATOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880131910.6 | CHARGE AMPLIFIERS WITH DC STABILIZATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200880132060.1 | TRANSISTOR POWER SWITCH DEVICE RESISTANT AGAINST REPETITIVE AVALANCHE BREAKDOWN |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200910007747.9 | HIGH FREQUENCY POWER SWITCHING CIRCUIT WITH ADJUSTABLE DRIVE CURRENT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200910140565.9 | LEAD FRAME FOR SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200910142600 | SUB-THRESHOLD CMOS TEMPERATURE DETECTOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200910149320.2 | METHOD FOR ASSEMBLING STACKABLE SEMICONDUCTOR PACKAGES |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200910159553.0 | METHOD OF FORMING WIRE BONDS IN SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980103655.9 | PERIPHERAL MODULE REGISTER ACCESS METHODS AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980104243 | ANALOG-TO-DIGITAL CONVERTER WITH VARIABLE GAIN AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980106158.4 | QUALIFICATION OF CONDITIONAL DEBUG INSTRUCTIONS BASED ON ADDRESS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980115765.7 | CACHE COHERENCY PROTOCOL IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980118853.2 | CIRCUIT FOR AND AN ELECTRONIC DEVICE INCLUDING A NONVOLATILE MEMORY CELL AND A PROCESS OF FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980120007.4 | UTILIZATION OF A STORE BUFFER FOR ERROR RECOVERY ON A STORE ALLOCATION CACHE MISS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980128467.1 | SYSTEM AND METHOD FOR POWER MANAGEMENT |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 200980129456.5 | BRANCH TARGET BUFFER ALLOCATION |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 200980129750.6 | SEMICONDUCTOR DEVICES WITH EXTENDED ACTIVE REGIONS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980130621.9 | BALUN SIGNAL TRANSFORMER AND METHOD OF FORMING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980131904.5 | PROVISION OF EXTENDED ADDRESSING MODES IN A SINGLE INSTRUCTION MULTIPLE DATA (SIMD) DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980132364.2 | DEBUG INSTRUCTION FOR USE IN A MULTI-THREADED DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980132486.1 | DEBUG MESSAGE GENERATION USING A SELECTED ADDRESS TYPE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980133071.6 | MEMORY DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980134809.0 | CIRCUIT AND METHOD FOR OPTIMIZING MEMORY SENSE AMPLIFIER TIMING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980134821.1 | ADAPTIVE FEEDBACK AND POWER CONTROL FOR USB DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980136772.5 | INTEGRATED CIRCUIT HAVING BOOSTED ARRAY VOLTAGE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980138708.0 | DATA CONVERSION CIRCUITRY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980143207.1 | PERMISSIONS CHECKING FOR DATA PROCESSING INSTRUCTIONS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980143516.9 | TRANSDUCER WITH DECOUPLED SENSING IN MUTUALLY ORTHOGONAL DIRECTIONS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980146148.3 | PROGRAMMABLE ERROR ACTIONS FOR A CACHE IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980148071.3 | TOUCH SENSOR PANEL USING REGIONAL AND LOCAL ELECTRODES TO INCREASE NUMBER OF SENSE LOCATIONS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980148878 | RF DEVICE AND METHOD WITH TRENCH UNDER BOND PAD FEATURE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980149473.5 | ERROR DETECTION IN A MULTI-PROCESSOR DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980150738.3 | MICROELECTROMECHANICAL DEVICE WITH ISOLATED MICROSTRUCTURES AND METHOD OF PRODUCING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980151877.8 | LED DRIVER WITH FEEDBACK CALIBRATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980153654.5 | DETERMINING INITIAL ROTOR POSITION OF AN ALTERNATING CURRENT MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980154030.5 | METHOD OF FORMING A SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980154760.5 | SEMICONDUCTOR STRUCTURE, AN INTEGRATED CIRCUIT INCLUDING A SEMICONDUCTOR STRUCTURE AND A METHOD FOR MANUFACTURING A SEMICONDUCTOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980154951.1 | PACKAGE ASSEMBLY AND METHOD OF TUNING A NATURAL RESONANT FREQUENCY OF A PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980154952.6 | RADIO FREQUENCY REMOTE CONTROLLER DEVICE, INTEGRATED CIRCUIT AND METHOD FOR SELECTING AT LEAST ONE DEVICE TO BE CONTROLLED |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980155477.4 | RECEIVING NODE IN A PACKET COMMUNICATIONS SYSTEM AND METHOD FOR MANAGING A BUFFER IN A RECEIVING NODE IN A PACKET COMMUNICATIONS SYSTEM |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 200980155611.0 | PROCESSING DATA FLOWS |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 200980158627 | A METHOD AND SYSTEM ARRANGED FOR FILTERING AN IMAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980159203.2 | TONE RELAY SYSTEM AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980159464.4 | TOUCH-SCREEN INTERFACE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980159468.2 | BATTERY CHARGING CIRCUIT AND ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980159640.4 | MULTICHANNEL RECEIVER SYSTEM AND METHOD FOR MULTICHANNEL RECEIVER MONITORING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980159641.9 | INTEGRATED CIRCUIT WITH CHANNEL ESTIMATION MODULE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980160430.7 | TRANSISTOR POWER SWITCH DEVICE AND METHOD OF MEASURING ITS CHARACTERISTICS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980160433.0 | DATA ADMINISTRATION UNIT, DATA ACCESS UNIT, NETWORK ELEMENT, NETWORK, AND METHOD FOR UPDATING A DATA STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980160434.5 | CONTROLLER SYSTEM, INTEGRATED CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980160482.4 | INTEGRATED CIRCUIT COMPRISING VOLTAGE MODULATION CIRCUITRY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980160483.9 | DIVERSITY ANTENNA SYSTEM AND TRANSMISSION METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980160519.3 | DUTY CYCLE CORRECTOR AND DUTY CYCLE CORRECTION METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980160573.8 | SIGNAL PROCESSING SYSTEM, INTEGRATED CIRCUIT COMPRISING BUFFER CONTROL LOGIC AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980162321.9 | CONFERENCE CALL SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980162323.8 | RESPONSE TO WEAROUT IN AN ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980162392.9 | ADVANCED COMMUNICATION CONTROLLER UNIT AND METHOD FOR RECORDING PROTOCOL EVENTS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980162501.7 | PUMP SYSTEM AND MOTORIZED VEHICLE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980162502.1 | VERTICAL POWER TRANSISTOR DEVICE, SEMICONDUCTOR DIE AND METHOD OF MANUFACTURING A VERTICAL POWER TRANSISTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980162615.1 | RECEIVER AND METHOD FOR EQUALIZING SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980162659.4 | BYPASS CAPACITOR CIRCUIT AND METHOD OF PROVIDING A BYPASS CAPACITANCE FOR AN INTEGRATED CIRCUIT DIE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201010004666.6 | DUAL DIE SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201010113690.3 | METHOD FOR MAKING SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201010116814.3 | LEAD FRAME SHEET |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201010139991.3 | METHOD FOR DETECTING AUDIO SIGNAL TRANSIENT AND TIME-SCALE MODIFICATION BASED ON SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201010141754.0 | METHOD OF MAKING SEMICONDUCTOR PACKAGE WITH IMPROVED STANDOFF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201010147513.7 | LEAD FRAME FOR SEMICONDUCTOR DEVICE |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 201010192111.9 | STEPPER MOTOR CONTROLLER AND METHOD FOR CONTROLLING THE SAME |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 201010213286.3 | METHOD AND APPARATUS FOR DC-TO-DC CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201010213923.7 | THIN SEMICONDUCTOR PACKAGE AND METHOD FOR MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201010222612.7 | METHOD AND SYSTEM FOR TOUCH SENSOR INTERACE FAULT DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201010236800.5 | METHOD OF ASSEMBLING INTEGRATED CIRCUIT DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201010255738.4 | SEMICONDUCTOR DEVICE WITH NESTED ROWS OF CONTACTS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201010292924.5 | BRACE FOR WIRE BOND |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201010297545.5 | METHOD OF TESTING D/A AND A/D CONVERTERS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201010601547.9 | PRESSURE SENSOR AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080004924.9 | INTEGRATED CIRCUIT COMPRISING FREQUENCY GENERATION CIRCUITRY FOR CONTROLLING A FREQUENCY SOURCE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080005033.5 | DUAL HIGH-K OXIDES WITH SIGE CHANNEL |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080005182.1 | SUBSTRATE BONDING WITH METAL GERMANIUM SILICON MATERIAL |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080005920.2 | CAPACITANCE-TO-VOLTAGE INTERFACE CIRCUIT, AND RELATED OPERATING METHODS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080006319.5 | AUTHENTICATED DEBUG ACCESS FOR FIELD RETURNS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080009241.2 | CONTINUOUS-TIME SIGMA-DELTA MODULATOR WITH MULTIPLE FEEDBACK PATHS HAVING INDEPENDENT DELAYS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080009454.5 | ANTIFUSE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080012403.8 | VERTICALLY INTEGRATED MEMS ACCELERATION TRANSDUCER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080013875.5 | EXPOSED PAD BACKSIDE PRESSURE SENSOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080014168.8 | PEAK DETECTION WITH DIGITAL CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080014331.0 | MEMORY TESTING WITH SNOOP CAPABILITIES IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080014872.3 | NEGATIVE VOLTAGE GENERATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080015511.0 | DEBUG SIGNALING IN A MULTIPLE PROCESSOR DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080016069.3 | THROUGH SUBSTRATE VIAS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080016420.9 | ADDRESS TRANSLATION TRACE MESSAGE GENERATION FOR DEBUG |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080020480.8 | METHOD TO CALIBRATE START VALUES FOR WRITE LEVELING IN A MEMORY SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080022230.8 | DEVICE WITH PROXIMITY DETECTION CAPABILITY |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080025282.0 | METHOD AND CIRCUIT FOR CHARGING AND DISCHARGING A CIRCUIT NODE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080025392.7 | PROCESSOR AND METHOD FOR DYNAMIC AND SELECTIVE ALTERATION OF ADDRESS TRANSLATION |
| EDEECCALE CELUCONDUCEOD TO | 07.7 | 201000021000 | DECEMBED LIVERY AND COMPACT |

CN 201080031009.9 RECEIVER WITH AUTOMATIC GAIN CONTROL

FREESCALE SEMICONDUCTOR, INC.

| FREESCALE SEMICONDUCTOR, INC. | CN 201080034626.4 PULSE WIDTH MODULATION FREQUENCY CONVERSION |
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| FREESCALE SEMICONDUCTOR, INC. | CN 201080038090.3 MEMS DEVICE WITH STRESS ISOLATION AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080038435.5 POWER TRANSISTOR WITH TURN OFF CONTROL AND METHOD FOR OPERATING |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080043105.5 SEMICONDUCTOR DEVICE WITH OXYGEN-DIFFUSION BARRIER LAYER AND METHOD FOR FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080043119.7 CAPACITIVE TOUCH SENSOR DEVICE CONFIGURATION SYSTEMS AND METHODS |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080043387.9 OPERATING AN EMULATED ELECTRICALLY ERASABLE (EEE) MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080047064.7 SEMICONDUCTOR WAFER HAVING SCRIBE LANE ALIGNMENT MARKS FOR REDUCING CRACK PROPAGATION |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080048571.2 ONE-TIME PROGRAMMABLE MEMORY DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080052492.9 METHODS AND APPARATUS FOR PERFORMING CAPACITIVE TOUCH SENSING AND PROXIMITY DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080052594.0 SYSTEMS AND METHODS FOR DELIVERING POWER IN RESPONSE TO A CONNECTION EVENT |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080056932.8 ELECTRICAL COUPLING OF WAFER STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080062117.2 CHIP DAMAGE DETECTION DEVICES FOR A SEMICONDUCTOR INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080062157.7 A NETWORK ELEMENT, TELECOMMUNICATION SYSTEM, INTEGRATED CIRCUIT AND A METHOD FOR PROVIDING A TELEPHONY CONNECTION |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080063511.8 BOND PAD WITH MULTIPLE LAYER OVER PAD METALLIZATION AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080064048.9 DETECTOR AND METHOD FOR DETECTING AN OSCILLATORY SIGNAL AMONG NOISE |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080065710.2 TOKEN BUCKET MANAGEMENT APPARATUS AND METHOD OF MANAGING A TOKEN BUCKET |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080065994.5 MULTI-CHANNEL SNIFFER SYSTEM AND METHOD FOR MULTI- CHANNEL SNIFFER SYNCHRONIZATION |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080066832.3 INTEGRATED CIRCUIT, ELECTRONIC DEVICE AND ESD PROTECTION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080067339.3 INFORMATION PROCESSING DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080067372.6 INTEGRATED CIRCUIT DEVICE AND METHOD FOR GENERATING A TUNING SIGNAL FOR CALIBRATING A VOLTAGE CONTROLLED OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080068132.8 DISPLAY CONTROLLING UNIT, IMAGE DISPLAYING SYSTEM AND METHOD FOR OUTPUTTING IMAGE DATA |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080068158.2 CLOCK CIRCUIT FOR PROVIDING AN ELECTRONIC DEVICE WITH A CLOCK SIGNAL, ELECTRONIC DEVICE WITH A CLOCK CIRCUIT AND METHOD FOR PROVIDING AN ELECTRONIC DEVICE WITH A CLOCK SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080068162.9 ELECTRONIC CIRCUIT, SAFETY CRITICAL SYSTEM, AND METHOD FOR PROVIDING A RESET SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080068267.4 APPARATUS AND METHOD FOR REDUCING PROCESSOR LATENCY |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080068785.6 VIDEO PROCESSING SYSTEM AND METHOD FOR PARALLEL PROCESSING OF VIDEO DATA |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080068792.6 PUSH-PUSH OSCILLATOR CIRCUIT |

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| FREESCALE SEMICONDUCTOR, INC. | CN 201080069170.5 | METHODS FOR PROCESSING A SEMICONDUCTOR WAFER, A SEMICONDUCTOR WAFER AND A SEMICONDUCTOR DEVICE |
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| FREESCALE SEMICONDUCTOR, INC. | CN 201080069623.4 | INTEGRATED CIRCUIT DEVICE, WIRELESS COMMUNICATION UNIT AND METHOD OF MANUFACTURE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080069626.8 | DECODER FOR DETERMINING A SUBSTANCE OR MATERIAL STRUCTURE OF A DETECTED OBJECT BASED ON SIGNALS OF A CAPACTIVE SENSOR AND METHOD FOR DETERMINING A SUBSTANCE OR MATERIAL STRUCTURE OF A DETECTED OBJECT BASED ON SIGNALS ON A CAPACTIVE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080069837.1 | VOLTAGE SWITCHING CIRCUITRY, INTEGRATED DEVICE AND INTEGRATED CIRCUIT, AND METHOD OF VOLTAGE SWITCHING |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080070281.8 | METHOD FOR ENABLING CALIBRATION DURING START-UP OF A MICRO CONTROLLER UNIT AND INTEGRATED CIRCUIT THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080070285.6 | INTEGRATED CIRCUIT DEVICE AND METHOD FOR DETECTING AN EXCESSIVE VOLTAGE STATE |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080070327.6 | METHOD FOR BIT RATE CONTROL WITHIN A SCALABLE VIDEO CODING SYSTEM AND SYSTEM THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080070328.0 | TACTILE INPUT DEVICE, MICROPROCESSOR SYSTEM AND METHOD FOR CONTROLLING A TACTILE INPUT |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080070336.5 | METHOD AND APPARATUS FOR MANAGING POWER IN A MULTI-CORE PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | CN 201080070352.4 | AN INTEGRATED CIRCUIT AND A METHOD OF POWER MANAGEMENT OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN 201110044560.3 | MRAM DEVICE AND METHOD OF ASSEMBLING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN 201110063844.7 | SEMICONDUCTOR DEVICES AND METHODS OF ASSEMBLING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN 201110065715.1 | METHOD OF PACKAGING SEMICONDUCTOR DIE WITH CAP ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | CN 201110082117.5 | SEMICONDUCTOR PACKAGE AND LEAD FRAME THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN 201110094128.5 | METHOD OF ASSEMBLING SEMICONDUCTOR DEVICE WITH INSULATING SUBSTRATE AND HEAT SINK |
| FREESCALE SEMICONDUCTOR, INC. | CN 201110097375.0 | LEAD FRAME WITH COINED INNER LEADS |
| FREESCALE SEMICONDUCTOR, INC. | CN 201110123304.3 | SEMICONDUCTOR DEVICE WITH STAGGERED LEADS |
| FREESCALE SEMICONDUCTOR, INC. | CN 201110127297.4 | SEMICONDUCTOR DEVICE WITH HEAT SPREADER |
| FREESCALE SEMICONDUCTOR, INC. | CN 201110131708.7 | METHOD AND SYSTEM FOR TESING OSCILLATING CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN 201110147062.1 | VIDEO PROCESSING SYSTEM, COMPUTER PROGRAM PRODUCT AND METHOD FOR DECODING AN ENCODED VIDEO STREAM |
| FREESCALE SEMICONDUCTOR, INC. | CN 201110147477.9 | VIDEO PROCESSING SYSTEM, COMPUTER PROGRAM PRODUCT AND METHOD FOR MANAGING A TRANSFER OF INFORMATION BETWEEN A MEMORY UNIT AND A DECODER |
| FREESCALE SEMICONDUCTOR, INC. | CN 201110154414.6 | METHOD OF ASSEMBLING SEMICONDUCTOR DEVICE WITH HEAT SPREADER |
| FREESCALE SEMICONDUCTOR, INC. | CN 201110162405.1 | FLANK WETTABLE SEMICONDUCTOR DEVICE |

| FREESCALE SEMICONDUCTOR, INC. | CN | 201110169920.2 | METHOD OF ASSEMBLING SEMICONDUCTOR DEVICE |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 201110180310.2 | METHOD OF APPARATUS FOR MOLDING SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110189595.6 | BACKLIT VIDEO DISPLAY WITH DYNAMIC LUMINANCE SCALING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110190190.4 | BATTERY CELL EQUALIZER SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110190207.6 | CURRENT REDUCTION IN A SINGLE STAGE CYCLIC ANALOG TO DIGITAL CONVERTER WITH VARIABLE RESOLUTION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110195445.6 | SOFT PROGRAM OF A NON-VOLATILE MEMORY BLOCK |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110205715.7 | STACKED DIE SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110221731.5 | MEMORY WITH LOW VOLTAGE MODE OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110227755.1 | SEMICONDUCTOR DEVICE DIE BONDING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110228725 | DATA PROCESSING SYSTEM WITH PERIPHAL CONFIGURATION INFORMATION ERROR DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110228863.0 | SEMICONDUCTOR DEVICE AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110230237.5 | DIGITAL GLITCH FILTER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110236686.0 | MONOLITHIC MICROWAVE INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110240721.6 | MEMS PRESSURE SENSOR DEVICE AND METHOD OF FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110243371.9 | METHOD FOR FORMING A CAPPED MICRO-ELECTRO- MECHANICAL SYSTEM (MEMS) DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110248478.2 | CHARGE PUMP HAVING RAMP RATE CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110251644.4 | PATTERNING A GATE STACK OF A NON-VOLATILE MEMORY (NVM) WITH SIMULTANEOUS ETCH IN NON-NVM AREA |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110253157.1 | POWER DEVICE AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110262810.0 | MEMS DEVICE ASSEMBLY AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110307017.8 | PROXIMITY OR TOUCH SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110308443.3 | DATA PROCESSING SYSTEM HAVING SELECTIVE INVALIDATION OF SNOOP REQUESTS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110326978.3 | QFN DEVICE AND LEAD FRAME THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110328909.6 | INTEGRATED CIRCUIT HAVING A MEMORY WITH LOW VOLTAGE READ/WRITE OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110334782.9 | METHOD OF MAKING A MICRO-ELECTRO-MECHANICAL- SYSTEMS (MEMS) DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110335789.2 | DEBUGGER RECOVERY ON EXIT FROM LOW POWER MODE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110349969.6 | AREA-EFFICIENT HIGH VOLTAGE BIPOLAR-BASED ESD PROTECTION TARGETING NARROW DESIGN WINDOWS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110356537.8 | INTEGRATED ANTENNA PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110361920.2 | METHOD OF TESTING PARALLEL POWER CONNECTIONS OF |

SEMICONDUCTOR DEVICE

| FREESCALE SEMICONDUCTOR, INC. | CN | 201110362781.5 | DIFFERENTIAL EQUALIZERS WITH SOURCE DEGENERATION AND FEEDBACK CIRCUITS |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 201110375044.9 | PRESSURE SENSOR AND METHOD OF ASSEMBLING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110384933.1 | AUTOMOTIVE RADAR SYSTEM AND METHOD FOR USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110410571.9 | OSCILLATOR SYSTEMS HAVING ANNULAR RESONANT CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110462926.9 | VOLTAGE LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110463126.9 | MASTER SLAVE FLIP-FLOP WITH LOW POWER CONSUMPTION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180005566.8 | METHOD OF MAKING A SEMICONDUCTOR STRUCTURE USEFUL IN MAKING A SPLIT GATE NON-VOLATILE MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180006596.0 | ESD PROTECTION DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180007153.3 | DATA PROCESSING SYSTEM HAVING BROWN-OUT DETECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180007327.6 | QUIESCENT CURRENT (IDDQ) INDICATION AND TESTING APPARATUS AND METHODS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180013415.7 | SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180013625.6 | DC to DC CONVERTER HAVING SWITCH CONTROL AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180015877.2 | SEMICONDUCTOR DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180015959.7 | APPARATUS AND METHOD TO COMPENSATE FOR INJECTION LOCKING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180018612.8 | MULTI-PORT MEMORY HAVING A VARIABLE NUMBER OF USED WRITE PORTS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180021441.4 | EMULATED ELECTRICALLY ERASABLE (EEE) MEMORY AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180021771.3 | CIRCUIT FOR VERIFYING THE WRITE ENABLE OF A ONE TIME PROGRAMMABLE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180022504.8 | OVERVOLTAGE PROTECTION CIRCUIT FOR AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180025514.7 | DATA PROCESSOR HAVING MULTIPLE LOW POWER MODES |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180029997.8 | SWITCHING REGULATOR WITH INPUT CURRENT LIMITING CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180032138.4 | TRANSMISSION GATE CIRCUITRY FOR HIGH VOLTAGE TERMINAL |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180064061.9 | INTEGRATED CIRCUIT DEVICE AND METHOD FOR PERFORMING CONDITIONAL NEGATION OF DATA |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180065549.3 | PHASED-ARRAY RECEIVER, RADAR SYSTEM AND VEHICLE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180065572.2 | DEVICE AND METHOD FOR COMPUTING A FUNCTION VALUE OF A FUNCTION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180065584.5 | INTEGRATED CIRCUIT DEVICE AND METHOD FOR CALCULATING A PREDICATE VALUE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180066480.6 | INTEGRATED CIRCUIT DEVICE, VOLTAGE REGULATION CIRCUITRY AND METHOD FOR REGULATING A VOLTAGE SUPPLY SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180067317.1 | SEMICONDUCTOR DEVICE AND RELATED FABRICATION METHODS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201180067792.9 | OVERCURRENT PROTECTION DEVICE AND METHOD OF OPERATING A POWER SWITCH |
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| CN | 201180067805.2 | OVERCURRENT PROTECTION DEVICE AND METHOD OF OPERATING A POWER SWITCH |
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| CN | 201180069679.4 | METHOD FOR RANKING PATHS FOR POWER OPTIMIZATION OF AN INTEGRATED CIRCUIT DESIGN AND CORRESPONDING COMPUTER PROGRAM PRODUCT |
| CN | 201210017188.1 | MEMS SENSOR WITH FOLDED TORSION SPRINGS |
| CN | 201210017263.4 | IN-LINE REGISTER FILE BITCELL |
| CN | 201210017521.9 | MEMS SENSOR WITH DUAL PROOF MASSES |
| CN | 201210019722.2 | MULTIPLE FUNCTION POWER DOMAIN LEVEL SHIFTER |
| CN | 201210019970.7 | METHOD AND APPARATUS FOR PROCESSING TEMPORAL AND SPATIAL OVERLAPPING UPDATES FOR AN ELECTRONIC DISPLAY |
| CN | 201210020014.0 | VOLTAGE REGULATION CIRCUITRY AND RELATED OPERATING METHODS |
| CN | 201210028857.5 | SEMICONDUCTOR DEVICE AND RELATED FABRICATION METHODS |
| CN | 201210029471.6 | DIGITAL METHOD TO OBTAIN THE I-V CURVES OF NVM BITCELLS |
| CN | 201210035054.2 | MEMS DEVICE HAVING VARIABLE GAP WIDTH AND METHOD OF MANUFACTURE |
| CN | 201210037938.1 | ANCHORED CONDUCTIVE VIA AND METHOD FOR FORMING |
| CN | 201210040831.2 | MEMORY CONTROLLER ADDRESS AND DATA PIN MULTIPLEXING |
| CN | 201210042210.8 | SYNCHRONOUS DATA PROCESSING SYSTEM AND METHOD |
| CN | 201210047612.7 | VOLTAGE LEVEL SHIFTER |
| CN | 201210048097.4 | VIAS BETWEEN CONDUCTIVE LAYERS TO IMPROVE RELIABILITY |
| CN | 201210057325.4 | LEAD FRAME FOR ASSEMBLING SEMICONDUCTOR DEVICE |
| CN | 201210057627.1 | METHOD OF DESIGNING INTEGRATED CIRCUIT THAT ACCOUNTS FOR DEVICE AGING |
| CN | 201210074875.7 | SPLIT-GATE NON-VOLATILE MEMORY CELL HAVING IMPROVED OVERLAP TOLERANCE AND METHOD THEREFOR |
| CN | 201210079180.8 | SELECTABLE THRESHOLD RESET CIRCUIT |
| CN | 201210093356.5 | PATTERNING A GATE STACK OF A NON-VOLATILE MEMORY (NVM) WITH FORMATION OF A CAPACITOR |
| CN | 201210096699.7 | OSCILLATOR CIRCUIT |
| CN | 201210106456.7 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING NANOCRYSTALS |
| CN | 201210114188.3 | MEMS DEVICE WITH CENTRAL ANCHOR FOR STRESS ISOLATION |
| CN | 201210116609.6 | CACHE MEMORY WITH DYNAMIC LOCKSTEP SUPPORT |
| CN | 201210131114.0 | SEMICONDUCTOR DEVICE AND METHOD OF ASSEMBLING SAME |
| CN | 201210137486.4 | ELECTRICALLY PROGRAMMABLE FUSE MODULE IN SEMICONDUCTOR DEVICE |
| CN | 201210141356.8 | RECONFIGURABLE INTEGRATED CIRCUIT |
| | CN C | CN 201210017188.1 CN 201210017263.4 CN 201210017521.9 CN 201210019722.2 CN 201210029471.6 CN 201210035054.2 CN 201210040831.2 CN 201210040831.2 CN 201210047612.7 CN 201210057325.4 CN 201210057325.4 CN 201210079180.8 CN 201210079180.8 CN 201210093356.5 CN 201210096699.7 CN 201210114188.3 CN 201210116609.6 CN 2012101371486.4 |

| FREESCALE SEMICONDUCTOR, INC. | CN | 201210142693.9 | TIMING CONTROL IN SYNCHRONOUS MEMORY DATA TRANSFER |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 201210161809.3 | CHARGE PUMP CIRCUIT WITH FAST START-UP |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210173980.6 | SEMICONDUCTOR SENSOR DEVICE AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210176628.8 | DUAL PORT PRESSURE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210178054.8 | ACTIVE TILING PLACEMENT FOR IMPROVED LATCH-UP IMMUNITY |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210182560.4 | TRIMMING CIRCUIT FOR CLOCK SOURCE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210188567.7 | WRITING DATA TO SYSTEM MEMORY IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210194848.3 | RELAXATION OSCILLATOR WITH LOW POWER CONSUMPTION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210195682.7 | SYSTEM ON CHIP AND CONTROL MODULE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210201083.1 | BRANCH TARGET BUFFER ADDRESSING IN A DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210236232.8 | POWER MOSFET STRUCTURE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210244251.5 | POWER ADAPTER AND ELECTRICAL CONNECTOR THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210251178.4 | MICROWAVE ADAPTORS AND RELATED OSCILLATOR SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210257566.3 | COMPARATOR AND RELAXATION OSCILLATOR EMPLOYING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210263013.9 | COMBINED OUTPUT BUFFER AND ESD DIODE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210289779.4 | CONFIGURABLE CONTINUOUS TIME SIGMA DELTA ANALOG- TO-DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210291502.5 | TRENCH SEMICONDUCTOR DEVICES WITH EDGE TERMINATION STRUCTURES, AND METHODS OF MANUFACTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210295652.3 | IMPLANT FOR PERFORMANCE ENHANCEMENT OF SELECTED TRANSISTORS IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210296941.5 | SEMICONDUCTOR DEVICE WITH WAKE-UP UNIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210305062.4 | POWER MOSFET CURRENT SENSE STRUCTURE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210317297.5 | SEMICONDUCTOR DEVICE PACKAGING HAVING PRE- ENCAPSULATION THROUGH VIA FORMATION USING LEAD FRAMES WITH ATTACHED SIGNAL CONDUITS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210327433.9 | ATTACHING A MEMS TO A BONDING WAFER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210328798.3 | INCIDENT CAPACITIVE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210333682.9 | SEMICONDUCTOR DEVICE AND METHOD OF ASSEMBLING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210334279.8 | SEMICONDUCTOR DEVICE AND METHOD OF ASSEMBLING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210334326.9 | BAND GAP REFERENCE VOLTAGE GENERATOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210349012.6 | METHODS AND APPARATUS FOR TESTING MULTIPLE-IC DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210349048.4 | VOLTAGE-CONTROLLED OSCILLATORS AND RELATED SYSTEMS |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 201210350088.0 | INTERFACE SYSTEM AND METHOD WITH BACKWARD COMPATABILITY |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 201210352749.3 | SEMICONDUCTOR WAFER DICING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210352772.2 | SYSTEM AND METHOD FOR PERFORMING SCAN TEST |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210369230.6 | ROTARY DISK GYROSCOPE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210404564.2 | METHOD FOR VERIFYING DIGITAL TO ANALOG CONVERTER DESIGN |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210417123.6 | INERTIAL SENSOR WITH OFF-AXIS SPRING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210417135.9 | SYSTEMS AND METHODS FOR SEMAPHORE-BASED PROTECTION OF SHARED SYSTEM RESOURCES |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210426250.2 | BUILT-IN SELF TRIM FOR NON-VOLATILE MEMORY REFERENCE CURRENT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210448070.4 | SEMICONDUCTOR SENSOR DEVICE AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210448241.3 | METHOD OF PACKAGING SEMICONDUCTOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210452056.1 | METHOD AND SYSTEM FOR DEBLOCK FILTERING CODED MACROBLOCKS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210468156.3 | RAIL TO RAIL DIFFERENTIAL BUFFER INPUT STAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210485240.6 | HELIX SUBSTRATE AND THREE-DIMENSIONAL PACKAGE WITH SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210487006.7 | MULTI-VOLTAGE DOMAIN CIRCUIT DESIGN VERIFICATION METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210513275.6 | METHOD OF PROTECTING AGAINST VIA FAILURE AND STRUCTURE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210529697.2 | TRENCH GATE TRANSISTOR AND METHOD OF FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210544579.9 | TOUCH SENSE INTERFACE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210545271.6 | SYSTEM FOR OPTIMIZING NUMBER OF DIES PRODUCED ON A WAFER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210551411.0 | STATE RETENTION POWER GATED CELL |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210583531.9 | SEMICONDUCTOR WAFER PLATING BUS AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210584489.2 | EXTENDABLE-ARM ANTENNAS, AND MODULES AND SYSTEMS IN WHICH THEY ARE INCORPORATED |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210597852.4 | WIRE BONDING MACHINE AND METHOD FOR TESTING WIRE BOND CONNECTIONS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210597853.9 | MIXED SIGNAL IP CORE PROTOTYPING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310006802.9 | MONITORING SYSTEM FOR DETECTING DEGRADATION OF INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310016840.2 | SKEWED SRAM CELL |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310024955.6 | PIPELINED ANALOG-TO-DIGITAL CONVERTER HAVING REDUCED POWER CONSUMPTION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310028149.6 | A DELAY LINE PHASE SHIFTER WITH SELECTABLE PHASE SHIFT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310028470.4 | AN ADJUSTABLE POWER SPLITTER AND CORRESPONDING METHODS AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310029975.2 | SEMICONDUCTOR DEVICE HAVING A NANOTUBE LAYER |

AND METHOD FOR FORMING

| FREESCALE SEMICONDUCTOR, INC. | CN | 201310031117.1 | SEMICOCNDUCTOR DEVICE HAVING DIFFERENT NON- VOLATILE MEMORIES HAVING NANOCRYSTALS OF DIFFERING DENSITIES AND METHOD THEREFOR |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 201310031119.0 | STRUCTURE AND METHOD FOR HEALING TUNNEL DIELECTRIC OF NON-VOLATILE MEMORY CELLS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310034892.2 | ENCAPSULANT WITH COROSION INHIBITOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310037748.4 | VIBRATION ROBUST X-AXIS RING GYRO TRANSDUCER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310044690.6 | ELECTRONIC DEVICE FOR DETECTING ERRONEOUS KEY SELECTION ENTRY |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310044701.0 | SELF-ADAPTING VOLTAGE AMPLIFIER AND BATTERY CHARGER DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310074969.9 | MOLD CHASE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310078670.0 | SEMICONDUCTOR DEVICE AND METHOD OF ASSEMBLING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310082531.5 | SAMPLE AND HOLD CIRCUIT AND DIFFERENTIAL SAMPLE AND HOLD CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310089140.6 | RANDOM VALUE PRODUCTION METHODS AND SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310102611.2 | FULLY COMPLEMENTARY SELF-BIASED DIFFERENTIAL RECEIVER WITH STARTUP CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310113519.6 | LOW POWER SRPG CELL |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310118959.0 | ELECTRONIC DEVICE WITH POWER MODE CONTROL BUFFERS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310123041.5 | SEMICONDUCTOR DEVICE WITH INTEGRAL HEAT SINK |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310134795.0 | Sharing Stacked BJT Clamps for System Level ESD Protection |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310140547.7 | MASTER-SLAVE FLIP-FLOP WITH LOW POWER CONSUMPTION |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310146515.8 | ERASING A NON-VOLATILE MEMORY (NVM) SYSTEM HAVING ERROR CORRECTION CODE (ECC) |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310148193.0 | MEMORY WITH WORD LEVEL POWER GATING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310150287.1 | LEAD FRAME AND SUBSTRATE SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310167146.0 | APPARATUS AND METHOD FOR CONTROLLING CHARGE PUMP |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310168850.8 | VOLTAGE LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310184678.5 | TAMPER DETECTOR FOR SECURE MODULE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310187162.6 | BASK DEMODULATOR AND METHOD FOR DEMODULATING BASK MODULATED SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310190891.7 | COMPARATOR AND CLOCK SIGNAL GENERATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310191174.6 | CAVITY-TYPE SEMICONDUCTOR PACKAGE AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310196242.8 | PHOTRONIC DEVICE WITH REFLECTOR AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310201046.5 | APPARATUS FOR CONTROLLING COMPARATOR INPUT OFFSET VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310205001.5 | INDUCTIVE ELEMENT WITH INTERRUPTER REGION AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310205005.3 | FIELD FOCUSING FEATURES IN A RERAM CELL |

| FREESCALE SEMICONDUCTOR, INC. | CN | 201310206388.6 | PROCESSOR RESOURCE AND EXECUTION PROTECTION METHODS AND APPARATUS |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 201310229576.0 | MULTIPLE HELIX SUBSTRATE AND THREE-DIMENSIONAL PACKAGE WITH SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310230768.3 | An New MaxQFP Package |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310237613.2 | Synchronous Rectifier Timer for Discontinuous Mode DC/DC Converter |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310247508.7 | EMULATED ELECTRICALLY ERASABLE MEMORY HAVING AN ADDRESS RAM FOR DATA STORED IN FLASH MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310265326.2 | HIGH BREAKDOWN VOLTAGE LDMOS DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310265329.6 | SEMICONDUCTOR DEVICE AND DRIVER CIRCUIT WITH A CURRENT CARRYING REGION AND ISOLATION STRUCTURE INTERCONNECTED THROUGH A RESISTOR CIRCUIT, AND METHOD OF MANUFACTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310265352.5 | SEMICONDUCTOR DEVICE AND DRIVER CIRCUIT WITH DRAIN AND ISOLATION STRUCTURE INTERCONNECTED THROUGH A DIODE CIRCUIT, AND METHOD OF MANUFACTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310267888.0 | SEMICONDUCTOR DEVICE PACKAGE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310267931.3 | POWER TRANSISTOR WITH HEAT DISSIPATION AND METHOD THEREFORE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310272473.2 | FLIP-FLOP CIRCUIT WITH RESISTIVE POLY ROUTING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310272482.5 | SEMICONDUCTOR DEVICE DIE ATTACHMENT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310277351.2 | Angular Rate Sensor With Quadrature Error Compensation |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310285429.5 | BIPOLAR TRANSISTOR WITH HIGH BREAKDOWN VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310287464.0 | Sensor Package and Method of Forming Same |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310317710.2 | NON-LEADED TYPE SEMICONDUCTOR PACKAGE AND METHOD OF ASSEMBLING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310320678.3 | SINGLE-EVENT LATCH-UP PREVENTION TECHNIQUES FOR A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310323638.4 | VARIABLE RELUCTANCE SENSOR INTERFACE WITH INTEGRATION BASED ARMING THRESHOLD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310350039.1 | LOW DROPOUT VOLTAGE REGULATOR WITH A FLOATING VOLTAGE REFERENCE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310377459.9 | WAVEFORM CONVERSION CIRCUIT WITH REDUCED JITTER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310410093.0 | VOLTAGE TRANSLATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310410597.2 | MICROELECTRONIC PACKAGES HAVING TRENCH VIAS AND METHODS FOR THE MANUFACTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310411053.8 | SYSTEMS AND METHODS FOR CODE PROTECTION IN NON-VOLATILE MEMORY SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310413821.3 | SEMICONDUCTOR DEVICES WITH IMPEDANCE MATCHING CIRCUITS, AND METHODS OF MANUFACTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310415650.8 | Matrix Lid Heatspreader for Flip Chip Package |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310416804.5 | NVM WITH CHARGE PUMP AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310436857.3 | ELECTRONIC CIRCUITS WITH VARIABLE ATTENUATORS AND |

METHODS OF THEIR OPERATION

| FREESCALE SEMICONDUCTOR, INC. | CN | 201310437393.8 | METHOD OF MAKING A LOGIC TRANSISTOR AND A NON- VOLATILE MEMORY (NVM) CELL |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 201310450260.4 | STATE RETENTION POWER GATED CELL |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980153609.X | CIRCUIT AND METHOD FOR SPEED MONITORING OF AN ELECTRIC MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980153662.X | METHOD, SYSTEM AND INTEGRATED CIRCUIT FOR ACCESS TO A MEMORY ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980158910.X | WIRELESS COMMUNICATION DEVICE AND SEMICONDUCTOR PACKAGE DEVICE HAVING A POWER AMPLIFIER THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980160481.X | DIVERSITY RECEIVER AND TRANSCEIVER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 200980162601.X | METHOD AND SYSTEM FOR ENABLING ACCESS TO FUNCTIONALITY PROVIDED BY RESOURCES OUTSIDE OF AN OPERATING SYSTEM ENVIRONMENT |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201010276483.X | LEAD FRAME FOR SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201010590311.X | BRACE FOR LONG BOND WIRE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080005845.X | MEMORY HAVING NEGATIVE VOLTAGE WRITE ASSIST CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080008701.X | DYNAMIC RANDOM ACCESS MEMORY (DRAM) REFRESH |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080015418.X | SENSOR DEVICE WITH REDUCED PARASITIC-INDUCED ERROR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080051994.X | MEMORY DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080065699.X | POWER GATING CONTROL MODULE, INTEGRATED CIRCUIT DEVICE, SIGNAL PROCESSING SYSTEM, ELECTRONIC DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080066558.X | AUDIO COMMUNICATION DEVICE, METHOD FOR OUTPUTTING AN AUDIO SIGNAL, AND COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080066942.X | POWER SWITCHING APPARATUS AND METHOD FOR IMPROVING CURRENT SENSE ACCURACY |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080067368.X | METHOD FOR PROVIDING DATA PROTECTION FOR DATA STORED WITHIN A MEMORY ELEMENT AND INTEGRATED CIRCUIT DEVICE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080068259.X | LATCH CIRCUIT, FLIP-FLOP CIRCUIT AND FREQUENCY DIVIDER |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201080068795.X | MEMORY MANAGEMENT UNIT FOR A MICROPROCESSOR SYSTEM, MICROPROCESSOR SYSTEM AND METHOD FOR MANAGING MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110000656.X | PRESSURE SENSOR AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110062115.X | MRAM DEVICE AND METHOD OF ASSEMBLING SAME |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110246814.X | TOUCH SENSOR CONTROLLER FOR DRIVING A TOUCH SENSOR SHIELD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110293438.X | DATA PROCESSOR FOR PROCESSING DECORATED INSTRUCTIONS WITH CACHE BYPASS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110356332.X | METHOD AND APPARATUS FOR MONITORING FREE AIR BALL (FAB) FORMATION IN WIRE BONDING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110400936.X | PROCESSOR WITH PROGRAMMABLE VIRTUAL PORTS |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201110461367.X | TOUCH PAD CAPACITIVE SENSOR CIRCUIT |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 201180067127.X | INTEGRATED CIRCUIT DEVICE, POWER MANAGEMENT MODULE AND METHOD FOR PROVIDING POWER MANAGEMENT |
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| FREESCALE SEMICONDUCTOR, INC. | CN | 201210100138.X | OSCILLATOR CIRCUIT FOR GENERATING CLOCK SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210401167.X | LOW POWER SCAN FLIP-FLOP CELL |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210407786.X | SEMICONDUCTOR STRUCTURE HAVING A THROUGH SUBSTRATE VIA (TSV) AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201210543767.X | PACKAGED LEADLESS SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310209342.X | SPLIT PAD FOR CIRCUIT BOARD |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310237859.X | CAPACITIVE KEYPAD POSITION SENSOR WITH LOW CROSS-INTERFERENCE |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310264977.X | A SEMICONDUCTOR PACKAGE STRUCTURE HAVING AN AIR GAP AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | CN | 201310292129.X | METHODS AND STRUCTURES FOR MULTIPORT MEMORY DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | MEMORY DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | ISOLATED CAPACITORS WITHIN SHALLOW TRENCH ISOLATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | SENSOR DEVICE WITH SEALING STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | MICRO ELECTROMECHANICAL SYSTEMS (MEMS) HAVING A GAP STOP AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | STACKED SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | STACKED SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | RERAM DEVICE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | LOGIC TRANSISTOR AND NON-VOLATILE MEMORY CELL INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | HIGH PRECISION SINGLE EDGE CAPTURE AND DELAY MEASUREMENT CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | VEHICLE-BORNE RADAR SYSTEMS WITH CONTINUOUS- TIME, SIGMA DELTA ANALOG-TO-DIGITAL CONVERTERS, AND METHODS OF THEIR OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | STRESS-BASED TECHNIQUES FOR DETECTING AN IMMINENT READFAILURE IN A NON-VOLATILE MEMORY ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | INTEGRATED CIRCUIT DIE ASSEMBLY WITH HEAT SPREADER |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | CLOCKED MEMORY WITH WORD LINE ACTIVATION DURING A FIRST PORTION OF THE CLOCK CYCLE |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | CLOCKED MEMORY WITH LATCHING PREDECODER CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | SENSING DEVICE AND RELATED OPERATING METHODS |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | METHODS AND SYSTEMS FOR ADJUSTING NVM CELL BIAS CONDITIONS BASED UPON OPERATING TEMPERATURE TO REDUCE PERFORMANCE DEGRADATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | METHODS AND SYSTEMS FOR ADJUSTING NVM CELL BIAS CONDITIONS FOR PROGRAM/ERASE OPERATIONS TO |

REDUCE PERFORMANCE DEGRADATION

| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | CAPACITIVE PRESSURE SENSOR IN AN OVERMOLDED PACKAGE |
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| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | TRANSDUCER-INCLUDING DEVICES, AND METHODS AND APPARATUS FOR THEIR CALIBRATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | RECONFIGURABLE CIRCUIT AND DECODER THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | NON-VOLATILE MEMORY (NVM) THAT USES SOFT PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | Sensor Packaging Method and Sensor Packages |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | DATA PROCESSOR DEVICE FOR HANDLING A WATCHPOINT AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | PRESSURE SENSOR WITH DIFFERENTIAL CAPACITIVE OUTPUT |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | LEADFRAMES, AIR-CAVITY PACKAGES, AND ELECTRONIC DEVICES WITH OFFSET VENT HOLES, AND METHODS OF THEIR MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | WIRELESS POWER TRANSMITTERS WITH WIDE INPUT VOLTAGE RANGE AND METHODS OF THEIR OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | NON-VOLATILE MEMORY (NVM) WITH ADAPTIVE WRITE OPERATIONS |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | SEMICONDUCTOR PACKAGE WITH STRESS RELIEF AND HEAT SPREADER |
| FREESCALE SEMICONDUCTOR, INC. | CN | Not yet available | STATE RETENTION POWER GATED CELL FOR INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | CN | PCT/IB2011/051285 | PROCESSOR SYSTEM WITH PREDICATE REGISTER, COMPUTER SYSTEM, METHOD FOR MANAGING PREDICATES AND COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | CN | PCT/IB2011/051353 | INTEGRATED CIRCUIT DEVICE AND METHODS OF PERFORMING BIT MANIPULATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | CN | PCT/IB2011/051357 | A METHOD AND APPARATUS FOR CONTROLLING FETCH- AHEAD IN A VLES PROCESSOR ARCHITECTURE |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL200980141501.9 | METHOD OF MAKING A SPLIT GATE MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | CN | ZL200980144991.8 | ADAPTIVE IIP2 CALIBRATION |
| FREESCALE SEMICONDUCTOR, INC. | DE | 02729351.3 | COMPONENT WITH FILTER AND METHOD OF MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | DE | 04810477.2 | APPARATUS AND METHOD FOR TIME ORDERING EVENTS IN A SYSTEM HAVING MULTIPLE TIME DOMAINS |
| FREESCALE SEMICONDUCTOR, INC. | DE | 08713946.5 | MULTI-LAYER SOURCE/DRAIN STRESSOR |
| FREESCALE SEMICONDUCTOR, INC. | DE | 09787356.6 | WIRELESS COMMUNICATION DEVICE AND SEMICONDUCTOR PACKAGE DEVICE HAVING A POWER AMPLIFIER THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | DE | 09803305.3 | BRANCH TARGET BUFFER ALLOCATION |
| FREESCALE SEMICONDUCTOR, INC. | DE | 09846744.2 | MULTICHANNEL RECEIVER SYSTEM AND METHOD FOR MULTICHANNEL RECEIVER MONITORING |
| FREESCALE SEMICONDUCTOR, INC. | DE | 10712502.3 | CHIP DAMAGE DETECTION DEVICES FOR A SEMICONDUCTOR INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | DE | 102006051151.4 | METHOD FOR FORMING MULTI-LAYER BUMPS ON A SUBSTRATE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 02713474.1 | LITHOGRAPHIC TEMPLATE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 02729351.3 | COMPONENT WITH FILTER AND METHOD OF MANUFACTURING |

MANUFACTURING

| FREESCALE SEMICONDUCTOR, INC. | EP | 02790328.5 | COMMUNICATION NETWORK AND ARRANGEMENT FOR USE THEREIN |
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| FREESCALE SEMICONDUCTOR, INC. | EP | 03714137.1 | SEMICONDUCTOR DEVICE HAVING A WIRE BOND PAD AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 03742271.4 | HETERO-INTEGRATION OF SEMICONDUCTOR MATERIALS ON SILICON |
| FREESCALE SEMICONDUCTOR, INC. | EP | 03809486.8 | APPARATUS AND METHOD FOR POWER MANAGEMENT IN A TIRE PRESSURE MONITORING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | EP | 04801054.0 | LOW-POWER COMPILER-PROGRAMMABLE MEMORY WITH FAST ACCESS TIMING |
| FREESCALE SEMICONDUCTOR, INC. | EP | 04804851.6 | FREQUENCY GENERATION IN A WIRELESS COMMUNICATION UNIT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 04805019.9 | POWER CONTROL SYSTEM FOR A WIRELESS COMMUNICATION UNIT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 04810477.2 | APPARATUS AND METHOD FOR TIME ORDERING EVENTS IN A SYSTEM HAVING MULTIPLE TIME DOMAINS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 04811469.8 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT, AND SEMICONDUCTOR COMPONENT FORMED THEREBY |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05702507.4 | DEVICE HAVING FAILURE RECOVERY CAPABILITIES AND A METHOD FOR FAILURE RECOVERY |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05702531.4 | AUDIO COMMUNICATION UNIT WITH INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05708797.5 | SMART POWER REGULATION IN LOW COST BATTERY CHARGING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05711379.7 | METHOD OF MAKING A SEMICONDUCTOR DEVICE USING TREATED PHOTORESIST |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05711887.9 | SEMICONDUCTOR PACKAGE WITH CROSSING CONDUCTOR ASSEMBLY AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05712099.0 | METHOD AND APPARATUS FOR DOHERTY AMPLIFIER BIASING |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05725380.9 | WIRELESS TRANSCEIVER AND METHOD OF OPERATING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05728353.3 | MULTIPLE-STAGE FILTERING DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05732055.8 | MASKING WITHIN A DATA PROCESSING SYSTEM HAVING APPLICABILITY FOR A DEVELOPMENT INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05732887.4 | SEMICONDUCTOR DEVICE AND METHOD OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05736239.4 | ADAPTIVE PROTECTION CIRCUIT FOR A POWER AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05738443.0 | PROTECTION OF AN INTEGRATED CIRCUIT AND METHOD THEREFORE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05738546.0 | SEPARATELY STRAINED N-CHANNEL AND P-CHANNEL TRANSISTORS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05740025.1 | IDEA FOR FORMING FUSI GATE WITH HIGH GATE DIELECTRIC |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05742467.3 | METHOD AND DEVICE FOR PROCESSING IMAGE DATA |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05744165.1 | MEMORY DEVICE WITH A DATA HOLD LATCH |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05766956.6 | METHOD AND SYSTEM FOR PERFORMING DEBLOCKING FILTERING |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05766959.0 | DEVICE AND METHOD FOR COMPENSATING FOR VOLTAGE DROPS |
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| FREESCALE SEMICONDUCTOR, INC. | EP | 05767906.0 | METHOD OF FORMING A SEMICONDUCTOR STRUCTURE |
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| FREESCALE SEMICONDUCTOR, INC. | EP | 05776970.5 | DEVICE AND METHOD FOR MEDIA ACCESS CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05778236.9 | A RECEIVER AND A METHOD FOR CHANNEL ESTIMATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05782558.0 | METHOD OF FORMING A NANOCLUSTER CHARGE STORAGE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05782794.1 | PORE SEALING AND CLEANING POROUS LOW DIELECTRIC CONSTANT STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05782905.3 | SEMICONDUCTOR DEVICE AND METHOD OF FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05782962.4 | WIRELESS COMMUNICATION UNIT AND METHOD FOR HANDOVER |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05789338.0 | POWER SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING A POWER SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05798898.2 | APPARATUS AND METHOD FOR PROVIDING INFORMATION TO A CACHE MODULE USING FETCH BURSTS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05799438.6 | SYSTEM AND METHOD FOR CONTROLLING VOLTAGE AND FREQUENCY IN A MULTIPLE VOLTAGE ENVIRONMENT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05801606.4 | METHOD AND APPARATUS FOR NON-INTRUSIVE TRACING |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05804148.4 | DEVICE AND METHOD FOR COMPENSATING FOR VOLTAGE DROPS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05810905.9 | ELECTRONIC DEVICE AND METHOD FOR CONTROLLING CURRENT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05815815.5 | WIRELESS SUBCRIBER COMMUNICATION UNIT AND METHOD OF POWER CONTROL THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05816173.8 | METHOD FOR CLEANING A SEMICONDUCTOR STRUCTURE AND CHEMISTRY THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 05822578.0 | METHOD OF INTEGRATING OPTICAL DEVICES AND ELECTRONIC DEVICES ON AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06118723.3 | METHOD OF IDENTIFYING AN IMPROVED CONFIGURATION FOR A COMMUNICATION SYSTEM USING CODING GAIN AND AN APPARATUS THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06701214.6 | PROTECTION SYSTEM AND METHOD OF OPERATION THEREIN |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06710929.8 | A METHOD FOR SCHEDULING ATM CELLS AND A DEVICE HAVING ATM CELL SCHEDULING CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06723039.1 | AN ELECTRONIC DEVICE HAVING A MEMORY ELEMENT AND METHOD OF OPERATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06724650.4 | SEMICONDUCTOR DEVICE STRUCTURE AND INTEGRATED CIRCUIT THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06735153.6 | INTERLAYER DIELECTRIC UNDER STRESS FOR AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06739498.1 | SYSTEM AND METHOD FOR PROTECTING LOW VOLTAGE TRANSCEIVER |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06761965.0 | BIAS CIRCUIT FOR A RADIO FREQUENCY POWER-AMPLIFIER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06765736.1 | A METHOD AND DEVICE FOR PROVIDING A SECURITY BREACH INDICATIVE AUDIO ALERT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06773131.5 | SUBSTRATE CONTACT FOR A CAPPED MEMS AND METHOD OF |

MAKING THE SUBSTRATE CONTACT AT THE WAFER LEVEL

| FREESCALE SEMICONDUCTOR, INC. | EP | 06777374.7 | METHOD ANS SYSTEM FOR TRANSMITTING A DATUM FROM A TIME-DEPENDENT DATA STORAGE MEANS |
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| FREESCALE SEMICONDUCTOR, INC. | EP | 06777377.0 | METHOD AND APPARATUS FOR TRANSMITTING DATA IN A FLEXRAY NODE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06777421.6 | METHOD AND SYSTEM OF GROUPING INTERRUPTS FROM A TIME-DEPENDENT DATA STORAGE MEANS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06777587.4 | IMPROVEMENTS IN OR RELATING TO BUFFER MANAGEMENT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06777712.8 | MICROPROCESSOR AND METHOD FOR REGISTER ADDRESSING THEREIN |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06788428.8 | PACKAGED INTEGRATED CIRCUIT WITH ENHANCED THERMAL DISSIPATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06800928.1 | A BOUNDED SIGNAL MIXER AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06807261.0 | ANALOGUE-TO-DIGITAL CONVERTER APPARATUS AND METHOD OF REUSING AN ANALOGUE-TO-DIGITAL CONVERTER CICRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06809343.4 | ELECTROSTATIC DISCHARGE PROTECTION APPARATUS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06816682.6 | ELECTRONIC DEVICE INCLUDING A TRANSISTOR STRUCTURE HAVING AN ACTIVE REGION ADJACENT TO A STRESSOR LAYER AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06816841.8 | FINE PITCH INTERCONNECT AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06821265.3 | NETWORK AND METHOD FOR SETTING A TIME-BASE OF A NODE IN THE NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06821314.9 | PROTECTION CIRCUIT APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06830063.1 | MEMORY SYSTEM AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06830820.4 | POWER SUPPLY SWITCHING APPARATUS WITH SEVERE OVERLOAD DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06831874.0 | DATA COMMUNICATION SYSTEM AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06842417.5 | IMAGE PROCESSING APPARATUS AND METHOD OF TRANSFERRING IMAGE DATA |
| FREESCALE SEMICONDUCTOR, INC. | EP | 06851955.2 | SEMICONDUCTOR DEVICE AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07703810.7 | COMMUNICATION DEVICE, INTEGRATED CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07705686.9 | SEMICONDUCTOR DEVICE AND METHOD OF FORMING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07726215.2 | CALIBRATION SIGNAL GENERATOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07735889.3 | GENERATING A FRAME OF AUDIO DATA |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07735894.3 | LOW COST FAULT TOLERANT SLAVE NODE IN AN HETEROGENEOUS NETWORK OF NODES |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07756373.2 | NOISE ISOLATION BETWEEN CIRCUIT BLOCKS IN AN INTEGRATED CIRCUIT CHIP |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07756489.6 | APPARATUS AND METHOD FOR ADJUSTING AN OPERATING PARAMETER OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07757307.9 | MEMORY WITH CLOCKED SENSE AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07757316.0 | SEMICONDUCTOR FABRICATION PROCESS USING ETCH STOP LAYER TO OPTIMIZE FORMATION OF SOURCE/DRAIN STRESSOR |

| FREESCALE SEMICONDUCTOR, INC. | EP | 07757888.8 | MEMORY CIRCUIT |
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| FREESCALE SEMICONDUCTOR, INC. | EP | 07758028.0 | STRESSOR INTEGRATION AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07758081.9 | NON-VOLATILE MEMORY WITH CONTROLLED PROGRAM/ERASE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07758334.2 | TRANSISTOR AND METHOD WITH DUAL LAYER PASSIVATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07758336.7 | LEAD FRAME BASED, OVER-MOLDED SEMICONDUCTOR PACKAGE WITH INTEGRATED THROUGH HOLE TECHNOLOGY (THT) HEAT SPREADER PIN(S) AND ASSOCIATED METHOD OF MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07760578.0 | SYSTEM AND METHOD FOR SHARING RESET AND BACKGROUND COMMUNICATION ON A SINGLE MCU PIN |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07777658.1 | DYNAMIC TIMING ADJUSTMENT IN A CIRCUIT DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07789692.6 | CIRCUIT ARRANGEMENT FOR FILTERING UNWANTED SIGNALS FROM A CLOCK SIGNAL, PROCESSING SYSTEM AND METHOD OF FILTERING UNWANTED SIGNALS FROM A CLOCK SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07789911.0 | DIGITAL SQUIB DRIVER |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07789925.0 | INTEGRATED CIRCUIT COMPRISING ERROR CORRECTION LOGIC, AND A METHOD OF ERROR CORRECTION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07797098.6 | FLEXIBLE MACROBLOCK ORDERING WITH REDUCED DATA TRAFFIC AND POWER CONSUMPTION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07797139.8 | MESSAGE BUFFER FOR A RECEIVER APPARATUS ON A COMMUNICATIONS BUS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07798752.7 | VIDEO INFORMATION PROCESSING SYSTEM WITH SELECTIVE CHROMA DEBLOCK FILTERING |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07805073.9 | CIRCUIT, INTEGRATED CIRCUIT AND METHOD FOR DISSIPATING HEAT FROM AN INDUCTIVE LOAD |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07805075.4 | INTEGRATED CIRCUIT, ELECTRONIC DEVICE AND ESD PROTECTION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07814592.7 | SCALING VIDEO PROCESSING COMPLEXITY BASED ON POWER SAVINGS FACTOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07814883.0 | SENSOR HAVING FREE FALL SELF-TEST CAPABILITY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07826062.7 | MOTOR CONTROLLER FOR DETERMINING A POSITION OF A ROTOR OF AN AC MOTOR, AC MOTOR SYSTEM, AND METHOD OF DETERMINING A POSITION OF A ROTOR OF AN AC MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07826833.1 | METHOD, INTEGRATED CIRCUIT, AND COMMUNICATION UNIT FOR SCHEDULING A PROCESSING OF PACKET STREAM CHANNELS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07840436.5 | LOCALIZED CONTENT ADAPTIVE FILTER FOR LOW POWER SCALABLE IMAGE PROCESSING |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07843360.4 | METHOD OF MAKING A CONTACT ON A BACKSIDE OF A DIE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07853658.8 | METHOD OF PACKAGING A SEMICONDUCTOR DEVICE AND A PREFABRICATED CONNECTOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07854550.6 | DYNAMIC ALLOCATION OF MESSAGE BUFFERS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 07859537.8 | DATA PROCESSOR PERFORMANCE PREDICTION |
| EDEECCALE CELACONDICEOD INC | ED | 00540055 | MIXED CIDCULE |

EP 08710075.6 MIXER CIRCUIT

FREESCALE SEMICONDUCTOR, INC.

| FREESCALE SEMICONDUCTOR, INC. | EP | 08713946.5 | MULTI-LAYER SOURCE/DRAIN STRESSOR |
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| FREESCALE SEMICONDUCTOR, INC. | EP | 08719701.8 | TONE MONITORING APPARATUS AND METHOD OF IDENTIFYING A TONE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08727500.4 | METHOD OF MAKING A NON-VOLATILE MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08727504.6 | METHOD OF MAKING A SEMICONDUCTOR DEVICE HAVING HIGH VOLTAGE TRANSISTORS, NON-VOLATILE MEMORY TRANSISTORS, AND LOGIC TRANSISTORS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08729114.2 | MICROELECTRONIC ASSEMBLY WITH IMPROVED ISOLATION VOLTAGE PERFORMANCE AND A METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08729512.7 | SOURCE/DRAIN STRESSOR AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08730837.5 | ANALOG TO DIGITAL CONVERTER WITH AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08737801.4 | A SYSTEM AND A METHOD FOR SELECTING A CACHE WAY |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08746993.8 | THREAD DE-EMPHASIS INSTRUCTION FOR MULTITHREADED PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08751147.3 | METHOD AND APPARATUS FOR DECODING RECEIVED DATA SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08751258.8 | DISPLAY CONTROLLER, IMAGE PROCESSING SYSTEM, DISPLAY SYSTEM, APPARATUS AND COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08754938.2 | LOW VOLTAGE DATA PATH IN MEMORY ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08763210.5 | APPARATUS AND A METHOD FOR DETECTING FAULTS IN THE DELIVERY OF ELECTRICAL POWER TO ELECTRICAL LOADS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08763466.3 | PROCESSING POSITION-RELATED INPUT DATA FROM A ROTATIONAL MACHINE WHOSE ANGULAR SPEED IS VARIABLE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08771855.7 | METHOD OF PACKAGING AN INTEGRATED CIRCUIT DIE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08776432.0 | MEMORY SYSTEM AND SEMICONDUCTOR DEVICE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08781552.8 | INTERCONNECT IN A MULTI-ELEMENT PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08781984.3 | SEMICONDUCTOR DEVICE TEST SYSTEM HAVING REDUCED CURRENT LEAKAGE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08782025.4 | DUAL GATE OXIDE DEVICE INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08789549.6 | POLY-RESISTOR, AND LINEAR AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08789638.7 | HETERO-STRUCTURE FIELD EFFECT TRANSISTOR, INTEGRATED CIRCUIT INCLUDING A HETERO-STRUCTURE FIELD EFFECT TRANSISTOR AND METHOD FOR MANUFACTURING A HETERO-STRUCTURE FIELD EFFECT TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08807471.1 | AN ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT, EQUIPMENT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08807502.3 | METHOD OF FORMING A POWER SEMICONDUCTOR DEVICE AND POWER SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08858814.0 | ERROR DETECTOR IN A CACHE MEMORY USING CONFIGURABLE WAY REDUNDANCY |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08867823.0 | 3-D SEMICONDUCTOR DIE STRUCTURE WITH CONTAINING FEATURE AND METHOD |
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08872032.1 ELECTROSTATIC DISCHARGE PROTECTION

EP

FREESCALE SEMICONDUCTOR, INC.

| FREESCALE SEMICONDUCTOR, INC. | EP | 08875847.9 | COMMUNICATING ON AN ELECTRICAL BUS |
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| FREESCALE SEMICONDUCTOR, INC. | EP | 08875848.7 | COMPUTATIONAL GENERATION OF NARROW-BANDWIDTH DIGITAL SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08875934.5 | FLEXIBLE BUS DRIVER |
| FREESCALE SEMICONDUCTOR, INC. | EP | 08875951.9 | TRANSISTOR POWER SWITCH DEVICE RESISTANT AGAINST REPETITIVE AVALANCHE BREAKDOWN |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09171681.1 | DEVICE AND METHOD FOR COMPENSATING FOR VOLTAGE DROPS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09714840.7 | MICROELECTROMECHANICAL SYSTEMS COMPONENT AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09715944.6 | RESISTOR TRIGGERED ELECTROSTATIC DISCHARGE PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09720623.9 | READ REFERENCE TECHNIQUE WITH CURRENT DEGRADATION PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09727967.3 | DUAL GATE LATERAL DIFFUSED MOS TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09731806.7 | SPRING MEMBER FOR USE IN A MICROELECTROMECHANICAL SYSTEMS SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09764060.1 | TRANSISTOR POWER SWITCH DEVICE AND METHOD OF MEASURING ITS CHARACTERISTICS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09786286.6 | CIRCUIT AND METHOD FOR SPEED MONITORING OF AN ELECTRIC MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09786287.4 | METHOD, SYSTEM AND INTEGRATED CIRCUIT FOR ACCESS TO A MEMORY ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09786290.8 | DETERMINING INITIAL ROTOR POSITION OF AN ALTERNATING CURRENT MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09786348.4 | SEMICONDUCTOR STRUCTURE, AN INTEGRATED CIRCUIT INCLUDING A SEMICONDUCTOR STRUCTURE AND A METHOD FOR MANUFACTURING A SEMICONDUCTOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09786706.3 | TOUCH-SCREEN INTERFACE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09786707.1 | BATTERY CHARGING CIRCUIT AND ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09786896.2 | INTEGRATED CIRCUIT COMPRISING TRACE LOGIC AND METHOD FOR PROVIDING TRACE INFORMATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09787296.4 | INTEGRATED CIRCUIT COMPRISING VOLTAGE MODULATION CIRCUITRY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09787302.0 | DIVERSITY ANTENNA SYSTEM AND TRANSMISSION METHOD |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09787303.8 | DIVERSITY RECEIVER AND TRANSCEIVER |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09787356.6 | WIRELESS COMMUNICATION DEVICE AND SEMICONDUCTOR PACKAGE DEVICE HAVING A POWER AMPLIFIER THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09800718.0 | DEBUG MESSAGE GENERATION USING A SELECTED ADDRESS TYPE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09800726.3 | BURIED ASSYMETRIC JUNCTION ESD PROTECTION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09807470.1 | HIGH POWER SEMICONDUCTOR DEVICE FOR WIRELESS APPLICATIONS AND METHOD OF FORMING A HIGH POWER SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09808557.4 | TRANSISTOR WITH GAIN VARIATION COMPENSATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09820959.6 | INTERRUPT ACKNOWLEDGMENT IN A DATA PROCESSING |

SYSTEM

| FREESCALE SEMICONDUCTOR, INC. | EP | 09822395.1 | METHOD OF MAKING A SPLIT GATE MEMORY CELL |
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| FREESCALE SEMICONDUCTOR, INC. | EP | 09830864.6 | TOUCH SENSOR PANEL USING REGIONAL AND LOCAL ELECTRODES TO INCREASE NUMBER OF SENSE LOCATIONS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09832363.7 | ERROR DETECTION IN A MULTI-PROCESSOR DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09839931.4 | INTEGRATED CIRCUIT COMPRISING FREQUENCY GENERATION CIRCUITRY FOR CONTROLLING A FREQUENCY SOURCE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09840268.8 | PROCESSING DATA FLOWS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09842554.9 | RADIO FREQUENCY REMOTE CONTROLLER DEVICE, INTEGRATED CIRCUIT AND METHOD FOR SELECTING AT LEAST ONE DEVICE TO BE CONTROLLED |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09842903.8 | A METHOD AND SYSTEM ARRANGED FOR FILTERING AN IMAGE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09844556.2 | TONE RELAY SYSTEM AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09844559.6 | INTEGRATED CIRCUIT AND INTEGRATED CIRCUIT PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09846747.5 | INTEGRATED CIRCUIT WITH CHANNEL ESTIMATION MODULE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09847273.1 | INTEGRATED CIRCUIT, COMMUNICATION UNIT AND METHOD FOR PHASE ADJUSTMENT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09847274.9 | INTEGRATED CIRCUIT, TRANSCEIVER AND METHOD FOR LEAKAGE CANCELLATION IN A RECEIVE PATH |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09847275.6 | DATA ADMINISTRATION UNIT, DATA ACCESS UNIT, NETWORK ELEMENT, NETWORK, AND METHOD FOR UPDATING A DATA STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09847522.1 | SIGNAL PROCESSING SYSTEM, INTEGRATED CIRCUIT COMPRISING BUFFER CONTROL LOGIC AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09849718.3 | DUTY CYCLE CORRECTOR AND DUTY CYCLE CORRECTION METHOD |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09851059.7 | RESPONSE TO WEAROUT IN AN ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09851060.5 | CONFERENCE CALL SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09851225.4 | ADVANCED COMMUNICATION CONTROLLER UNIT AND METHOD FOR RECORDING PROTOCOL EVENTS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09851400.3 | VERTICAL POWER TRANSISTOR DEVICE, SEMICONDUCTOR DIE AND METHOD OF MANUFACTURING A VERTICAL POWER TRANSISTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09851401.1 | PUMP SYSTEM AND MOTORIZED VEHICLE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09851596.8 | METHOD AND SYSTEM FOR ENABLING ACCESS TO FUNCTIONALITY PROVIDED BY RESOURCES OUTSIDE OF AN OPERATING SYSTEM ENVIRONMENT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09851597.6 | RECEIVER AND METHOD FOR EQUALIZING SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09851598.4 | INTEGRATED CIRCUIT AND METHOD FOR REDUCING VIOLATIONS OF A TIMING COSTRAINT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 09851600.8 | BYPASS CAPACITOR CIRCUIT AND METHOD OF PROVIDING A |

BYPASS CAPACITANCE FOR AN INTEGRATED CIRCUIT DIE

| FREESCALE SEMICONDUCTOR, INC. | EP | 10712502.3 | CHIP DAMAGE DETECTION DEVICES FOR A SEMICONDUCTOR INTEGRATED CIRCUIT |
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| FREESCALE SEMICONDUCTOR, INC. | EP | 10736186.7 | DUAL HIGH-K OXIDES WITH SiGe CHANNEL |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10736189.1 | AUTHENTICATED DEBUG ACCESS FOR FIELD RETURNS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10738898.5 | SUBSTRATE BONDING WITH METAL GERMANIUM SILICON MATERIAL |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10741553.1 | EXPOSED PAD BACKSIDE PRESSURE SENSOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10742033.3 | INTEGRATED CIRCUIT, ELECTRONIC DEVICE AND ESD PROTECTION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10744102.4 | DYNAMIC RANDOM ACCESS MEMORY (DRAM) REFRESH |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10746596.5 | CONTINUOUS-TIME SIGMA-DELTA MODULATOR WITH MULTIPLE FEEDBACK PATHS HAVING INDEPENDENT DELAYS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10749489.0 | INTEGRATED CIRCUIT DEVICE AND METHOD FOR GENERATING A TUNING SIGNAL FOR CALIBRATING A VOLTAGE CONTROLLED OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10756542.6 | VERTICALLY INTEGRATED MEMS ACCELERATION TRANSDUCER |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10762036.1 | NEGATIVE VOLTAGE GENERATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10762097.3 | SENSOR DEVICE WITH REDUCED PARASITIC-INDUCED ERROR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10764819.8 | THROUGH SUBSTRATE VIAS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10775238.8 | METHOD TO CALIBRATE START VALUES FOR WRITE LEVELING IN A MEMORY SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10776806.1 | INTEGRATED CIRCUIT DEVICE, ELECTRONIC DEVICE AND METHOD FOR DETECTING TIMING VIOLATIONS WITHIN A CLOCK SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10778097.5 | DEVICE WITH PROXIMITY DETECTION CAPABILITY |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10786551.1 | METHOD AND CIRCUIT FOR CHARGING AND DISCHARGING A CIRCUIT NODE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10786554.5 | PROCESSOR AND METHOD FOR DYNAMIC AND SELECTIVE ALTERATION OF ADDRESS TRANSLATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10795792.0 | POWER SWITCHING APPARATUS AND METHOD FOR IMPROVING CURRENT SENSE ACCURACY |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10797771.2 | RECEIVER WITH AUTOMATIC GAIN CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10798596.2 | METHODS FOR PROCESSING A SEMICONDUCTOR WAFER, A SEMICONDUCTOR WAFER AND A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10805821.5 | INTEGRATED CIRCUIT DEVICE, WIRELESS COMMUNICATION UNIT AND METHOD OF MANUFACTURE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10806982.4 | PULSE WIDTH MODULATION FREQUENCY CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10809168.7 | VOLTAGE SWITCHING CIRCUITRY, INTEGRATED DEVICE AND INTEGRATED CIRCUIT, AND METHOD OF VOLTAGE SWITCHING |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10814136.7 | MEMS DEVICE WITH STRESS ISOLATION AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10817624.9 | MEMORY DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10818094.4 | TACTILE INPUT DEVICE, MICROPROCESSOR SYSTEM AND |

METHOD FOR CONTROLLING A TACTILE INPUT

| FREESCALE SEMICONDUCTOR, INC. | EP | 10819201.4 | SEMICONDUCTOR DEVICE WITH OXYGEN-DIFFUSION BARRIER LAYER AND METHOD FOR FABRICATING SAME |
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| FREESCALE SEMICONDUCTOR, INC. | EP | 10820978.4 | CAPACITIVE TOUCH SENSOR DEVICE CONFIGURATION SYSTEMS AND METHODS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10825377.4 | SEMICONDUCTOR WAFER HAVING SCRIBE LANE ALIGNMENT MARKS FOR REDUCING CRACK PROPAGATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10830402.3 | ONE-TIME PROGRAMMABLE MEMORY DEVICE AND METHODS THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10831941.9 | MEMORY DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10831984.9 | METHODS AND APPARATUS FOR PERFORMING CAPACITIVE TOUCH SENSING AND PROXIMITY DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10831985.6 | SYSTEMS AND METHODS FOR DELIVERING POWER IN RESPONSE TO A CONNECTION EVENT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10843791.4 | A NETWORK ELEMENT, TELECOMMUNICATION SYSTEM, INTEGRATED CIRCUIT AND A METHOD FOR PROVIDING A TELEPHONY CONNECTION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10845951.2 | BOND PAD WITH MULTIPLE LAYER OVER PAD METALLIZATION AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10846022.1 | DETECTOR AND METHOD FOR DETECTING AN OSCILLATORY SIGNAL AMONG NOISE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10846024.7 | DATA PROCESSING METHOD, DATA PROCESSOR AND APPARATUS INCLUDING A DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10848291.0 | POWER GATING CONTROL MODULE, INTEGRATED CIRCUIT DEVICE, SIGNAL PROCESSING SYSTEM, ELECTRONIC DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10848292.8 | TOKEN BUCKET MANAGEMENT APPARATUS AND METHOD OF MANAGING A TOKEN BUCKET |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10849332.1 | MULTI-CHANNEL SNIFFER SYSTEM AND METHOD FOR MULTI- CHANNEL SNIFFER SYNCHRONIZATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10849762.9 | AUDIO COMMUNICATION DEVICE, METHOD FOR OUTPUTTING AN AUDIO SIGNAL, AND COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10852813.4 | INFORMATION PROCESSING DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10852816.7 | METHOD FOR PROVIDING DATA PROTECTION FOR DATA STORED WITHIN A MEMORY ELEMENT AND INTEGRATED CIRCUIT DEVICE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10854977.5 | DISPLAY CONTROLLING UNIT, IMAGE DISPLAYING SYSTEM AND METHOD FOR OUTPUTTING IMAGE DATA |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10854978.3 | ELECTRONIC CIRCUIT, SAFETY CRITICAL SYSTEM, AND METHOD FOR PROVIDING A RESET SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10854979.1 | CLOCK CIRCUIT FOR PROVIDING AN ELECTRONIC DEVICE WITH A CLOCK SIGNAL, ELECTRONIC DEVICE WITH A CLOCK CIRCUIT AND METHOD FOR PROVIDING AN ELECTRONIC DEVICE WITH A CLOCK SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10855252.2 | LATCH CIRCUIT, FLIP-FLOP CIRCUIT AND FREQUENCY DIVIDER |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10855254.8 | APPARATUS AND METHOD FOR REDUCING PROCESSOR LATENCY |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10856351.1 | VIDEO PROCESSING SYSTEM AND METHOD FOR PARALLEL PROCESSING OF VIDEO DATA |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10856352.9 | PUSH-PUSH OSCILLATOR CIRCUIT |
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| FREESCALE SEMICONDUCTOR, INC. | EP | 10856354.5 | MEMORY MANAGEMENT UNIT FOR A MICROPROCESSOR SYSTEM, MICROPROCESSOR SYSTEM AND METHOD FOR MANAGING MEMORY |
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| FREESCALE SEMICONDUCTOR, INC. | EP | 10858059.8 | LOW-VOLTAGE EXIT DETECTOR, ERROR DETECTOR, LOW- VOLTAGE SAFE CONTROLLER, BROWN-OUT DETECTION METHOD, AND BROWN-OUT SELF-HEALING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10858361.8 | DECODER FOR DETERMINING A SUBSTANCE OR MATERIAL STRUCTURE OF A DETECTED OBJECT BASED ON SIGNALS OF A CAPACTIVE SENSOR AND METHOD FOR DETERMINING A SUBSTANCE OR MATERIAL STRUCTURE OF A DETECTED OBJECT BASED ON SIGNALS ON A CAPACTIVE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10859964.8 | INTEGRATED CIRCUIT DEVICE AND METHOD FOR DETECTING AN EXCESSIVE VOLTAGE STATE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10860036.2 | METHOD FOR ENABLING CALIBRATION DURING START-UP OF A MICRO CONTROLLER UNIT AND INTEGRATED CIRCUIT THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10860038.8 | METHOD FOR BIT RATE CONTROL WITHIN A SCALABLE VIDEO CODING SYSTEM AND SYSTEM THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10860047.9 | METHOD AND APPARATUS FOR MANAGING POWER IN A MULTI-CORE PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 10860114.7 | AN INTEGRATED CIRCUIT AND A METHOD OF POWER MANAGEMENT OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11167376.0 | VIDEO PROCESSING SYSTEM, COMPUTER PROGRAM PRODUCT AND METHOD FOR DECODING AN ENCODED VIDEO STREAM |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11167377.8 | VIDEO PROCESSING SYSTEM, COMPUTER PROGRAM PRODUCT AND METHOD FOR MANAGING A TRANSFER OF INFORMATION BETWEEN A MEMORY UNIT AND A DECODER |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11170004.3 | BATTERY CELL EQUALIZER SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11170039.9 | CURRENT REDUCTION IN A SINGLE STAGE CYCLIC ANALOG TO DIGITAL CONVERTER WITH VARIABLE RESOLUTION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11170299.9 | MEMORY WITH LOW VOLTAGE MODE OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11170583.6 | ANALOG-TO-DIGITAL CONVERTER HAVING A SINGLE SET OF COMPARATORS FOR A MULTI-STAGE SAMPLING CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11176316.5 | MEMS PRESSURE SENSOR DEVICE AND METHOD OF FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11176611.9 | PATTERNING A GATE STACK OF A NON-VOLATILE MEMORY (NVM) WITH SIMULTANEOUS ETCH IN NON-NVM AREA |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11176623.4 | CHARGE PUMP HAVING RAMP RATE CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11177484.0 | DATA PROCESSOR FOR PROCESSING DECORATED INSTRUCTIONS WITH CACHE BYPASS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11184861.0 | METHOD OF MAKING A MICRO-ELECTRO-MECHANICAL- SYSTEMS (MEMS) DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11185418.8 | AREA-EFFICIENT HIGH VOLTAGE BIPOLAR-BASED ESD PROTECTION TARGETING NARROW DESIGN WINDOWS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11185452.7 | INTEGRATED ANTENNA PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11188965.5 | AUTOMOTIVE RADAR SYSTEM AND METHOD FOR USING |

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| FREESCALE SEMICONDUCTOR, INC. | EP | 11733213.0 | NON-VOLATILE MEMORY DEVICE AND METHOD THEREFOR |
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| FREESCALE SEMICONDUCTOR, INC. | EP | 11737455.3 | DATA PROCESSING SYSTEM HAVING BROWN-OUT DETECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11737456.1 | QUIESCENT CURRENT (IDDQ) INDICATION AND TESTING APPARATUS AND METHODS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11754552.5 | OVERCURRENT PROTECTION DEVICE AND METHOD OF OPERATING A POWER SWITCH |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11754553.3 | OVERCURRENT PROTECTION DEVICE AND METHOD OF OPERATING A POWER SWITCH |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11766306.2 | SEMICONDUCTOR DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11777760.7 | OPEN CIRCUIT DETECTOR AND METHOD THEREFORE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11777773.0 | OVERVOLTAGE PROTECTION CIRCUIT FOR AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11787069.1 | DATA PROCESSOR HAVING MULTIPLE LOW POWER MODES |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11796147.4 | SWITCHING REGULATOR WITH INPUT CURRENT LIMITING CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11807201.6 | TRANSMISSION GATE CIRCUITRY FOR HIGH VOLTAGE TERMINAL |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11854624.1 | INTEGRATED CIRCUIT DEVICE AND METHOD FOR PERFORMING CONDITIONAL NEGATION OF DATA |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11855941.8 | INTEGRATED CIRCUIT DEVICE AND METHOD FOR CALCULATING A PREDICATE VALUE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11856370.9 | PHASED-ARRAY RECEIVER, RADAR SYSTEM AND VEHICLE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11856420.2 | DEVICE AND METHOD FOR COMPUTING A FUNCTION VALUE OF A FUNCTION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11857416.9 | SEMICONDUCTOR DEVICE AND RELATED FABRICATION METHODS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11857657.8 | INTEGRATED CIRCUIT DEVICE, VOLTAGE REGULATION CIRCUITRY AND METHOD FOR REGULATING A VOLTAGE SUPPLY SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | EP | 11858080.2 | INTEGRATED CIRCUIT DEVICE, POWER MANAGEMENT MODULE AND METHOD FOR PROVIDING POWER MANAGEMENT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12151623.1 | MEMS SENSOR WITH DUAL PROOF MASSES |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12151630.6 | MEMS SENSOR WITH FOLDED TORSION SPRINGS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12151635.5 | IN-LINE REGISTER FILE BITCELL |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12151640.5 | METHOD AND APPARATUS FOR PROCESSING TEMPORAL AND SPATIAL OVERLAPPING UPDATES FOR AN ELECTRONIC DISPLAY |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12151642.1 | MULTIPLE FUNCTION POWER DOMAIN LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12154159.3 | MEMS DEVICE ASSEMBLY AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12154237.7 | DIGITAL METHOD TO OBTAIN THE I-V CURVES OF NVM BITCELLS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12154277.3 | VIAS BETWEEN CONDUCTIVE LAYERS TO IMPROVE RELIABILITY |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12154287.2 | MEMS DEVICE HAVING VARIABLE GAP WIDTH AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12159924.5 | SYNCHRONOUS DATA PROCESSING SYSTEM AND METHOD |

| FREESCALE SEMICONDUCTOR, INC. | EP | 12159961.7 | MEMORY CONTROLLER ADDRESS AND DATA PIN MULTIPLEXING |
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| FREESCALE SEMICONDUCTOR, INC. | EP | 12160380.7 | SELECTABLE THRESHOLD RESET CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12162868.9 | MEMS DEVICE WITH CENTRAL ANCHOR FOR STRESS ISOLATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12164037.9 | CACHE MEMORY WITH DYNAMIC LOCKSTEP SUPPORT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12164961.0 | SELECTIVE ROUTING OF LOCAL MEMORY ACCESSES AND DEVICE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12169620.7 | DUAL PORT PRESSURE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12169865.8 | ACTIVE TILING PLACEMENT FOR IMPROVED LATCH-UP IMMUNITY |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12170078.5 | METHOD AND APPARATUS FOR GENERATING GATE-LEVEL ACTIVITY DATA FOR USE IN CLOCK GATING EFFICIENCY ANALYSIS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12174843.8 | COMBINED OUTPUT BUFFER AND ESD DIODE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12174973.3 | FUSED BUSS FOR PLATING FEATURES ON A SEMICONDUCTOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12175266.1 | CONFIGURABLE CONTINUOUS TIME SIGMA DELTA ANALOG- TO-DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12179289.9 | SEMICONDUCTOR DEVICE PACKAGING HAVING PRE- ENCAPSULATION THROUGH VIA FORMATION USING LEAD FRAMES WITH ATTACHED SIGNAL CONDUITS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12179294.9 | SEMICONDUCTOR DEVICE WITH WAKE-UP UNIT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12179305.3 | MOSFET MISMATCH CHARACTERIZATION CIRCUIT |
| REESCALE SEMICONDUCTOR, INC. | EP | 12180251.6 | INCIDENT CAPACITIVE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12180259.9 | MEMORY MANAGEMENT UNIT (MMU) HAVING REGION DESCRIPTOR GLOBALIZATION CONTROLS AND METHOD OF OEPRATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12180945.3 | METHOD OF MAKING A SEMICONDUCTOR DEVICE, AND SEMICONDUCTOR DEVICE MADE THEREBY |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12185914.4 | VOLTAGE-CONTROLLED OSCILLATORS AND RELATED SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12185932.6 | INTERFACE SYSTEM AND METHOD WITH BACKWARD COMPATABILITY |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12185946.6 | METHODS AND APPARATUS FOR TESTING MULTIPLE-IC DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12186133.0 | ROTARY DISK GYROSCOPE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12186147.0 | STACKED SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12186166.0 | STACKED SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12187977.9 | SYSTEMS AND METHODS FOR SEMAPHORE-BASED PROTECTION OF SHARED SYSTEM RESOURCES |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12189879.5 | SEMICONDUCTOR DEVICE AND APPARATUS INCLUDING SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12191704.1 | A METHOD OF DECODING A RECEIVED SC-FDMA SYMBOL IN A RECEIVER IN A OFDM COMMUNICATION SYSTEM, A RECEIVER, AN APPARATUS, AN OFDM COMMUNICATION SYSTEM AND A COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12193879.9 | METHOD AND APPARATUS FOR NETWORK STREAMING |
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| FREESCALE SEMICONDUCTOR, INC. | EP | 12194444.1 | METHOD AND SYSTEM FOR PROCESSING DATA FLOWS |
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| FREESCALE SEMICONDUCTOR, INC. | EP | 12194468.0 | PACKAGED LEADLESS SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12194494.6 | WIRELESS COMMUNICATION DEVICE AND SEMICONDUCTOR PACKAGE DEVICE HAVING A POWER AMPLIFIER THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12194503.4 | METHOD AND APPARATUS FOR RESETTING AT LEAST ONE NODE WITHIN A CPRI RADIO BASE STATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | EP | 12196094.2 | EXTENDABLE-ARM ANTENNAS, AND MODULES AND SYSTEMS IN WHICH THEY ARE INCORPORATED |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13150356.7 | SYSTEM AND METHOD FOR PROCESSING DATA FLOWS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13150503.4 | CHANNEL ESTIMATION IN WIRELESS COMMUNICATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13150825.1 | PIPELINED ANALOG-TO-DIGITAL CONVERTER HAVING REDUCED POWER CONSUMPTION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13151698.1 | STRUCTURE AND METHOD FOR HEALING TUNNEL DIELECTRIC OF NON-VOLATILE MEMORY CELLS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13151789.8 | SEMICOCNDUCTOR DEVICE HAVING DIFFERENT NON- VOLATILE MEMORIES HAVING NANOCRYSTALS OF DIFFERING DENSITIES AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13151793.0 | A DELAY LINE PHASE SHIFTER WITH SELECTABLE PHASE SHIFT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13151802.9 | AN ADJUSTABLE POWER SPLITTER AND CORRESPONDING METHODS AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13151813.6 | ENCAPSULANT WITH COROSION INHIBITOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13151824.3 | METHOD FOR FORMING DIE ASSEMBLY WITH HEAT SPREADER |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13155182.2 | METHOD FOR IMPLEMENTING SECURITY OF NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13160459.7 | RANDOM VALUE PRODUCTION METHODS AND SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13161733.4 | MICROWAVE ADAPTORS AND RELATED OSCILLATOR SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13161832.4 | WRITE CONTENTION-FREE, NOISE-TOLERANT MULTIPORT BITCELL |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13161836.5 | LOGIC TRANSISTOR AND NON-VOLATILE MEMORY CELL INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13161838.1 | RERAM DEVICE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13161840.7 | Sharing Stacked BJT Clamps for System Level ESD Protection |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13161848.0 | SAMPLE AND HOLD CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13161850.6 | ERASING A NON-VOLATILE MEMORY (NVM) SYSTEM HAVING ERROR CORRECTION CODE (ECC) |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13167454.1 | MULTICHANNEL RECEIVER SYSTEM AND METHOD FOR MULTICHANNEL RECEIVER MONITORING |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13167459.0 | MULTICHANNEL RECEIVER SYSTEM AND METHOD FOR MULTICHANNEL RECEIVER MONITORING |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13169490.3 | INTEGRATED CIRCUIT DIE ASSEMBLY WITH HEAT SPREADER |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13169521.5 | PROCESSOR RESOURCE AND EXECUTION PROTECTION |

METHODS AND APPARATUS

| FREESCALE SEMICONDUCTOR, INC. | EP | 13169541.3 | STRESS-BASED TECHNIQUES FOR DETECTING AN IMMINENT READFAILURE IN A NON-VOLATILE MEMORY ARRAY |
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| FREESCALE SEMICONDUCTOR, INC. | EP | 13169553.8 | CLOCKED MEMORY WITH WORD LINE ACTIVATION DURING A FIRST PORTION OF THE CLOCK CYCLE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13169562.9 | CLOCKED MEMORY WITH LATCHING PREDECODER CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13169572.8 | VRS INTERFACE WITH 1/T ARMING FUNCTION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13169578.5 | SENSING DEVICE AND RELATED OPERATING METHODS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13169583.5 | Synchronous Rectifier Timer for Discontinuous Mode DC/DC Converter |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13172863.6 | FILM-ASSIST MOLDED GEL-FILL CAVITY PACKAGE WITH OVERFLOW RESERVOIR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13172879.2 | POWER TRANSISTOR WITH HEAT DISSIPATION AND METHOD THEREFORE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13172894.1 | SEMICONDUCTOR DEVICE AND DRIVER CIRCUIT WITH A CURRENT CARRYING REGION AND ISOLATION STRUCTURE INTERCONNECTED THROUGH A RESISTOR CIRCUIT, AND METHOD OF MANUFACTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13173216.6 | DEVICE PACKAGE WITH RIGID INTERCONNECT STRUCTURE CONNECTING DIE AND SUBSTRATE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13173226.5 | SEMICONDUCTOR DEVICE AND DRIVER CIRCUIT WITH DRAIN AND ISOLATION STRUCTURE INTERCONNECTED THROUGH A DIODE CIRCUIT, AND METHOD OF MANUFACTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13173238.0 | Sensor Package and Method of Forming Same |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13173268.7 | SEMICONDUCTOR DEVICE PACKAGE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13173277.8 | HIGH BREAKDOWN VOLTAGE LDMOS DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13173286.9 | Angular Rate Sensor With Quadrature Error Compensation |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13177131.3 | METHODS AND SYSTEMS FOR ADJUSTING NVM CELL BIAS CONDITIONS BASED UPON OPERATING TEMPERATURE TO REDUCE PERFORMANCE DEGRADATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13177161.0 | METHODS AND SYSTEMS FOR ADJUSTING NVM CELL BIAS CONDITIONS FOR PROGRAM/ERASE OPERATIONS TO REDUCE PERFORMANCE DEGRADATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13177186.7 | CAPACITIVE PRESSURE SENSOR IN AN OVERMOLDED PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13177826.8 | RERAM DEVICE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13178058.7 | VARIABLE RELUCTANCE SENSOR INTERFACE WITH INTEGRATION BASED ARMING THRESHOLD |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13179520.5 | STACKED MICROELECTRONIC PACKAGES HAVING SIDEWALL CONDUCTORS AND METHODS FOR THE FABRICATION THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13179539.5 | LOW DROPOUT VOLTAGE REGULATOR WITH A FLOATING VOLTAGE REFERENCE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13179559.3 | ADAPTIVE ERROR CORRECTION FOR NON-VOLATILE MEMORIES |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13179567.6 | NON-VOLATILE MEMORY (NVM) THAT USES SOFT PROGRAMMING |
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| FREESCALE SEMICONDUCTOR, INC. | EP | 13179577.5 | PRESSURE SENSOR WITH DIFFERENTIAL CAPACITIVE OUTPUT |
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| FREESCALE SEMICONDUCTOR, INC. | EP | 13179590.8 | LEADFRAMES, AIR-CAVITY PACKAGES, AND ELECTRONIC DEVICES WITH OFFSET VENT HOLES, AND METHODS OF THEIR MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13180554.1 | TRANSDUCER-INCLUDING DEVICES, AND METHODS AND APPARATUS FOR THEIR CALIBRATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13183320.4 | SEMICONDUCTOR DEVICES WITH IMPEDANCE MATCHING CIRCUITS, AND METHODS OF MANUFACTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13183355.0 | QUIESCENT CURRENT DETERMINATION USING IN-PACKAGE VOLTAGE MEASUREMENTS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13183374.1 | Matrix Lid Heatspreader for Flip Chip Package |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13183405.3 | NON-VOLATILE MEMORY (NVM) WITH ADAPTIVE WRITE OPERATIONS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13183411.1 | SYSTEMS AND METHODS FOR CODE PROTECTION IN NON-VOLATILE MEMORY SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13183417.8 | NVM WITH CHARGE PUMP AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13184575.2 | VOLTAGE TRANSLATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13184837.6 | THERMAL SENSOR SYSTEM AND METHOD BASED ON CURRENT RATIO |
| FREESCALE SEMICONDUCTOR, INC. | EP | 13275126.4 | VEHICLE-BORNE RADAR SYSTEMS WITH CONTINUOUS-TIME, SIGMA DELTA ANALOG-TO-DIGITAL CONVERTERS, AND METHODS OF THEIR OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | EP | 94109689.3 | METHOD AND STRUCTURE FOR FORMING AN INTEGRATED CIRCUIT PATTE RN ON A SEMICONDUCTOR SUBSTRAT E |
| FREESCALE SEMICONDUCTOR, INC. | EP | 99118540.6 | PROGRAMMABLE DELAY CONTROL IN A MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | FR | 02729351.3 | COMPONENT WITH FILTER AND METHOD OF MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | FR | 04810477.2 | APPARATUS AND METHOD FOR TIME ORDERING EVENTS IN A SYSTEM HAVING MULTIPLE TIME DOMAINS |
| FREESCALE SEMICONDUCTOR, INC. | FR | 09787356.6 | WIRELESS COMMUNICATION DEVICE AND SEMICONDUCTOR PACKAGE DEVICE HAVING A POWER AMPLIFIER THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | FR | 09803305.3 | BRANCH TARGET BUFFER ALLOCATION |
| FREESCALE SEMICONDUCTOR, INC. | FR | 09846744.2 | MULTICHANNEL RECEIVER SYSTEM AND METHOD FOR MULTICHANNEL RECEIVER MONITORING |
| FREESCALE SEMICONDUCTOR, INC. | FR | 10712502.3 | CHIP DAMAGE DETECTION DEVICES FOR A SEMICONDUCTOR INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | GB | 0325852.2 | METHOD AND DEVICE FOR DERIVING A PREDISTORTED SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | GB | 02729351.3 | COMPONENT WITH FILTER AND METHOD OF MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | GB | 04810477.2 | APPARATUS AND METHOD FOR TIME ORDERING EVENTS IN A SYSTEM HAVING MULTIPLE TIME DOMAINS |
| FREESCALE SEMICONDUCTOR, INC. | GB | 08713946.5 | MULTI-LAYER SOURCE/DRAIN STRESSOR |
| FREESCALE SEMICONDUCTOR, INC. | GB | 09787356.6 | WIRELESS COMMUNICATION DEVICE AND SEMICONDUCTOR PACKAGE DEVICE HAVING A POWER AMPLIFIER THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | GB | 09803305.3 | BRANCH TARGET BUFFER ALLOCATION |

| FREESCALE SEMICONDUCTOR, INC. | GB | 09846744.2 | MULTICHANNEL RECEIVER SYSTEM AND METHOD FOR MULTICHANNEL RECEIVER MONITORING |
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| FREESCALE SEMICONDUCTOR, INC. | GB | 10712502.3 | CHIP DAMAGE DETECTION DEVICES FOR A SEMICONDUCTOR INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | IN | 0681/DEL/2005 | DIGITAL CLOCK FREQUENCY DOUBLER |
| FREESCALE SEMICONDUCTOR, INC. | IN | 0819/DEL/2005 | TRANSMISSION LINE DRIVER |
| FREESCALE SEMICONDUCTOR, INC. | IN | 1044/DELNP/2008 | MULTI-THREADED PROCESSOR ARCHITECTURE |
| FREESCALE SEMICONDUCTOR, INC. | IN | 1046/DELNP/2008 | SEMICONDUCTOR STACKED DIE/WAFER CONFIGURATION AND PACKAGING AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | IN | 108/DEL/2007 | METHOD FOR FABRICATING A PCB |
| FREESCALE SEMICONDUCTOR, INC. | IN | 109/DEL/2007 | METHOD OF PACKAGING SEMICONDUCTOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | IN | 1098/DEL/2006 | METHOD AND SYSTEM FOR INCORPORATING VIA REDUNDANCY IN TIMING ANALYSIS |
| FREESCALE SEMICONDUCTOR, INC. | IN | 1124/DEL/2006 | CLOCK BALANCING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | IN | 1254/DELNP/2009 | ONE TRANSISTOR DRAM CELL STRUCTURE AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | IN | 1297/DELNP/2008 | METHOD AND SYSTEM FOR ACKNOWLEDGING FRAMES IN A COMMMUNICATION NETWORK |
| FREESCALE SEMICONDUCTOR, INC. | IN | 1373/DEL/2005 | CHARGE PUMP CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | IN | 1394/DEL/2005 | TRANSMISSION LINE DRIVER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | IN | 1404/DEL/2005 | DIFFERENTIAL RECEIVER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | IN | 1498/DELNP/2009 | METHOD OF PACKAGING A SEMICONDUCTOR DEVICE AND A PREFABRICATED CONNECTOR |
| FREESCALE SEMICONDUCTOR, INC. | IN | 1545/DELNP/2009 | METHOD OF MAKING A CONTACT ON A BACKSIDE OF A DIE |
| FREESCALE SEMICONDUCTOR, INC. | IN | 156/DEL/2009 | VIA DEFINITION FOR SEMICONDUCTOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | IN | 1669/DEL/2005 | METHOD AND SYSTEM FOR REDUCING DELAY NOISE IN AN IC |
| FREESCALE SEMICONDUCTOR, INC. | IN | 1913/DEL/2005 | CLOCK GENERATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | IN | 192/DEL/2007 | METHOD AND SYSTEM FOR ESTIMATING POWER CONSUMPTION OF INTEGRATED CIRCUIT DESIGN |
| FREESCALE SEMICONDUCTOR, INC. | IN | 192/DEL/2011 | ESTIMATION AND COMPENSATION OF CLOCK VARIATION IN RECEIVED SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | IN | 1925/DEL/2005 | PVT VARIATION DETECTION AND COMPENSATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | IN | 1926/DEL/2005 | PVT VARIATION DETECTION AND COMPENSATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | IN | 1928/DEL/2005 | PVT VARIATION DETECTION AND COMPENSATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | IN | 2125/DEL/2006 | METHOD AND SYSTEM OF EXECUTING A SOFTWARE APPLICATION IN HIGHLY CONSTRAINED MEMORY SITUATION |
| FREESCALE SEMICONDUCTOR, INC. | IN | 2170/DEL/2006 | SYSTEM AND METHOD FOR MONITORING CLOCK SIGNAL IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | IN | 2189/DELNP/2008 | SIGNAL CONVERTERS WITH MULTIPLE GATE DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | IN | 2211/DEL/2006 | SYSTEM AND METHOD FOR REDUCING POWER CONSUMPTION IN A LOW-DENSITY PARITY-CHECK (LDPC) |

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| FREESCALE SEMICONDUCTOR, INC. | IN | 2262/DEL/2006 | MILLER CAPACITANCE TOLERANT BUFFER ELEMENT |
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| FREESCALE SEMICONDUCTOR, INC. | IN | 2263/DEL/2006 | SYSTEM AND METHOD FOR TESTING MEMORY BLOCKS IN AN SOC DESIGN |
| FREESCALE SEMICONDUCTOR, INC. | IN | 2306/DELNP/2007 | METHOD FOR SHARING BANDWIDTH USING REDUCED DUTY CYCLE SIGNALS |
| FREESCALE SEMICONDUCTOR, INC. | IN | 2307/DELNP/2007 | SYSTEM AND METHOD FOR FALL DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | IN | 2308/DELNP/2007 | METHOD OF FORMING A SEMICONDUCTOR PACKAGE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | IN | 231/DEL/2009 | METHOD OF READING MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | IN | 235/DEL/2007 | METHOD AND SYSTEM FOR MANAGING COMMUNICATIONS BETWEEN SUB-SYSTEMS OF A COMMUNICATION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | IN | 2374/DEL/2006 | LOW VOLTAGE LOW POWER CLASS A/B OUTPUT STAGE |
| FREESCALE SEMICONDUCTOR, INC. | IN | 2432/DEL/2008 | STANDBY CONTROL CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | IN | 2477/DEL/2009 | MEMORY DEVICE AND SENSE CIRCUITRY THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | IN | 248/DELNP/2006 | DATA PROCESSING SYSTEM IMPLEMENTING SIMD OPERATIONS AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | IN | 2485/DEL/2008 | LOW POWER SELF-GATED, PULSE TRIGGERED CLOCK GATING CELL |
| FREESCALE SEMICONDUCTOR, INC. | IN | 2487/DELNP/2009 | METHOD OF MAKING A NON-VOLATILE MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | IN | 2538/DEL/2006 | METHOD AND SYSTEM FOR DESIGNING TEST CIRCUIT IN A SYSTEM ON CHIP |
| FREESCALE SEMICONDUCTOR, INC. | IN | 2636/DEL/2005 | SEQUENCE-INDEPENDENT POWER-ON RESET FOR MULTIVOLTAGE CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | IN | 2689/DEL/2005 | DIGITAL CLOCK FREQUENCY MULTIPLIER |
| FREESCALE SEMICONDUCTOR, INC. | IN | 2848/DELNP/2008 | ELECTRONIC ASSEMBLY HAVING GRADED WIRE BONDING |
| FREESCALE SEMICONDUCTOR, INC. | IN | 29/DEL/2006 | SCAN CELL FOR AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | IN | 3020/DELNP/2008 | SYSTEM AND METHOD FOR CONTROLLING THE TRANSMIT POWER OF A WIRELESS MODULE |
| FREESCALE SEMICONDUCTOR, INC. | IN | 3028/DELNP/2007 | PACKAGED DEVICE AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | IN | 304/DEL/2009 | READ ONLY MEMORY AND METHOD OF READING SAME |
| FREESCALE SEMICONDUCTOR, INC. | IN | 3193/DELNP2006 | LOW IF RADIO RECEIVER |
| FREESCALE SEMICONDUCTOR, INC. | IN | 3309/DELNP/2006 | LAND GRID ARRAY PACKAGED DEVICE AND METHOD OF FORMING SAME |
| FREESCALE SEMICONDUCTOR, INC. | IN | 3342/DEL/2005 | METHOD FOR ESTIMATING PROCESSOR ENERGY USAGE |
| FREESCALE SEMICONDUCTOR, INC. | IN | 3574/DELNP/2010 | ELECTRONIC ASSEMBLY MANUFACTURING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | IN | 364/DELNP/2008 | SYSTEM AND METHOD FOR ADJUSTING ACQUISITION PHASE |
| FREESCALE SEMICONDUCTOR, INC. | IN | 4442/DELNP/2009 | MICROELECTRONIC ASSEMBLY WITH IMPROVED ISOLATION VOLTAGE PERFORMANCE AND A METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | IN | 5053/DELNP/2005 | METHOD AND APPARATUS FOR DYNAMIC PREFETCH BUFFER CONFIGURATION AND REPLACEMENT |
| FREESCALE SEMICONDUCTOR, INC. | IN | 5182/DELNP/2008 | WARPAGE-REDUCING PACKAGING DESIGN |
| FREESCALE SEMICONDUCTOR, INC. | IN | 5313/DELNP/2005 | METHOD AND APPARATUS FOR SELECTING CACHE WAYS AVAILABLE FOR REPLACEMENT |

WAYS AVAILABLE FOR REPLACEMENT

| FREESCALE SEMICONDUCTOR, INC. FREESCALE SEMICONDUCTOR, INC. FREESCALE SEMICONDUCTOR, INC. FREESCALE SEMICONDUCTOR, INC. | IN IN IN IN | 5478/DELNP/2008 5757/DELNP/2008 5974/DELNP/2008 650/DELNP/2009 | SYSTEM AND METHOD FOR FAST MOTION ESTIMATION BIT LINE PRECHARGE IN EMBEDDED MEMORY METHOD AND APPARATUS FOR A STEPPED-DRIFT MOSFET |
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| FREESCALE SEMICONDUCTOR, INC. | IN IN | 5974/DELNP/2008 | METHOD AND APPARATUS FOR A STEPPED-DRIFT |
| | IN | | |
| FREESCALE SEMICONDUCTOR, INC. | | 650/DELNP/2009 | |
| | IN | 200 | VIDEO INFORMATION PROCESSING SYSTEM WITH SELECTIVE CHROMA DEBLOCK FILTERING |
| FREESCALE SEMICONDUCTOR, INC. | 113 | 6651/DELNP/2008 | SEMICONDUCTOR DEVICE AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | IN | 6705/DELNP/2009 | THREAD DE-EMPHASIS INSTRUCTION FOR MULTITHREADED PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | IN | 682/DEL/2005 | CLOCK DELAY COMPENSATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | IN | 7143/DELNP/2008 | METHOD OF MAKING A MULTIPLE CRYSTAL ORIENTATION SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | IN | 7344/DELNP/2008 | LEAD FRAME BASED, OVER-MOLDED SEMICONDUCTOR PACKAGE WITH INTEGRATED THROUGH HOLE TECHNOLOGY (THT) HEAT SPREADER PIN(S) AND ASSOCIATED METHOD OF MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | IN | 7703/DELNP/2007 | INTEGRATED CIRCUIT WITH IMPROVED SIGNAL NOISI ISOLATION AND METHOD FOR IMPROVING SIGNAL NOISE ISOLATION |
| FREESCALE SEMICONDUCTOR, INC. | IN | 7751/DELNP/2008 | STRESSOR INTEGRATION AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | IN | 79/DEL/2009 | FLIP-FLOP CIRCUIT WITH INTERNAL LEVEL SHIFTER |
| FREESCALE SEMICONDUCTOR, INC. | IN | 7967/DELNP/2006 | MULTYLAYER CAVITY SLOT ANTENNA |
| FREESCALE SEMICONDUCTOR, INC. | IN | 7968/DELNP/2006 | RECESSED SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | IN | 8/DEL/2007 | SHORT CIRCUIT AND OVER-VOLTAGE PROTECTION FOR A DATA BUS |
| FREESCALE SEMICONDUCTOR, INC. | IN | 8122/DELNP/2010 | METHOD AND CIRCUIT FOR EFUSE PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | IN | 821/DEL/2010 | METHOD FOR REDUCING SURFACE AREA OF PAD LIMITED SEMICONDUCTOR DIE LAYOUT |
| FREESCALE SEMICONDUCTOR, INC. | IN | 938/DEL/2006 | METHOD OF DETERMINING A SYNCHRONOUS PHASE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2000-201009 | STRESS COMPENSATION COMPOSITION AND SEMICONDUCTOR COMPONENT FORMED USING THE STRESS COMPENSATION COMPOSITION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2000-289730 | FILTER APPARATUS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2002-577647 | LITHOGRAPHIC TEMPLATE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2006-321047 | METHOD FOR PACKAGING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2007-326329 | RAIL TO RAIL BUFFER AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2007-500763 | SEMICONDUCTOR PACKAGE WITH CROSSING CONDUCTOR ASSEMBLY AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2007-519216 | ULTRA-THIN DIE AND METHOD OF FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2008-118358 | METHOD AND CIRCUIT FOR GENERATING OUTPUT VOLTAGES FROM INPUT VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2008-118360 | METHOD AND CIRCUIT FOR REDUCING REGULATOR OUTPUT NOISE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2008-138177 | OUTPUT CORRECTION CIRCUIT FOR THREE-AXIS ACCELEROMETER |

| FREESCALE SEMICONDUCTOR, INC. | JP | 2008-537752 | A METHOD OF MAKING AN INVERTED-T CHANNEL TRANSISTOR |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 2008-542309 | LATERALLY GROWN NANOTUBES AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2008-545893 | SEMICONDUCTOR DEVICE HAVING STRESSORS AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2008-545900 | TRANSISTOR WITH IMMERSED CONTACTS AND METHODS OF FORMING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2008-554454 | METHOD AND APPARATUS FOR FORMING A SEMICONDUCTOR- ON-INSULATOR (SOI) BODY-CONTACTED DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2008-555430 | METHOD AND APPARATUS FOR TESTING A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2008-556487 | METHOD AND APPARATUS FOR INDICATING DIRECTIONALITY IN INTEGRATED CIRCUIT MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2009-024785 | PULSE WIDTH MODULATION CIRCUIT, PULSE WIDTH MODULATION METHOD, AND REGULATOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2009-028928 | METHOD FOR MANUFACTURING SEMICONDUCTOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2009-072564 | CURRENT DRIVE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2009-112158 | DRIVER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2009-504367 | LEAD FRAME BASED, OVER-MOLDED SEMICONDUCTOR PACKAGE WITH INTEGRATED THROUGH HOLE TECHNOLOGY (THT) HEAT SPREADER PIN(S) AND ASSOCIATED METHOD OF MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2009-51205 | SELF-CALIBRATING OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2009-512193 | CONTACT SURROUNDED BY PASSIVATION AND POLYIMIDE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2009-513348 | DIE LEVEL METAL DENSITY GRADIENT FOR IMPROVED FLIP CHIP PACKAGE RELIABILITY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2009-517460 | ELECTROSTATIC DISCHARGE PROTECTION APPARATUS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2009-532490 | SENSOR HAVING FREE FALL SELF-TEST CAPABILITY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2009-537251 | TWO-PORT SRAM HAVING IMPROVED WRITE OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2009-537253 | METHOD OF MAKING A CONTACT ON A BACKSIDE OF A DIE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2009-544874 | FORMING A SEMICONDUCTOR DEVICE HAVING A METAL ELECTRODE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2009-546386 | DIFFERENTIAL CAPACITIVE SENSOR AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2009-547344 | METHOD OF MAKING A SEMICONDUCTOR DEVICE HAVING HIGH VOLTAGE TRANSISTORS, NON-VOLATILE MEMORY TRANSISTORS, AND LOGIC TRANSISTORS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2009-549654 | MULTI-LAYER SOURCE/DRAIN STRESSOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2009-551780 | SOURCE/DRAIN STRESSOR AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2009-552003 | MICROELECTRONIC ASSEMBLY WITH IMPROVED ISOLATION VOLTAGE PERFORMANCE AND A METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2009-552780 | SYSTEM AND METHOD FOR TESTING AND PROVIDING AN INTEGRATED CIRCUIT HAVING MULTIPLE MODULES OR SUBMODULES |

SUBMODULES

| FREESCALE SEMICONDUCTOR, INC. | JP 2009-5527 | 82 TRENCH FORMATION IN A SEMICONDUCTOR MATERIAL |
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| FREESCALE SEMICONDUCTOR, INC. | JP 2009-5536 | ELECTRONIC DEVICE INCLUDING CHANNEL REGIONS LYING AT DIFFERENT ELEVATIONS AND PROCESSES OF FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-1131 | OBJECT DETECTOR INCLUDING ELECTRIC FIELD MEASUREMENT FUNCTION HAVING VARIABLE SENSITIVITY |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-1819 | 54 SEMICONDUCTOR DEVICE HAVING A BOND PAD AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5021 | 76 A FIRST INTER-LAYER DIELECTRIC STACK FOR NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5075 | 23 THREAD DE-EMPHASIS INSTRUCTION FOR MULTITHREADED PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5112 | 40 ONE TIME PROGRAMMABLE ELEMENT SYSTEM IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5156 | 55 HETERO-STRUCTURE FIELD EFFECT TRANSISTOR, INTEGRATED CIRCUIT INCLUDING A HETERO-STRUCTURE FIELD EFFECT TRANSISTOR AND METHOD FOR MANUFACTURING A HETERO-STRUCTURE FIELD EFFECT TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5170 | 37 DYNAMIC VOLTAGE ADJUSTMENT FOR MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5200 | 25 SYMMETRICAL DIFFERENTIAL CAPACITIVE SENSOR AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5229 | 93 INTERCONNECT IN A MULTI-ELEMENT PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5229 | 98 RF CIRCUIT WITH CONTROL UNIT TO REDUCE SIGNAL POWER UNDER APPROPRIATE CONDITIONS |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5240 | 70 DUAL GATE OXIDE DEVICE INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5269 | 84 SYSTEM AND METHOD FOR MONITORING DEBUG EVENTS |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5269 | 85 PHASE CHANGE MEMORY STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5280 | 16 PROGRAMMABLE ROM USING TWO BONDED STRATA AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5280 | 26 CLOCK CIRCUIT WITH CLOCK TRANSFER CAPABILITY AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-53110 | METHOD FOR INTEGRATING NVM CIRCUITRY WITH LOGIC CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5369 | 74 ERROR DETECTOR IN A CACHE MEMORY USING CONFIGURABLE WAY REDUNDANCY |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5407 | 04 LIQUID LEVEL SENSING DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5407 | 77 ELECTRICAL ERASABLE PROGRAMMABLE MEMORY TRANSCONDUCTANCE TESTING |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5422 | 35 MIGFET CIRCUIT WITH ESD PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5450 | 40 BALUN TRANSFORMER WITH IMPROVED HARMONIC SUPRESSION |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5468 | PERIPHERAL MODULE REGISTER ACCESS METHODS AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5476 | 58 ADJUSTABLE PIPELINE IN A MEMORY CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5507 | 9 READ REFERENCE TECHNIQUE WITH CURRENT DEGRADATION PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | JP 2010-5507 | LED DRIVER WITH DYNAMIC POWER MANAGEMENT |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-1514 | BATTERY CELL EQUALIZER SYSTEM |
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| FREESCALE SEMICONDUCTOR, INC. | JP 2011-15 | 1483 CURRENT REDUCTION IN A SINGLE STAGE CYCLIC ANALOG TO DIGITAL CONVERTER WITH VARIABLE RESOLUTION |
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| FREESCALE SEMICONDUCTOR, INC. | JP 2011-15 | 3682 SOFT PROGRAM OF A NON-VOLATILE MEMORY BLOCK |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-16 | DATA PROCESSING SYSTEM WITH PERIPHAL CONFIGURATION INFORMATION ERROR DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-16 | 7168 POLYMER CORE WIRE |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-16 | 7449 MEMS PRESSURE SENSOR DEVICE AND METHOD OF FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-17 | 4607 SEMICONDUCTOR DEVICE AND PROCESS FOR DESIGNING A MASK |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-18 | MEMS DEVICE ASSEMBLY AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-18 | PATTERNING A GATE STACK OF A NON-VOLATILE MEMORY (NVM) WITH SIMULTANEOUS ETCH IN NON-NVM AREA |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-21 | METHOD OF MAKING A MICRO-ELECTRO-MECHANICAL- SYSTEMS (MEMS) DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-239 | DEBUGGER RECOVERY ON EXIT FROM LOW POWER MODE |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-24 | 7770 AREA-EFFICIENT HIGH VOLTAGE BIPOLAR-BASED ESD PROTECTION TARGETING NARROW DESIGN WINDOWS |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-259 | 9676 AUTOMOTIVE RADAR SYSTEM AND METHOD FOR USING SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-27. | 2993 MEMORY HAVING A LATCHING SENSE AMPLIFIER RESISTANT TO NEGATIVES BIAS TEMPERATURE INSTABILITY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-28 | 2742 VOLTAGE REGULATION CIRCUITRY AND RELATED OPERATING METHODS |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-28 | METHOD AND APPARATUS FOR PROCESSING TEMPORAL AND SPATIAL OVERLAPPING UPDATES FOR AN ELECTRONIC DISPLAY |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-28 | MEMS SENSOR WITH DUAL PROOF MASSES |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-28 | MEMS SENSOR WITH FOLDED TORSION SPRINGS |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-50 | 7495 MULTI-VOLTAGE ELECTROSTATIC DISCHARGE PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-50 | 7496 CACHE COHERENCY PROTOCOL IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-510 | D525 CIRCUIT FOR AND AN ELECTRONIC DEVICE INCLUDING A NONVOLATILE MEMORY CELL AND A PROCESS OF FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-51 | 1659 CAPACITIVE SENSOR WITH STRESS RELIEF THAT COMPENSATES FOR PACKAGE STRESS |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-51 | METHOD FOR ELECTRICALLY TRIMMING AN NVM REFERENCE CELL |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-52 | 1136 SYSTEM AND METHOD FOR FETCHING INFORMATION TO A CACHE MODULE USING A WRITE BACK ALLOCATE ALGORITHM |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-52 | 1137 BRANCH TARGET BUFFER ALLOCATION |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-52 | 1138 SEMICONDUCTOR DEVICES WITH EXTENDED ACTIVE REGIONS |
| FREESCALE SEMICONDUCTOR, INC. | JP 2011-52 | 3841 TRANSISTOR WITH GAIN VARIATION COMPENSATION |
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| DEVICES FREESCALE SEMICONDUCTOR, INC. JP 2011-531051 ADAPTIVE IIP2 CALIBRATION FREESCALE SEMICONDUCTOR, INC. JP 2011-532161 INTERRUPT ACKNOWLEDGMENT IN A DATA PROCESS SYSTEM METHOD OF MAKING A SPLIT GATE MEMORY CELL FREESCALE SEMICONDUCTOR, INC. JP 2011-5334580 TEANSDUCER WITH DECOUPLED SENSING IN MUTUA ORTHOGONAL DIRECTIONS FREESCALE SEMICONDUCTOR, INC. JP 2011-536678 PROGRAMMABLE PERROR ACTIONS FOR A CACHE IN A PROCESSING SYSTEM FREESCALE SEMICONDUCTOR, INC. JP 2011-539600 RF DEVICE AND METHOD WITH TRENCH UNDER BON FEATURE FREESCALE SEMICONDUCTOR, INC. JP 2011-540323 HIGH POWER SEMICONDUCTOR DEVICE FOR WIRELES APPLICATIONS AND METHOD OF FORMING A HIGH PO SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. JP 2011-543626 INTEGRATED CIT. FREESCALE SEMICONDUCTOR, INC. JP 2011-543826 INTEGRATED CIT. FREESCALE SEMICONDUCTOR, INC. JP 2011-548021 DIAL HIGH-K OXIDES WITH SIGE CHANNEL FREESCALE SEMICONDUCTOR, INC. JP 2011-548021 CAPACITANCE-TO-VOLTAGE INTERFACE CIRCUIT, ANI RELATED OPERATION WITH METAL GERMANIUM SILI MATERIAL FREESCALE SEMICONDUCTOR, INC. JP 2011-548021 CAPACITANCE-TO-VOLTAGE INTERFACE CIRCUIT, ANI RELATED OPERATING METHODS FREESCALE SEMICONDUCTOR, INC. JP 2011-548021 CAPACITANCE-TO-VOLTAGE INTERFACE CIRCUIT, ANI RELATED OPERATING METHODS FREESCALE SEMICONDUCTOR, INC. JP 2011-55085 WANDOWN HAVING NEGATIVE VOLTAGE WRITE ASSIST CIRCUITAL AND METHOD THEREFOR FREESCALE SEMICONDUCTOR, INC. JP 2011-55085 VALUE FREESCALE SEMICONDUCTOR, INC. JP 2012-067874 SELECTABLE THRESHOLD RESET CIRCUIT, ANI RELATED OPERATING METHODS FREESCALE SEMICONDUCTOR, INC. JP 2012-067874 SELECTABLE THRESHOLD RESET CIRCUIT FREESCALE SEMICONDUCTOR, INC. JP 2012-067874 SELECTABLE THRESHOLD RESET CIRCUIT FREESCALE SEMICONDUCTOR, INC. JP 2012-067874 SELECTABLE THRESHOLD RESET CIRCUIT FREESCALE SEMICONDUCTOR, INC. JP 2012-067874 | FREESCALE SEMICONDUCTOR, INC. | JP | 2011-526074 | CIRCUIT AND METHOD FOR OPTIMIZING MEMORY SENSE AMPLIFIER TIMING |
| FREESCALE SEMICONDUCTOR, INC. JP 2011-532106 FREESCALE SEMICONDUCTOR, INC. JP 2011-533213 METHOD OF MAKING A SPLIT GATE MEMORY CELL FREESCALE SEMICONDUCTOR, INC. JP 2011-534580 TRANSDUCER WITH DECOUPLED SENSING IN MUTUA ORTHOGONAL DIRECTIONS FREESCALE SEMICONDUCTOR, INC. JP 2011-536378 FROGRAMMABLE ERROR ACTIONS FOR A CACHE IN A PROCESSING SYSTEM FREESCALE SEMICONDUCTOR, INC. JP 2011-539600 RF DEVICE AND METHOD WITH TRENCH UNDER BONJ FEATURE FREESCALE SEMICONDUCTOR, INC. JP 2011-540323 HIGH POWER SEMICONDUCTOR DEVICE FOR WIRELE APPLICATIONS AND METHOD OF FORMING A HIGHE SEMICONDUCTOR DEVICE WITH ISOLATE MICROELECTROMECHANICAL DEVICE MICROELECTROMECHANICAL DEVICE MICROELECTROMECHANICAL DEVICE MICROELECTROMECHANICAL DEVICE MICROELECTROMECHANICAL DEVICE MICROELECTROMECHANICAL MICROELECTROMECHANICAL MICROELECTROMECHANICAL MICROELECTROMECHANICAL MICROELECTROMECH | FREESCALE SEMICONDUCTOR, INC. | JP | 2011-526075 | ADAPTIVE FEEDBACK AND POWER CONTROL FOR USB DEVICES |
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| | FREESCALE SEMICONDUCTOR, INC. | JP | 2012-096894 | SENSOR DEVICE WITH SEALING STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. JP 2012-101072 PHASE LOCKED LOOP CIRCUIT HAVING A VOLTAGE | FREESCALE SEMICONDUCTOR, INC. | JP | 2012-100849 | LOAD CONTROL AND PROTECTION SYSTEM |
| CONTROLLED OSCILLATOR WITH IMPROVED BANDW | FREESCALE SEMICONDUCTOR, INC. | JP | 2012-101072 | PHASE LOCKED LOOP CIRCUIT HAVING A VOLTAGE CONTROLLED OSCILLATOR WITH IMPROVED BANDWIDTH |

| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-101073 | ELECTRICALLY PROGRAMMABLE FUSE MODULE IN SEMICONDUCTOR DEVICE |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-107015 | SELECTIVE ROUTING OF LOCAL MEMORY ACCESSES AND DEVICE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-121443 | DUAL PORT PRESSURE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-125197 | RELAXATION OSCILLATOR WITH LOW POWER CONSUMPTION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-131985 | WRITING DATA TO SYSTEM MEMORY IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-135889 | BRANCH TARGET BUFFER ADDRESSING IN A DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-159145 | FUSED BUSS FOR PLATING FEATURES ON A SEMICONDUCTOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-161149 | COMBINED OUTPUT BUFFER AND ESD DIODE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-167987 | CONFIGURABLE CONTINUOUS TIME SIGMA DELTA ANALOGTO-DIGITAL CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-168421 | ATTACHING A MEMS TO A BONDING WAFER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-169552 | IMPLANT FOR PERFORMANCE ENHANCEMENT OF SELECTED TRANSISTORS IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-169983 | SEMICONDUCTOR DEVICE WITH WAKE-UP UNIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-190037 | VOLTAGE-CONTROLLED OSCILLATORS AND RELATED SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-190978 | INTERFACE SYSTEM AND METHOD WITH BACKWARD COMPATABILITY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-192369 | MEMORY MANAGEMENT UNIT (MMU) HAVING REGION DESCRIPTOR GLOBALIZATION CONTROLS AND METHOD OF OEPRATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-192370 | METHODS AND APPARATUS FOR TESTING MULTIPLE-IC DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-195705 | INCIDENT CAPACITIVE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-234264 | SYSTEMS AND METHODS FOR SEMAPHORE-BASED PROTECTION OF SHARED SYSTEM RESOURCES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-234265 | SEMICONDUCTOR STRUCTURE HAVING A THROUGH SUBSTRATE VIA (TSV) AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-235730 | INERTIAL SENSOR WITH OFF-AXIS SPRING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-259248 | METHOD OF PROTECTING AGAINST VIA FAILURE AND STRUCTURE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-263592 | EXTENDABLE-ARM ANTENNAS, AND MODULES AND SYSTEMS IN WHICH THEY ARE INCORPORATED |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-274485 | INTEGRATED CIRCUIT HAVING A MEMORY WITH LOW VOLTAGE READ/WRITE OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-277272 | PIPELINED ANALOG-TO-DIGITAL CONVERTER HAVING REDUCED POWER CONSUMPTION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-277273 | SEMICONDUCTOR DEVICE HAVING A NANOTUBE LAYER AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-287211 | SEMICONDUCTOR WAFER PLATING BUS AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-33324 | ANCHORED CONDUCTIVE VIA AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-502067 | VERTICALLY INTEGRATED MEMS ACCELERATION TRANSDUCER |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-504695 | SENSOR DEVICE WITH REDUCED PARASITIC-INDUCED ERROR |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-504697 | DEBUG SIGNALING IN A MULTIPLE PROCESSOR DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-506049 | MEMORY TESTING WITH SNOOP CAPABILITIES IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-510817 | METHOD TO CALIBRATE START VALUES FOR WRITE LEVELING IN A MEMORY SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-511872 | DEVICE WITH PROXIMITY DETECTION CAPABILITY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-513963 | METHOD AND CIRCUIT FOR CHARGING AND DISCHARGING A CIRCUIT NODE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-516876 | MULTICHANNEL RECEIVER SYSTEM, RADAR SYSTEM AND VEHICLE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-520108 | INTEGRATED CIRCUIT, TRANSCEIVER AND METHOD FOR LEAKAGE CANCELLATION IN A RECEIVE PATH |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-521107 | SIGNAL PROCESSING SYSTEM AND INTEGRATED CIRCUIT COMPRISING A PREFETCH MODULE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-523677 | PULSE WIDTH MODULATION FREQUENCY CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-526804 | MEMS DEVICE WITH STRESS ISOLATION AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-526805 | POWER TRANSISTOR WITH TURN OFF CONTROL AND METHOD FOR OPERATING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-530887 | SEMICONDUCTOR DEVICE WITH OXYGEN-DIFFUSION BARRIER LAYER AND METHOD FOR FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-532080 | CAPACITIVE TOUCH SENSOR DEVICE CONFIGURATION SYSTEMS AND METHODS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-535212 | SEMICONDUCTOR WAFER HAVING SCRIBE LANE ALIGNMENT MARKS FOR REDUCING CRACK PROPAGATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-537451 | CONFERENCE CALL SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-538419 | ADVANCED COMMUNICATION CONTROLLER UNIT AND METHOD FOR RECORDING PROTOCOL EVENTS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-539420 | VERTICAL POWER TRANSISTOR DEVICE, SEMICONDUCTOR DIE AND METHOD OF MANUFACTURING A VERTICAL POWER TRANSISTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-539933 | SYSTEMS AND METHODS FOR DELIVERING POWER IN RESPONSE TO A CONNECTION EVENT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-543137 | MICRO ELECTROMECHANICAL SYSTEMS (MEMS) HAVING A GAP STOP AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-544551 | ELECTRICAL COUPLING OF WAFER STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-548063 | METHOD OF MAKING A SEMICONDUCTOR STRUCTURE USEFUL IN MAKING A SPLIT GATE NON-VOLATILE MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-550023 | ESD PROTECTION DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-550088 | DATA PROCESSING SYSTEM HAVING BROWN-OUT DETECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-551199 | QUIESCENT CURRENT (IDDQ) INDICATION AND TESTING APPARATUS AND METHODS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-557051 | DC to DC CONVERTER HAVING SWITCH CONTROL AND METHOD OF OPERATION |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-62441 | SYNCHRONOUS DATA PROCESSING SYSTEM AND METHOD |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 2012-62442 | MEMORY CONTROLLER ADDRESS AND DATA PIN MULTIPLEXING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-014353 | STRUCTURE AND METHOD FOR HEALING TUNNEL DIELECTRIC OF NON-VOLATILE MEMORY CELLS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-015963 | MEMS DEVICE ASSEMBLY AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-017041 | VIBRATION ROBUST X-AXIS RING GYRO TRANSDUCER |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-023094 | ULTRA-THIN DIE AND METHOD OF FABRICATING SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-034808 | METHOD FOR IMPLEMENTING SECURITY OF NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-034809 | SAMPLE AND HOLD CIRCUIT AND DIFFERENTIAL SAMPLE AND HOLD CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-039970 | FULLY COMPLEMENTARY SELF-BIASED DIFFERENTIAL RECEIVER WITH STARTUP CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-073741 | MICROWAVE ADAPTORS AND RELATED OSCILLATOR SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-074320 | SAMPLE AND HOLD CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-082167 | HIGH PRECISION SINGLE EDGE CAPTURE AND DELAY MEASUREMENT CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-091075 | TAMPER DETECTOR FOR SECURE MODULE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-091184 | MEMORY WITH WORD LEVEL POWER GATING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-103808 | VEHICLE-BORNE RADAR SYSTEMS WITH CONTINUOUS-TIME, SIGMA DELTA ANALOG-TO-DIGITAL CONVERTERS, AND METHODS OF THEIR OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-109020 | PHOTRONIC DEVICE WITH REFLECTOR AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-109877 | FIELD FOCUSING FEATURES IN A RERAM CELL |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-113109 | VRS INTERFACE WITH 1/T ARMING FUNCTION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-113997 | INDUCTIVE ELEMENT WITH INTERRUPTER REGION AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-114003 | METHODS AND STRUCTURES FOR REDUCING HEAT EXPOSURE OF THERMALLY SENSITIVE SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-115491 | PROCESSOR RESOURCE AND EXECUTION PROTECTION METHODS AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-115492 | CLOCKED MEMORY WITH WORD LINE ACTIVATION DURING A FIRST PORTION OF THE CLOCK CYCLE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-115493 | CLOCKED MEMORY WITH LATCHING PREDECODER CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-119536 | FILM-ASSIST MOLDED GEL-FILL CAVITY PACKAGE WITH OVERFLOW RESERVOIR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-126381 | SEMICONDUCTOR DEVICE AND DRIVER CIRCUIT WITH A CURRENT CARRYING REGION AND ISOLATION STRUCTURE INTERCONNECTED THROUGH A RESISTOR CIRCUIT, AND METHOD OF MANUFACTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-127558 | SEMICONDUCTOR DEVICE AND DRIVER CIRCUIT WITH DRAIN AND ISOLATION STRUCTURE INTERCONNECTED THROUGH A DIODE CIRCUIT, AND METHOD OF MANUFACTURE THEREOF |

| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-127559 | HIGH BREAKDOWN VOLTAGE LDMOS DEVICE |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-127611 | EMULATED ELECTRICALLY ERASABLE MEMORY HAVING AN ADDRESS RAM FOR DATA STORED IN FLASH MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-128001 | A SEMICONDUCTOR PACKAGE STRUCTURE HAVING AN AIR GAP AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-128002 | SEMICONDUCTOR DEVICE PACKAGE AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-13856 | SEMICOCNDUCTOR DEVICE HAVING DIFFERENT NON- VOLATILE MEMORIES HAVING NANOCRYSTALS OF DIFFERING DENSITIES AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-142647 | Angular Rate Sensor With Quadrature Error Compensation |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-142648 | DEVICE PACKAGE WITH RIGID INTERCONNECT STRUCTURE CONNECTING DIE AND SUBSTRATE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-143177 | BIPOLAR TRANSISTOR WITH HIGH BREAKDOWN VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-145321 | SRAM BIT CELL WITH REDUCED BIT LINE PRECHARGE VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-154160 | LOW DROPOUT VOLTAGE REGULATOR WITH A FLOATING VOLTAGE REFERENCE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-155610 | STACKED MICROELECTRONIC PACKAGES HAVING SIDEWALL CONDUCTORS AND METHODS FOR THE FABRICATION THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-155710 | SINGLE-EVENT LATCH-UP PREVENTION TECHNIQUES FOR A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-156660 | CAPACITIVE PRESSURE SENSOR IN AN OVERMOLDED PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-157841 | NON-VOLATILE MEMORY (NVM) THAT USES SOFT PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-159882 | VARIABLE RELUCTANCE SENSOR INTERFACE WITH INTEGRATION BASED ARMING THRESHOLD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-164657 | LEAD FRAME BASED, OVER-MOLDED SEMICONDUCTOR PACKAGE WITH INTEGRATED THROUGH HOLE TECHNOLOGY (THT) HEAT SPREADER PIN(S) AND ASSOCIATED METHOD OF MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-168786 | TRANSDUCER-INCLUDING DEVICES, AND METHODS AND APPARATUS FOR THEIR CALIBRATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-172542 | NVM WITH CHARGE PUMP AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-173131 | ADAPTIVE ERROR CORRECTION FOR NON-VOLATILE MEMORIES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-174151 | SEMICONDUCTOR DEVICES WITH IMPEDANCE MATCHING CIRCUITS, AND METHODS OF MANUFACTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-174166 | THERMAL SENSOR SYSTEM AND METHOD BASED ON CURRENT RATIO |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-175649 | Sensor Packaging Method and Sensor Packages |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-176861 | DATA PROCESSOR DEVICE FOR HANDLING A WATCHPOINT AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-176866 | PRESSURE SENSOR WITH DIFFERENTIAL CAPACITIVE OUTPUT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-176871 | LEADFRAMES, AIR-CAVITY PACKAGES, AND ELECTRONIC DEVICES WITH OFFSET VENT HOLES, AND METHODS OF |

THEIR MANUFACTURE

| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-178981 | MICROELECTRONIC PACKAGES HAVING TRENCH VIAS AND METHODS FOR THE MANUFACTURE THEREOF |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-190289 | NON-VOLATILE MEMORY (NVM) WITH ADAPTIVE WRITE OPERATIONS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-191302 | ELECTRONIC CIRCUITS WITH VARIABLE ATTENUATORS AND METHODS OF THEIR OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-199779 | High Voltage Diode |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-199780 | METHOD OF MAKING A LOGIC TRANSISTOR AND A NON- VOLATILE MEMORY (NVM) CELL |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-202874 | PACKAGING FOR SEMICONDUCTOR SENSOR DEVICES AND METHODS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-203039 | TWO-PORT SRAM HAVING IMPROVED WRITE OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-39969 | RANDOM VALUE PRODUCTION METHODS AND SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-502573 | SEMICONDUCTOR DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-502580 | APPARATUS AND METHOD TO COMPENSATE FOR INJECTION LOCKING |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-504926 | MULTI-PORT MEMORY HAVING A VARIABLE NUMBER OF USED WRITE PORTS |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-507972 | OPEN CIRCUIT DETECTOR AND METHOD THEREFORE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-507977 | EMULATED ELECTRICALLY ERASABLE (EEE) MEMORY AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-508012 | CIRCUIT FOR VERIFYING THE WRITE ENABLE OF A ONE TIME PROGRAMMABLE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-509076 | OVERVOLTAGE PROTECTION CIRCUIT FOR AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-512565 | POWER SWITCHING APPARATUS AND METHOD FOR IMPROVING CURRENT SENSE ACCURACY |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-512625 | DATA PROCESSOR HAVING MULTIPLE LOW POWER MODES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-515361 | SWITCHING REGULATOR WITH INPUT CURRENT LIMITING CAPABILITIES |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-517553 | INTEGRATED CIRCUIT DEVICE AND METHOD FOR GENERATING A TUNING SIGNAL FOR CALIBRATING A VOLTAGE CONTROLLED OSCILLATOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-518394 | TRANSMISSION GATE CIRCUITRY FOR HIGH VOLTAGE TERMINAL |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-520226 | DISPLAY CONTROLLING UNIT, IMAGE DISPLAYING SYSTEM AND METHOD FOR OUTPUTTING IMAGE DATA |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-525369 | VIDEO PROCESSING SYSTEM AND METHOD FOR PARALLEL PROCESSING OF VIDEO DATA |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-525370 | PUSH-PUSH OSCILLATOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-530803 | METHODS FOR PROCESSING A SEMICONDUCTOR WAFER, A SEMICONDUCTOR WAFER AND A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-532280 | LOW-VOLTAGE EXIT DETECTOR, ERROR DETECTOR, LOW- VOLTAGE SAFE CONTROLLER, BROWN-OUT DETECTION METHOD, AND BROWN-OUT SELF-HEALING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-533291 | INTEGRATED CIRCUIT DEVICE, WIRELESS COMMUNICATION |

UNIT AND METHOD OF MANUFACTURE THEREFOR

| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-539352 | METHOD FOR ENABLING CALIBRATION DURING START- UP OF A MICRO CONTROLLER UNIT AND INTEGRATED CIRCUIT THEREFOR |
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| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-79324 | RERAM DEVICE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-93707 | ERASING A NON-VOLATILE MEMORY (NVM) SYSTEM HAVING ERROR CORRECTION CODE (ECC) |
| FREESCALE SEMICONDUCTOR, INC. | JP | 2013-95791 | CAVITY-TYPE SEMICONDUCTOR PACKAGE AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | JP | 63-274342 | DATA PROCESSOR WITH DEVELOPMEN T SUPPORT FEATURES |
| FREESCALE SEMICONDUCTOR, INC. | JP | NA | SWITCHING AMPLIFIER HAVING DIGITAL CORRECTION AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | JP | NA | CIRCUIT DEVICE WITH AT LEAST PARTIAL PACKAGING AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | JP | NA | CIRCUIT DEVICE WITH AT LEAST PARTIAL PACKAGING AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | JP | NA | INTEGRATED ANTENNA PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | JP | Not yet available | DIGITAL METHOD TO OBTAIN THE I-V CURVES OF NVM BITCELLS |
| FREESCALE SEMICONDUCTOR, INC. | JP | Not yet available | SEMICONDUCTOR DEVICE AND RELATED FABRICATION METHODS |
| FREESCALE SEMICONDUCTOR, INC. | JP | Not yet available | SEMICONDUCTOR DEVICE AND RELATED FABRICATION METHODS |
| FREESCALE SEMICONDUCTOR, INC. | JP | PCT/RU2011/000107 | OVERCURRENT PROTECTION DEVICE AND METHOD OF OPERATING A POWER SWITCH |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2006-119025 | LOW VOLTAGE LOW POWER CLASS A/B OUTPUT STAGE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2006-119486 | METHOD FOR PACKAGING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2006-7013210 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT, AND SEMICONDUCTOR COMPONENT FORMED THEREBY |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7001880 | SEMICONDUCTOR DEVICES AND METHOD OF FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7001921 | ELECTRONIC DEVICE INCLUDING DISCONTINUOUS STORAGE ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7007606 | MICROELECTRONIC ASSEMBLY AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7008172 | SEMICONDUCTOR DEVICE HAVING NANO-PILLARS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7008694 | PROGRAMMABLE FUSE WITH SILICON GERMANIUM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7009819 | MULTIPLE DEVICE TYPES INCLUDING AN INVERTED-T CHANNEL TRANSISTOR AND METHOD THEREFORE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7010294 | LATERALLY GROWN NANOTUBES AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7010932 | FINE PITCH INTERCONNECT AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7011022 | ELECTRONIC DEVICE INCLUDING A TRANSISTOR STRUCTURE HAVING AN ACTIVE REGION ADJACENT TO A STRESSOR LAYER AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7013174 | METHOD AND PROGRAM PRODUCT FOR PROTECTING |

INFORMATION IN EDA TOOL DESIGN VIEWS

| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7014424 | SUPERJUNCTION POWER MOSFET |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7018381 | SPLIT GATE MEMORY CELL IN A FINFET |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7018457 | MEMORY CELL USING A DIELECTRIC HAVING NON-UNIFORM THICKNESS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7019010 | SYSTEM AND METHOD FOR FAST MOTION ESTIMATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7020067 | METHOD AND APPARATUS FOR TESTING A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7020330 | METHOD AND APPARATUS FOR INDICATING DIRECTIONALITY IN INTEGRATED CIRCUIT MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7020577 | CAP LAYER FOR AN ALUMINUM COPPER BOND PAD |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7020579 | SEMICONDUCTOR PROCESS INTEGRATING SOURCE/DRAIN STRESSORS AND INTERLEVEL DIELECTRIC LAYER STRESSORS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7020618 | NOISE ISOLATION BETWEEN CIRCUIT BLOCKS IN AN INTEGRATED CIRCUIT CHIP |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7020966 | BIT LINE PRECHARGE IN EMBEDDED MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7021970 | DYNAMIC TIMING ADJUSTMENT IN A CIRCUIT DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7022159 | WARP COMPENSATED PACKAGE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7022455 | METHOD OF FORMING A SEMICONDUCTOR DEVICE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7022488 | ELECTRONIC DEVICE AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7022525 | SILICIDED NONVOLATILE MEMORY AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7023407 | MEMORY WITH CLOCKED SENSE AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7023448 | SEMICONDUCTOR DEVICE AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7023823 | BARRIER FOR USE IN 3-D INTEGRATION OF CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7024174 | APPARATUS AND METHOD FOR ADJUSTING AN OPERATING PARAMETER OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7024213 | LEAD FRAME BASED, OVER-MOLDED SEMICONDUCTOR PACKAGE WITH INTEGRATED THROUGH HOLE TECHNOLOGY (THT) HEAT SPREADER PIN(S) AND ASSOCIATED METHOD OF MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7028517 | CONTENTION-FREE HIERARCHICAL BIT LINE IN EMBEDDEI MEMORY AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7029534 | DIE LEVEL METAL DENSITY GRADIENT FOR IMPROVED FLIP CHIP PACKAGE RELIABILITY |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2008-7031752 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7001710 | TRANSISTOR WITH ASYMMETRY FOR DATA STORAGE CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7003904 | SUPERJUNCTION TRENCH DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7004277 | LEVEL SHIFTING CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7005238 | VIDEO INFORMATION PROCESSING SYSTEM WITH SELECTIVE CHROMA DEBLOCK FILTERING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7006625 | DISTRIBUTED ELECTROSTATIC DISCHARGE PROTECTION |

CIRCUIT WITH VARYING CLAMP SIZE

| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7008704 | SYSTEM AND METHOD FOR REDUCING EDGE EFFECT |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7008904 | METHODS AND APPARATUS FOR A QUAD FLAT NO-LEAD (QFN) PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7009009 | ONE TRANSISTOR DRAM CELL STRUCTURE AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7009943 | METHOD OF PACKAGING A SEMICONDUCTOR DEVICE AND A PREFABRICATED CONNECTOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7015540 | METHOD OF MAKING A NON-VOLATILE MEMORY DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7015607 | METHOD OF MAKING A SEMICONDUCTOR DEVICE HAVING HIGH VOLTAGE TRANSISTORS, NON-VOLATILE MEMORY TRANSISTORS, AND LOGIC TRANSISTORS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7016182 | DYNAMIC PAD SIZE TO REDUCE SOLDER FATIGUE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7017031 | MULTI-LAYER SOURCE/DRAIN STRESSOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7017436 | MEMORY HAVING A DUMMY BITLINE FOR TIMING CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7017872 | SOURCE/DRAIN STRESSOR AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7018243 | INTEGRATED CIRCUIT FUSE ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7018647 | TRENCH FORMATION IN A SEMICONDUCTOR MATERIAL |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7018982 | DEVICE AND METHOD FOR GENERATING CACHE USER INITIATED PRE-FETCH REQUESTS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7019937 | METHOD AND DEVICE FOR PROGRAMMING ANTI-FUSES |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7020035 | SIMPLIFIED DEBLOCK FILTERING FOR REDUCED MEMORY ACCESS AND COMPUTATIONAL COMPLEXITY |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7022966 | METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE TYPES OF SCHOTTKY JUNCTIONS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7023240 | LOW VOLTAGE DATA PATH IN MEMORY ARRAY |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7023333 | THREAD DE-EMPHASIS INSTRUCTION FOR MULTITHREADED PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2009-7025412 | ONE TIME PROGRAMMABLE ELEMENT SYSTEM IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2010-7000648 | DYNAMIC VOLTAGE ADJUSTMENT FOR MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2010-7001862 | STRESS RELIEF OF A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2010-7002371 | METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE OBTAINABLE THEREWITH |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2010-7004382 | METHOD OF PACKAGING AN INTEGRATED CIRCUIT DIE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2010-7004436 | RF CIRCUIT WITH CONTROL UNIT TO REDUCE SIGNAL POWER UNDER APPROPRIATE CONDITIONS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2010-7004818 | METHOD AND CIRCUIT FOR PREVENTING HIGH VOLTAGE MEMORY DISTURB |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2010-7004951 | SEMICONDUCTOR DEVICE TEST SYSTEM HAVING REDUCED CURRENT LEAKAGE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2010-7007108 | PROGRAMMABLE ROM USING TWO BONDED STRATA AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2010-7007865 | SIMD DOT PRODUCT OPERATIONS WITH OVERLAPPED OPERANDS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2010-7013959 | 3-D SEMICONDUCTOR DIE STRUCTURE WITH CONTAINING FEATURE AND METHOD |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2010-7015023 | MIGFET CIRCUIT WITH ESD PROTECTION |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2010-7017877 | NON-VOLATILE MEMORY WITH REDUCED CHARGE FLUENCE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2010-7019580 | BALUN TRANSFORMER WITH IMPROVED HARMONIC SUPRESSION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2010-7029038 | CIRCUIT FOR AND AN ELECTRONIC DEVICE INCLUDING A NONVOLATILE MEMORY CELL AND A PROCESS OF FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2010-7029593 | UTILIZATION OF A STORE BUFFER FOR ERROR RECOVERY ON A STORE ALLOCATION CACHE MISS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2010-7029643 | SEMICONDUCTOR DEVICE WITH REDUCED SENSITIVITY TO PACKAGE STRESS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-0066720 | CURRENT REDUCTION IN A SINGLE STAGE CYCLIC ANALOG TO DIGITAL CONVERTER WITH VARIABLE RESOLUTION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-0068760 | SOFT PROGRAM OF A NON-VOLATILE MEMORY BLOCK |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-0073893 | METHOD FOR FORMING A CAPPED MICRO-ELECTRO- MECHANICAL SYSTEM (MEMS) DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-0096047 | POLYMER CORE WIRE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-0111454 | METHOD OF MAKING A MICRO-ELECTRO-MECHANICAL- SYSTEMS (MEMS) DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-0118698 | DIFFERENTIAL EQUALIZERS WITH SOURCE DEGENERATION AND FEEDBACK CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-7005244 | ERROR DETECTION SCHEMES FOR A UNIFIED CACHE IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-7005826 | PROVISION OF EXTENDED ADDRESSING MODES IN A SINGLE INSTRUCTION MULTIPLE DATA (SIMD) DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-7006168 | DEBUG INSTRUCTION FOR USE IN A MULTI-THREADED DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-7006187 | TRANSISTOR WITH GAIN VARIATION COMPENSATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-7008865 | METHOD OF MAKING A SPLIT GATE MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-7010579 | TECHNIQUE FOR INTERCONNECTING INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-7014141 | LED DRIVER WITH FEEDBACK CALIBRATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-7019683 | ANTIFUSE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-7020042 | AUTHENTICATED DEBUG ACCESS FOR FIELD RETURNS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-7021299 | EXPOSED PAD BACKSIDE PRESSURE SENSOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-7021662 | DYNAMIC RANDOM ACCESS MEMORY (DRAM) REFRESH |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-7025451 | NEGATIVE VOLTAGE GENERATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-7026210 | ADDRESS TRANSLATION TRACE MESSAGE GENERATION FOR DEBUG |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-7026878 | METHOD TO CALIBRATE START VALUES FOR WRITE LEVELING IN A MEMORY SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-7026969 | PEAK DETECTION WITH DIGITAL CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-7029264 | METHOD AND CIRCUIT FOR CHARGING AND DISCHARGING A CIRCUIT NODE |
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KR 10-2011-77397

FREESCALE SEMICONDUCTOR, INC.

MEMORY WITH LOW VOLTAGE MODE OPERATION

| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2011-87208 | PATTERNING A GATE STACK OF A NON-VOLATILE MEMORY (NVM) WITH SIMULTANEOUS ETCH IN NON-NVM AREA |
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| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2012-0037853 | METHOD OF MAKING A SEMICONDUCTOR STRUCTURE USEFUL IN MAKING A SPLIT GATE NON-VOLATILE MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2012-0077643 | SYSTEMS AND METHODS FOR DATA CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2012-0096302 | MOSFET MISMATCH CHARACTERIZATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2012-0118813 | BUILT-IN SELF TRIM FOR NON-VOLATILE MEMORY REFERENCE CURRENT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2012-126062 | SEMICONDUCTOR SENSOR DEVICE AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2012-27035 | SYNCHRONOUS DATA PROCESSING SYSTEM AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2012-27036 | MEMORY CONTROLLER ADDRESS AND DATA PIN MULTIPLEXING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2012-59177 | DUAL PORT PRESSURE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2012-7003525 | SEMICONDUCTOR DEVICE AND RELATED FABRICATION METHODS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2012-7012730 | SEMICONDUCTOR WAFER HAVING SCRIBE LANE ALIGNMENT MARKS FOR REDUCING CRACK PROPAGATION |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2012-7012901 | SYSTEMS AND METHODS FOR DELIVERING POWER IN RESPONSE TO A CONNECTION EVENT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2012-8414 | MEMORY HAVING A LATCHING SENSE AMPLIFIER RESISTANT TO NEGATIVES BIAS TEMPERATURE INSTABILITY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2012-90177 | SEMICONDUCTOR DEVICE WITH WAKE-UP UNIT |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2013-0005009 | SKEWED SRAM CELL |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2013-0030738 | WRITE CONTENTION-FREE, NOISE-TOLERANT MULTIPORT BITCELL |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2013-0043611 | MICROWAVE ADAPTORS AND RELATED OSCILLATOR SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2013-0099574 | NON-VOLATILE MEMORY (NVM) THAT USES SOFT PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2013-0109709 | NON-VOLATILE MEMORY (NVM) WITH ADAPTIVE WRITE OPERATIONS |
| FREESCALE SEMICONDUCTOR, INC. | KR | 10-2013-109392 | NVM WITH CHARGE PUMP AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | MY | PI20094674 | METHOD OF FORMING SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | MY | PI20095012 | IMPROVED SEMICONDUCTOR PACKAGE AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | MY | PI2010000044 | SCAN BASED TEST ARCHITECTURE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | MY | PI2010001643 | LEAD FRAME FOR SEMICONDUCTOR PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | MY | PI2011001861 | SEMICONDUCTOR TRAY CARRIER |
| FREESCALE SEMICONDUCTOR, INC. | MY | PI2012004714 | SYSTEM AND METHOD FOR CLEANING BOND WIRE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 093130261 | ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 094116365 | SEPARATELY STRAINED N-CHANNEL AND P-CHANNEL TRANSISTORS |
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| FREESCALE SEMICONDUCTOR, INC. | TW | 094126428 | METHOD AND APPARATUS FOR PERFORMANCE ENHANCEMENT IN AN ASYMMETRICAL SEMICONDUCTOR DEVICE |
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| FREESCALE SEMICONDUCTOR, INC. | TW | 094127044 | METHOD AND APPARATUS FOR MOBILITY ENHANCEMENT IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 094129708 | PROGRAMMING AND ERASING STRUCTURE FOR A FLOATING GATE MEMORY CELL AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | TW | 094137697 | TRANSISTOR STRUCTURE WITH DUAL TRENCH FOR OPTIMIZED STRESS EFFECT AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095100764 | METHOD OF FABRICATING A SILICON-ON-INSULATOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095104264 | METHOD OF REMOVING NANOCLUSTERS IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095106162 | METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING A DIFFUSION BARRIER STACK AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095106398 | METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING ASYMMETRIC DIELECTRIC REGIONS AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095106399 | ANTIFUSE ELEMENT AND ELECTRICALLY REDUNDANT ANTIFUSE ARRAY FOR CONTROLLED RUPTURE LOCATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095107026 | SYSTEM FOR INTEGRATED DATA INTEGRITY VERIFICATION AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095107494 | MEMORY STRUCTURE AND METHOD OF PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095108016 | CONDUCTING METAL OXIDE WITH ADDITIVE AS P-MOS DEVICE ELECTRODE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095108670 | APPARATUS FOR CURRENT SENSING |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095109761 | METHOD AND APPARATUS FOR LOW VOLTAGE WRITE IN A STATIC RANDOM ACCESS MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095113584 | SEMICONDUCTOR PACKAGE AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095121340 | CHEMICAL DIE SINGULATION TECHNIQUE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095121983 | METHOD OF FORMING A SEMICONDUCTOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095125132 | PACKAGED INTEGRATED CIRCUIT WITH ENHANCED THERMAL DISSIPATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095125136 | STRESS RELEASE MECHANISM IN MEMS DEVICE AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095126624 | SPLIT GATE STORAGE DEVICE INCLUDING A HORIZONTAL FIRST GATE AND A VERTICAL SECOND GATE IN A TRENCH |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095127050 | ELECTRONIC DEVICE INCLUDING DISCONTINUOUS STORAGI ELEMENTS |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095129481 | NONVOLATILE MEMORY CELL PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095131664 | MEMORY WITH ROBUST DATA SENSING AND METHOD FOR SENSING DATA |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095131908 | GROOVED PLATEN WITH CHANNELS OR PATHWAY TO AMBIENT AIR |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095132821 | SEMICONDUCTOR STACKED DIE/WAFER CONFIGURATION AND PACKAGING AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095133783 | MICROELECTRONIC ASSEMBLY AND METHOD FOR FORMING |

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| FREESCALE SEMICONDUCTOR, INC. | TW | 095134084 | MICROELECTRONIC ASSEMBLY AND METHOD FOR FORMING THE SAME |
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| FREESCALE SEMICONDUCTOR, INC. | TW | 095136632 | SEMICONDUCTOR DEVICE HAVING NANO-PILLARS AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095137375 | PROGRAMMABLE FUSE WITH SILICON GERMANIUM |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095138067 | SEMICONDUCTOR STRUCTURE WITH REDUCED GATE DOPING AND METHODS FOR FORMING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095138069 | MULTIPLE DEVICE TYPES INCLUDING AN INVERTED-T CHANNEL TRANSISTOR AND METHOD THEREFORE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095138503 | ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUIT FOR MULTIPLE POWER DOMAIN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095138667 | SEMICONDUCTOR STRUCTURE AND METHOD OF ASSEMBLY |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095139041 | SEMICONDUCTOR DEVICE WITH REDUCED PACKAGE CROSSTALK AND LOSS |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095139043 | ELECTRONIC ASSEMBLY HAVING GRADED WIRE BONDING |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095139048 | PLASTIC PACKAGED DEVICE WITH DIE INTERFACE LAYER |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095139468 | ELECTRONIC DEVICE INCLUDING A TRANSISTOR STRUCTURE HAVING AN ACTIVE REGION ADJACENT TO A STRESSOR LAYER AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095139912 | FINE PITCH INTERCONNECT AND METHOD OF MAKING |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095139951 | SEMICONDUCTOR DEVICE AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095141602 | METHOD AND APPARATUS FOR PROGRAMMING/ERASING A NON-VOLATILE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095142110 | DEVICE AND METHOD FOR COMPENSATING FOR VOLTAGE DROPS |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095143436 | SUPERJUNCTION POWER MOSFET |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095144493 | TRANSISTOR WITH IMMERSED CONTACTS AND METHODS OF FORMING THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095145553 | SEMICONDUCTOR DEVICE COMPRISING A TRANSISTOR HAVING A COUNTER-DOPED CHANNEL REGION AND METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095146663 | INTEGRATED CIRCUIT USING FINFETS AND HAVING A STATIC RANDOM ACCESS MEMORY (SRAM) |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095147984 | SEMICONDUCTOR INTERCONNECT HAVING ADJACENT RESERVOIR FOR BONDING AND METHOD FOR FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095148584 | DUAL METAL SILICIDE SCHEME USING A DUAL SPACER PROCESS |
| FREESCALE SEMICONDUCTOR, INC. | TW | 095149108 | MEMORY CELL USING A DIELECTRIC HAVING NON-UNIFORM THICKNESS |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096100185 | REGULATED VOLTAGE SYSTEM AND METHOD OF PROTECTION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096100710 | METHOD AND APPARATUS FOR FORMING A SEMICONDUCTOR-ON-INSULATOR (SOI) BODY-CONTACTED DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096101922 | EPI T-GATE STRUCTURE FOR CoSi2 EXTENDIBILITY |
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| FREESCALE SEMICONDUCTOR, INC. | TW | 096103125 | NOISE ISOLATION BETWEEN CIRCUIT BLOCKS IN AN INTEGRATED CIRCUIT CHIP |
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| FREESCALE SEMICONDUCTOR, INC. | TW | 096103126 | METHOD AND APPARATUS FOR INDICATING DIRECTIONALITY IN INTEGRATED CIRCUIT MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096103282 | ERROR CORRECTION DEVICE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096104207 | DYNAMIC TIMING ADJUSTMENT IN A CIRCUIT DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096104890 | LOW VOLTAGE OUTPUT BUFFER AND METHOD FOR BUFFERING DIGITAL OUTPUT DATA |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096104932 | METAL GATE WITH ZIRCONIUM |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096105319 | APPARATUS AND METHOD FOR ADJUSTING AN OPERATING PARAMETER OF AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096106732 | METHOD FOR FORMING A DEPOSITED OXIDE LAYER |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096107088 | ELECTRICAL FIELD SENSORS |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096107305 | RF POWER TRANSISTOR DEVICE WITH METAL ELECTROMIGRATION DESIGN AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096107714 | SILICIDED NONVOLATILE MEMORY AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096107870 | ELECTRONIC DEVICE AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096108415 | MEMORY WITH CLOCKED SENSE AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096108569 | SEMICONDUCTOR DEVICE STRUCTURE AND INTEGRATED CIRCUIT THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096108790 | SEMICONDUCTOR FABRICATION PROCESS USING ETCH STOP LAYER TO OPTIMIZE FORMATION OF SOURCE/DRAIN STRESSOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096108958 | A WORLDWIDE DRIVER FOR A NON-VOLATILE MEMORY DEVICE, A NON-VOLATILE MEMORY DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096109128 | BARRIER FOR USE IN 3-D INTEGRATION OF CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096111387 | CONTACT SURROUNDED BY PASSIVATION AND POLYIMIDE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096111431 | METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING AN INTERLAYER AND STRUCTURE THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096111642 | MEMORY WITH LEVEL SHIFTING WORD LINE DRIVER AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096112138 | DIE LEVEL METAL DENSITY GRADIENT FOR IMPROVED FLIP CHIP PACKAGE RELIABILITY |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096112740 | METHOD OF FORMING A SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096121169 | RF POWER TRANSISTOR DEVICE WITH HIGH PERFORMANCE SHUNT CAPACITOR AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096124407 | WAFER AND METHOD OF FORMING ALIGNMENT MARKERS |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096127119 | DISTRIBUTED ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT WITH VARYING CLAMP SIZE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096133902 | ONE TRANSISTOR DRAM CELL STRUCTURE AND METHOD FOR FORMING |
| FREESCALE SEMICONDUCTOR, INC. | TW | 096135959 | METHODS AND APPARATUS FOR A QUAD FLAT NO-LEAD (QFN |

PACKAGE

| VOLTAGE PERFORMANCE AND A METHOD FOR FORMING TO SAME FREESCALE SEMICONDUCTOR, INC. TW 97103705 SOURCE/DRAIN STRESSOR AND METHOD THEREFOR FREESCALE SEMICONDUCTOR, INC. TW 097104336 MULTI-LAYER SOURCE/DRAIN STRESSOR FREESCALE SEMICONDUCTOR, INC. TW 097105061 FORMING A SEMICONDUCTOR DEVICE HAVING EPITAXIALL: GROWN SOURCE AND DRAIN REGIONS FREESCALE SEMICONDUCTOR, INC. TW 097106129 SEMICONDUCTOR DEVICE HAVING A METAL CARBIDE GATE WITH AN ELECTROPOSITIVE ELEMENT AND A METHOD OF MAKING THE SAME FREESCALE SEMICONDUCTOR, INC. TW 097106322 ELECTRONIC DEVICE INCLUDING CHANNEL REGIONS LYING AT DIFFERENT ELEVATIONS AND PROCESSES OF FORMING THE SAME FREESCALE SEMICONDUCTOR, INC. TW 097107237 TRENCH FORMATION IN A SEMICONDUCTOR MATERIAL FREESCALE SEMICONDUCTOR, INC. TW 097107252 INTEGRATED CIRCUIT FUSE ARRAY FREESCALE SEMICONDUCTOR, INC. TW 097112428 A FIRST INTER-LAYER DIELECTRIC STACK FOR NON- VOLATILE MEMORY FREESCALE SEMICONDUCTOR, INC. TW 097113393 ETCH METHOD IN THE MANUFACTURE OF A SEMICONDUCTOR DEVICE | | | | |
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| FREESCALE SEMICONDUCTOR, INC. TW 096138041 TWO-PORT SRAM HAVING IMPROVED WRITE OPERATION PACKAGING A DEVICE USING A DIELECTRIC LAYER FREESCALE SEMICONDUCTOR, INC. TW 096138041 TWO-PORT SRAM HAVING IMPROVED WRITE OPERATION METHOD OF PACKAGING A DEVICE USING A DIELECTRIC LAYER PACKAGING A DEVICE USING A DIELECTRIC LAYER PROMING A SEMICONDUCTOR, INC. TW 096151427 SYSTEM AND METHOD FOR REDUCING NOISE IN SENSORS WITH CAPACITIVE PICKUP FREESCALE SEMICONDUCTOR, INC. TW 097100225 SEMICONDUCTOR DEVICE HAVING A METAL FLECTRODE AND STRUCTURE THEREOF FREESCALE SEMICONDUCTOR, INC. TW 097100425 DIFFERENTIAL CAPACITIVE SENSOR AND METHOD OF FORMING A SEMICONDUCTOR DEVICE AND METHOD OF MAKING SAME FREESCALE SEMICONDUCTOR, INC. TW 097100887 SEMICONDUCTOR DEVICE AND METHOD OF FORMING A SEMICONDUCTOR DEVICE AND METHOD OF MAKING SAME FREESCALE SEMICONDUCTOR, INC. TW 09710297 METHOD OF MAKING A NON-VOLATILE MEMORY DEVICE PROBLEMS AND SEMICONDUCTOR DEVICE AND METHOD OF MAKING AND NON-VOLATILE MEMORY DEVICE PROBLEMS AND ADDRESS AND ADD | FREESCALE SEMICONDUCTOR, INC. | TW | 096136511 | |
| FREESCALE SEMICONDUCTOR, INC. TW 096151412 SYSTEM AND METHOD OF PACKAGING A DEVICE USING A DIELECTRIC LAYER PREESCALE SEMICONDUCTOR, INC. TW 096151427 FORMING A SEMICONDUCTOR DEVICE HAVING A METAL ELECTRODE AND STRUCTURE THEREOF PREESCALE SEMICONDUCTOR, INC. TW 097100452 DIFFERENTIAL CAPACITIVE SEMICONDUCTOR DEVICE HAVING A METAL ELECTRODE AND STRUCTURE THEREOF PREESCALE SEMICONDUCTOR, INC. TW 097100452 DIFFERENTIAL CAPACITIVE SENSOR AND METHOD OF FORMING A SEMICONDUCTOR DEVICE AND METHOD OF MAKING SAME PREESCALE SEMICONDUCTOR, INC. TW 097102097 METHOD OF MAKING A NON-VOLATILE MEMORY DEVICE PREESCALE SEMICONDUCTOR, INC. TW 097102702 METHOD OF MAKING A NON-VOLATILE MEMORY DEVICE PREESCALE SEMICONDUCTOR, INC. TW 097102702 METHOD OF MAKING A NON-VOLATILE MEMORY DEVICE PREESCALE SEMICONDUCTOR, INC. TW 097103738 ELECTRONIC DEVICE WITH CONNECTION BUMPS FREESCALE SEMICONDUCTOR, INC. TW 097103763 ELECTRONIC DEVICE WITH CONNECTION BUMPS FREESCALE SEMICONDUCTOR, INC. TW 097103763 ELECTRONIC DEVICE WITH CONNECTION BUMPS FREESCALE SEMICONDUCTOR, INC. TW 097103770 SOURCE/DRAIN STRESSOR AND METHOD THEREFOR FREESCALE SEMICONDUCTOR, INC. TW 097103765 SOURCE/DRAIN STRESSOR AND METHOD THEREFOR FREESCALE SEMICONDUCTOR, INC. TW 097103612 SEMICONDUCTOR DEVICE HAVING PETHAXIALLE GROWN SOURCE AND DRAIN REGIONS LYING FREESCALE SEMICONDUCTOR, INC. TW 097106322 ELECTRONIC DEVICE HAVING A METHOD OF MAKING A SEMICONDUCTOR MATERIAL FREESCALE SEMICONDUCTOR, INC. TW 097106322 BELECTRONIC DEVICE HAVING A DEPTHAXIALLE GROWN SOURCE AND DRAIN REGIONS LYING AT DIFFERENT ELEVATIONS AND PROCESSES OF FORMING THE SAME FREESCALE SEMICONDUCTOR, INC. TW 097106322 INTEGRATED CIRCUIT FUSE ARRAY FREESCALE SEMICONDUCTOR, INC. TW 097107252 INTEGRATED CIRCUIT FUSE ARRAY FREESCALE SEMICONDUCTOR, INC. TW 097107253 METHOD FOR SELECTIVE REMOVAL OF A LAYER AFENCENT AND A SEMICONDUCTOR FOR CONSTRUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097107333 SEPARATE LAYER FORMATION IN A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTO | FREESCALE SEMICONDUCTOR, INC. | TW | 096137896 | STRUCTURE EXTENDING THROUGH A BURIED INSULATING |
| LAYER FREESCALE SEMICONDUCTOR, INC. TW 096151412 SYSTEM AND METHOD FOR REDUCING NOISE IN SENSORS WITH CAPACITIVE PICKUP FREESCALE SEMICONDUCTOR, INC. TW 09615142 FORMING A SEMICONDUCTOR DEVICE HAVING A METAL ELECTRODE AND STRUCTURE THEREOF FREESCALE SEMICONDUCTOR, INC. TW 097100225 SEMICONDUCTOR DEVICE AND METHOD OF FORMING A SEMICONDUCTOR DEVICE AND METHOD OF MAKING SAME FREESCALE SEMICONDUCTOR, INC. TW 097100887 SEMICONDUCTOR DEVICE AND METHOD OF FORMING A SEMICONDUCTOR DEVICE AND METHOD OF FORMING A SEMICONDUCTOR DEVICE AND METHOD OF FORMING A SEMICONDUCTOR DEVICE OLDER FATIGUE FREESCALE SEMICONDUCTOR, INC. TW 097102702 METHOD OF MAKING A NON-VOLATILE MEMORY DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097103735 ELECTRONIC DEVICE SOLDER FATIGUE FREESCALE SEMICONDUCTOR, INC. TW 097103736 ELECTRONIC DEVICE WITH CONNECTION BUMPS FREESCALE SEMICONDUCTOR, INC. TW 097103703 MICROELECTRONIC ASSEMBLY MITH IMPROVED ISOLATION VOLTAGE PERFORMANCE AND A METHOD FOR FORMING TO SAME FREESCALE SEMICONDUCTOR, INC. TW 097103705 SOURCE/DRAIN STRESSOR AND METHOD THEREFOR FREESCALE SEMICONDUCTOR, INC. TW 097103706 MULTI-LAYER SOURCE/DRAIN STRESSOR FREESCALE SEMICONDUCTOR, INC. TW 097104336 MULTI-LAYER SOURCE/DRAIN STRESSOR FREESCALE SEMICONDUCTOR, INC. TW 097105021 SEMICONDUCTOR DEVICE HAVING A METHOD THEREFOR FREESCALE SEMICONDUCTOR, INC. TW 097105022 ELECTRONIC DEVICE HAVING A METHOD THEREFOR FREESCALE SEMICONDUCTOR, INC. TW 097105031 MULTI-LAYER SOURCE/DRAIN STRESSOR FREESCALE SEMICONDUCTOR, INC. TW 097105031 SEMICONDUCTOR DEVICE HAVING A METHOD OF MAKING THE SAME FREESCALE SEMICONDUCTOR, INC. TW 097105032 ELECTRONIC DEVICE HAVING A METHOD OF MAKING THE SAME FREESCALE SEMICONDUCTOR, INC. TW 097105032 FIRE SAME FREESCALE SEMICONDUCTOR, INC. TW 097105033 MICTOR DEVICE REMOVAL OF A LAYER ARE THE SAME FREESCALE SEMICONDUCTOR, INC. TW 0971071549 SEMICONDUCTOR DEVICE FREESCALE SEMICOND | FREESCALE SEMICONDUCTOR, INC. | TW | 096138041 | TWO-PORT SRAM HAVING IMPROVED WRITE OPERATION |
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| HIGH VOLTAGE TRANSISTORS, NON-VOLATILE MEMORY TRANSISTORS, ADD LOGIC TRANSISTORS SPARAL SEMICONDUCTOR, INC. TW 097103578 ELECTRONIC DEVICE WITH CONNECTION BUMPS FREESCALE SEMICONDUCTOR, INC. TW 97103703 MICROELECTRONIC ASSEMBLY WITH IMPROVED ISOLATION VOLTAGE PERFORMANCE AND A METHOD FOR FORMING TRANSISTORS, AND METHOD THEREFOR SAME FREESCALE SEMICONDUCTOR, INC. TW 097104336 MULTI-LAYER SOURCE/DRAIN STRESSOR FREESCALE SEMICONDUCTOR, INC. TW 097105061 FORMING A SEMICONDUCTOR DEVICE HAVING EPITAXIALL GROWN SOURCE AND DRAIN REGIONS FREESCALE SEMICONDUCTOR, INC. TW 097106129 SEMICONDUCTOR DEVICE HAVING A METHOD OF MAKING THE SAME FREESCALE SEMICONDUCTOR, INC. TW 097106322 ELECTRONIC DEVICE INCLUDING CHANNEL REGIONS LYING AT DIFFERENT ELEVATIONS AND PROCESSES OF FORMING THE SAME FREESCALE SEMICONDUCTOR, INC. TW 097107252 INTEGRATED CIRCUIT FUSE ARRAY FREESCALE SEMICONDUCTOR, INC. TW 097112428 METHOD FOR SELECTIVE REMOVAL OF A LAYER FREESCALE SEMICONDUCTOR, INC. TW 097112428 A FIRST INTER-LAYER DIELECTRIC STACK FOR NON-VOLATILE MEMORY FREESCALE SEMICONDUCTOR, INC. TW 097112430 SEPARATE LAYER FORMATION IN A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 09711393 ETCH METHOD IN THE MANUFACTURE OF A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 09711350 SEPARATE LAYER FORMATION IN A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 09711559 SEMICONDUCTOR WAFER PROCESSING FREESCALE SEMICONDUCTOR, INC. TW 097115590 METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE | FREESCALE SEMICONDUCTOR, INC. | TW | 097102535 | DYNAMIC PAD SIZE TO REDUCE SOLDER FATIGUE |
| FREESCALE SEMICONDUCTOR, INC. TW 97103703 MICROELECTRONIC ASSEMBLY WITH IMPROVED ISOLATION VOLTAGE PERFORMANCE AND A METHOD FOR FORMING THE SAME FREESCALE SEMICONDUCTOR, INC. TW 97103705 SOURCE/DRAIN STRESSOR AND METHOD THEREFOR FREESCALE SEMICONDUCTOR, INC. TW 097104336 MULTI-LAYER SOURCE/DRAIN STRESSOR FREESCALE SEMICONDUCTOR, INC. TW 097105061 FORMING A SEMICONDUCTOR DEVICE HAVING EPITAXIALL' GROWN SOURCE AND DRAIN REGIONS FREESCALE SEMICONDUCTOR, INC. TW 097106129 SEMICONDUCTOR DEVICE HAVING A METAL CARBIDE GATE WITH AN ELECTROPOSITIVE ELEMENT AND A METHOD OF MAKING THE SAME FREESCALE SEMICONDUCTOR, INC. TW 097107237 TRENCH FORMATION IN A SEMICONDUCTOR MATERIAL FREESCALE SEMICONDUCTOR, INC. TW 097107252 INTEGRATED CIRCUIT FUSE ARRAY FREESCALE SEMICONDUCTOR, INC. TW 097112428 METHOD FOR SELECTIVE REMOVAL OF A LAYER FREESCALE SEMICONDUCTOR, INC. TW 097112428 A FIRST INTER-LAYER DIELECTRIC STACK FOR NON- VOLATILE MEMORY FREESCALE SEMICONDUCTOR, INC. TW 09711339 ETCH METHOD IN THE MANUFACTURE OF A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097113453 SEPARATE LAYER FORMATION IN A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097115599 METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE | FREESCALE SEMICONDUCTOR, INC. | TW | 097102702 | HIGH VOLTAGE TRANSISTORS, NON-VOLATILE MEMORY |
| VOLTAGE PERFORMANCE AND A METHOD FOR FORMING TO SAME FREESCALE SEMICONDUCTOR, INC. TW 97103705 SOURCE/DRAIN STRESSOR AND METHOD THEREFOR FREESCALE SEMICONDUCTOR, INC. TW 097104336 MULTI-LAYER SOURCE/DRAIN STRESSOR FREESCALE SEMICONDUCTOR, INC. TW 097105061 FORMING A SEMICONDUCTOR DEVICE HAVING EPITAXIALL' GROWN SOURCE AND DRAIN REGIONS FREESCALE SEMICONDUCTOR, INC. TW 097106129 SEMICONDUCTOR DEVICE HAVING A METHOD OF MAKING THE SAME FREESCALE SEMICONDUCTOR, INC. TW 097106322 ELECTRONIC DEVICE INCLUDING CHANNEL REGIONS LYING AT DIFFERENT ELEVATIONS AND PROCESSES OF FORMING THE SAME FREESCALE SEMICONDUCTOR, INC. TW 097107237 TRENCH FORMATION IN A SEMICONDUCTOR MATERIAL FREESCALE SEMICONDUCTOR, INC. TW 097107252 INTEGRATED CIRCUIT FUSE ARRAY FREESCALE SEMICONDUCTOR, INC. TW 097112158 METHOD FOR SELECTIVE REMOVAL OF A LAYER FREESCALE SEMICONDUCTOR, INC. TW 097112428 A FIRST INTER-LAYER DIELECTRIC STACK FOR NON- VOLATILE MEMORY FREESCALE SEMICONDUCTOR, INC. TW 097113393 ETCH METHOD IN THE MANUFACTURE OF A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 09711353 SEPARATE LAYER FORMATION IN A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097115489 SEMICONDUCTOR WAFER PROCESSING FREESCALE SEMICONDUCTOR, INC. TW 097115593 METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE | FREESCALE SEMICONDUCTOR, INC. | TW | 097103578 | ELECTRONIC DEVICE WITH CONNECTION BUMPS |
| FREESCALE SEMICONDUCTOR, INC. TW 097105361 MULTI-LAYER SOURCE/DRAIN STRESSOR FREESCALE SEMICONDUCTOR, INC. TW 097105061 FORMING A SEMICONDUCTOR DEVICE HAVING EPITAXIALL' GROWN SOURCE AND DRAIN REGIONS FREESCALE SEMICONDUCTOR, INC. TW 097106129 SEMICONDUCTOR DEVICE HAVING A METAL CARBIDE GATE WITH AN ELECTROPOSITIVE ELEMENT AND A METHOD OF MAKING THE SAME FREESCALE SEMICONDUCTOR, INC. TW 097106322 ELECTRONIC DEVICE INCLUDING CHANNEL REGIONS LYING AT DIFFERENT ELEVATIONS AND PROCESSES OF FORMING THE SAME FREESCALE SEMICONDUCTOR, INC. TW 097107237 TRENCH FORMATION IN A SEMICONDUCTOR MATERIAL FREESCALE SEMICONDUCTOR, INC. TW 097107252 INTEGRATED CIRCUIT FUSE ARRAY FREESCALE SEMICONDUCTOR, INC. TW 097112428 METHOD FOR SELECTIVE REMOVAL OF A LAYER FREESCALE SEMICONDUCTOR, INC. TW 097113393 ETCH METHOD IN THE MANUFACTURE OF A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097113393 SEPARATE LAYER FORMATION IN A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097113393 SEPARATE LAYER FORMATION IN A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097115489 SEMICONDUCTOR WAFER PROCESSING FREESCALE SEMICONDUCTOR, INC. TW 097115593 METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE | FREESCALE SEMICONDUCTOR, INC. | TW | 97103703 | MICROELECTRONIC ASSEMBLY WITH IMPROVED ISOLATION VOLTAGE PERFORMANCE AND A METHOD FOR FORMING THE SAME |
| FREESCALE SEMICONDUCTOR, INC. TW 097105061 FORMING A SEMICONDUCTOR DEVICE HAVING EPITAXIALL' GROWN SOURCE AND DRAIN REGIONS FREESCALE SEMICONDUCTOR, INC. TW 097106129 SEMICONDUCTOR DEVICE HAVING A METAL CARBIDE GATE WITH AN ELECTROPOSITIVE ELEMENT AND A METHOD OF MAKING THE SAME FREESCALE SEMICONDUCTOR, INC. TW 097106322 ELECTRONIC DEVICE INCLUDING CHANNEL REGIONS LYING AT DIFFERENT ELEVATIONS AND PROCESSES OF FORMING THE SAME FREESCALE SEMICONDUCTOR, INC. TW 097107237 TRENCH FORMATION IN A SEMICONDUCTOR MATERIAL FREESCALE SEMICONDUCTOR, INC. TW 097107252 INTEGRATED CIRCUIT FUSE ARRAY FREESCALE SEMICONDUCTOR, INC. TW 97112158 METHOD FOR SELECTIVE REMOVAL OF A LAYER FREESCALE SEMICONDUCTOR, INC. TW 097112428 A FIRST INTER-LAYER DIELECTRIC STACK FOR NON- VOLATILE MEMORY FREESCALE SEMICONDUCTOR, INC. TW 097113393 ETCH METHOD IN THE MANUFACTURE OF A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097114353 SEPARATE LAYER FORMATION IN A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097115489 SEMICONDUCTOR WAFER PROCESSING FREESCALE SEMICONDUCTOR, INC. TW 097115593 METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE | FREESCALE SEMICONDUCTOR, INC. | TW | 97103705 | SOURCE/DRAIN STRESSOR AND METHOD THEREFOR |
| GROWN SOURCE AND DRAIN REGIONS FREESCALE SEMICONDUCTOR, INC. TW 097106129 SEMICONDUCTOR DEVICE HAVING A METAL CARBIDE GATE WITH AN ELECTROPOSITIVE ELEMENT AND A METHOD OF MAKING THE SAME FREESCALE SEMICONDUCTOR, INC. TW 097106322 ELECTRONIC DEVICE INCLUDING CHANNEL REGIONS LYING AT DIFFERENT ELEVATIONS AND PROCESSES OF FORMING THE SAME FREESCALE SEMICONDUCTOR, INC. TW 097107237 TRENCH FORMATION IN A SEMICONDUCTOR MATERIAL FREESCALE SEMICONDUCTOR, INC. TW 097107252 INTEGRATED CIRCUIT FUSE ARRAY FREESCALE SEMICONDUCTOR, INC. TW 097112428 METHOD FOR SELECTIVE REMOVAL OF A LAYER FREESCALE SEMICONDUCTOR, INC. TW 097112428 A FIRST INTER-LAYER DIELECTRIC STACK FOR NON-VOLATILE MEMORY FREESCALE SEMICONDUCTOR, INC. TW 097113393 ETCH METHOD IN THE MANUFACTURE OF A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097114353 SEPARATE LAYER FORMATION IN A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097115489 SEMICONDUCTOR WAFER PROCESSING FREESCALE SEMICONDUCTOR, INC. TW 097115593 METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE | FREESCALE SEMICONDUCTOR, INC. | TW | 097104336 | MULTI-LAYER SOURCE/DRAIN STRESSOR |
| WITH AN ELECTROPOSITIVE ELEMENT AND A METHOD OF MAKING THE SAME FREESCALE SEMICONDUCTOR, INC. TW 097106322 ELECTRONIC DEVICE INCLUDING CHANNEL REGIONS LYING AT DIFFERENT ELEVATIONS AND PROCESSES OF FORMING THE SAME FREESCALE SEMICONDUCTOR, INC. TW 097107237 TRENCH FORMATION IN A SEMICONDUCTOR MATERIAL FREESCALE SEMICONDUCTOR, INC. TW 097107252 INTEGRATED CIRCUIT FUSE ARRAY FREESCALE SEMICONDUCTOR, INC. TW 097112158 METHOD FOR SELECTIVE REMOVAL OF A LAYER A FIRST INTER-LAYER DIELECTRIC STACK FOR NON-VOLATILE MEMORY FREESCALE SEMICONDUCTOR, INC. TW 097113393 ETCH METHOD IN THE MANUFACTURE OF A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097114353 SEPARATE LAYER FORMATION IN A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097115489 SEMICONDUCTOR WAFER PROCESSING FREESCALE SEMICONDUCTOR, INC. TW 097115593 METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE | FREESCALE SEMICONDUCTOR, INC. | TW | 097105061 | FORMING A SEMICONDUCTOR DEVICE HAVING EPITAXIALLY GROWN SOURCE AND DRAIN REGIONS |
| AT DIFFERENT ELEVATIONS AND PROCESSES OF FORMING THE SAME FREESCALE SEMICONDUCTOR, INC. TW 097107237 TRENCH FORMATION IN A SEMICONDUCTOR MATERIAL FREESCALE SEMICONDUCTOR, INC. TW 097107252 INTEGRATED CIRCUIT FUSE ARRAY FREESCALE SEMICONDUCTOR, INC. TW 097112158 METHOD FOR SELECTIVE REMOVAL OF A LAYER FREESCALE SEMICONDUCTOR, INC. TW 097112428 A FIRST INTER-LAYER DIELECTRIC STACK FOR NON-VOLATILE MEMORY FREESCALE SEMICONDUCTOR, INC. TW 097113393 ETCH METHOD IN THE MANUFACTURE OF A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097114353 SEPARATE LAYER FORMATION IN A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097115489 SEMICONDUCTOR WAFER PROCESSING FREESCALE SEMICONDUCTOR, INC. TW 097115593 METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE | FREESCALE SEMICONDUCTOR, INC. | TW | 097106129 | |
| FREESCALE SEMICONDUCTOR, INC. TW 097107252 INTEGRATED CIRCUIT FUSE ARRAY FREESCALE SEMICONDUCTOR, INC. TW 97112158 METHOD FOR SELECTIVE REMOVAL OF A LAYER FREESCALE SEMICONDUCTOR, INC. TW 097112428 A FIRST INTER-LAYER DIELECTRIC STACK FOR NON- VOLATILE MEMORY FREESCALE SEMICONDUCTOR, INC. TW 097113393 ETCH METHOD IN THE MANUFACTURE OF A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097114353 SEPARATE LAYER FORMATION IN A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097115489 SEMICONDUCTOR WAFER PROCESSING FREESCALE SEMICONDUCTOR, INC. TW 097115593 METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE | FREESCALE SEMICONDUCTOR, INC. | TW | 097106322 | |
| FREESCALE SEMICONDUCTOR, INC. TW 97112158 METHOD FOR SELECTIVE REMOVAL OF A LAYER FREESCALE SEMICONDUCTOR, INC. TW 097112428 A FIRST INTER-LAYER DIELECTRIC STACK FOR NON- VOLATILE MEMORY FREESCALE SEMICONDUCTOR, INC. TW 097113393 ETCH METHOD IN THE MANUFACTURE OF A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097114353 SEPARATE LAYER FORMATION IN A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097115489 SEMICONDUCTOR WAFER PROCESSING FREESCALE SEMICONDUCTOR, INC. TW 097115593 METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE | FREESCALE SEMICONDUCTOR, INC. | TW | 097107237 | TRENCH FORMATION IN A SEMICONDUCTOR MATERIAL |
| FREESCALE SEMICONDUCTOR, INC. TW 097112428 A FIRST INTER-LAYER DIELECTRIC STACK FOR NON-VOLATILE MEMORY FREESCALE SEMICONDUCTOR, INC. TW 097113393 ETCH METHOD IN THE MANUFACTURE OF A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097114353 SEPARATE LAYER FORMATION IN A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097115489 SEMICONDUCTOR WAFER PROCESSING FREESCALE SEMICONDUCTOR, INC. TW 097115593 METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE | FREESCALE SEMICONDUCTOR, INC. | TW | 097107252 | INTEGRATED CIRCUIT FUSE ARRAY |
| VOLATILE MEMORY FREESCALE SEMICONDUCTOR, INC. TW 097113393 ETCH METHOD IN THE MANUFACTURE OF A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097114353 SEPARATE LAYER FORMATION IN A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097115489 SEMICONDUCTOR WAFER PROCESSING FREESCALE SEMICONDUCTOR, INC. TW 097115593 METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE | FREESCALE SEMICONDUCTOR, INC. | TW | 97112158 | METHOD FOR SELECTIVE REMOVAL OF A LAYER |
| SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097114353 SEPARATE LAYER FORMATION IN A SEMICONDUCTOR DEVICE FREESCALE SEMICONDUCTOR, INC. TW 097115489 SEMICONDUCTOR WAFER PROCESSING FREESCALE SEMICONDUCTOR, INC. TW 097115593 METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE | FREESCALE SEMICONDUCTOR, INC. | TW | 097112428 | |
| FREESCALE SEMICONDUCTOR, INC. TW 097115489 SEMICONDUCTOR WAFER PROCESSING FREESCALE SEMICONDUCTOR, INC. TW 097115593 METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE | FREESCALE SEMICONDUCTOR, INC. | TW | 097113393 | |
| FREESCALE SEMICONDUCTOR, INC. TW 097115593 METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE | FREESCALE SEMICONDUCTOR, INC. | TW | 097114353 | SEPARATE LAYER FORMATION IN A SEMICONDUCTOR DEVICE |
| | FREESCALE SEMICONDUCTOR, INC. | TW | 097115489 | SEMICONDUCTOR WAFER PROCESSING |
| | FREESCALE SEMICONDUCTOR, INC. | TW | 097115593 | |

| FREESCALE SEMICONDUCTOR, INC. | TW | 097115990 | LOW VOLTAGE DATA PATH IN MEMORY ARRAY |
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| FREESCALE SEMICONDUCTOR, INC. | TW | 097117315 | POWER LEAD-ON-CHIP BALL GRID ARRAY PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 97117841 | MULTIPLE MILLISECOND ANNEALS FOR SEMICONDUCTOR DEVICE FABRICATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 97118679 | METHOD FOR FORMING A DUAL METAL GATE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097119398 | METHOD OF FORMING A SEMICONDUCTOR DEVICE FEATURING A GATE STRESSOR AND SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097119553 | METHOD FOR FORMING A DUAL METAL GATE STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097119936 | ONE TIME PROGRAMMABLE ELEMENT SYSTEM IN AN INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097120502 | METHODS AND APPARATUS FOR EMI SHIELDING IN MULTI- CHIP MODULES |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097121961 | DYNAMIC VOLTAGE ADJUSTMENT FOR MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097122449 | SOURCE/DRAIN STRESSORS FORMED USING IN-SITU EPITAXIAL GROWTH |
| FREESCALE SEMICONDUCTOR, INC. | TW | 97125670 | COUPLING LAYER COMPOSITION FOR A SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE, METHOD OF FORMING THE COUPLING LAYER, AND APPARATUS FOR THE MANUFACTURE OF A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097125950 | HETERO-STRUCTURE FIELD EFFECT TRANSISTOR, INTEGRATED CIRCUIT INCLUDING A HETERO-STRUCTURE FIELD EFFECT TRANSISTOR AND METHOD FOR MANUFACTURING A HETERO-STRUCTURE FIELD EFFECT TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097126122 | SYMMETRICAL DIFFERENTIAL CAPACITIVE SENSOR AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097126694 | STRESS RELIEF OF A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 97126735 | INTERCONNECT IN A MULTI-ELEMENT PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097126812 | METHOD OF PACKAGING AN INTEGRATED CIRCUIT DIE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097126814 | METHOD AND CIRCUIT FOR PREVENTING HIGH VOLTAGE MEMORY DISTURB |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097127998 | SEMICONDUCTOR DEVICE TEST SYSTEM HAVING REDUCED CURRENT LEAKAGE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097129047 | DUAL GATE OXIDE DEVICE INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097131929 | PHASE CHANGE MEMORY STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097131951 | PHASE CHANGE MEMORY STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097134906 | PROGRAMMABLE ROM USING TWO BONDED STRATA AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097137045 | ELECTROMAGNETIC SHIELD FORMATION FOR INTEGRATED CIRCUIT DIE PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097137387 | INTEGRATED CIRCUIT MEMORY HAVING DYNAMICALLY ADJUSTABLE READ MARGIN AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097137798 | METHOD FOR INTEGRATING NVM CIRCUITRY WITH LOGIC CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097138301 | KNOCK SIGNAL DETECTION IN AUTOMOTIVE SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097139238 | SEMICONDUCTOR DEVICES WITH DIFFERENT DIELECTRIC |

THICKNESSES

| FREESCALE SEMICONDUCTOR, INC. | TW | 097140721 | METHOD FOR MANUFACTURING A NON-VOLATILE MEMORY, NON-VOLATILE MEMORY DEVICE, AND AN INTEGRATED CIRCUIT |
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| FREESCALE SEMICONDUCTOR, INC. | TW | 097147179 | LIQUID LEVEL SENSING DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | 97147471 | SEMICONDUCTOR DEVICE AND APPARATUS INCLUDING SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097147536 | METHOD FOR TESTING A SEMICONDUCTOR DEVICE AND A SEMICONDUCTOR DEVICE TESTING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097147540 | ERROR DETECTOR IN A CACHE MEMORY USING CONFIGURABLE WAY REDUNDANCY |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097147705 | 3-D SEMICONDUCTOR DIE STRUCTURE WITH CONTAINING FEATURE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097148059 | ELECTRONIC ASSEMBLY MANUFACTURING METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | 097151677 | MICROPAD FORMATION FOR A SEMICONDUCTOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098101409 | NON-VOLATILE MEMORY WITH REDUCED CHARGE FLUENCE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098101921 | STATE RETAINING POWER GATED LATCH AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098101922 | HIGH BANDWIDTH CACHE-TO-PROCESSING UNIT COMMUNICATION IN A MULTIPLE PROCESSOR/CACHE SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098102270 | BALUN TRANSFORMER WITH IMPROVED HARMONIC SUPRESSION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 98102531 | SHIELDED INTEGRATED CIRCUIT PAD STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098103080 | METHOD OF FORMING OPENINGS IN A SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098103728 | PERIPHERAL MODULE REGISTER ACCESS METHODS AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098103730 | MICROELECTROMECHANICAL SYSTEMS COMPONENT AND METHOD OF MAKING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | 98103850 | INTERMEDIATE PRODUCT FOR A MULTICHANNEL FET AND PROCESS FOR OBTAINING AN INTERMEDIATE PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098104740 | QUALIFICATION OF CONDITIONAL DEBUG INSTRUCTIONS BASED ON ADDRESS |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098104996 | HYBRID TRANSISTOR BASED POWER GATING SWITCH CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098106732 | OPTICAL COMMUNICATION INTEGRATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098107175 | MULTI-VOLTAGE ELECTROSTATIC DISCHARGE PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098109788 | CIRCUIT FOR AND AN ELECTRONIC DEVICE INCLUDING A NONVOLATILE MEMORY CELL AND A PROCESS OF FORMING THE ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 98111811 | SURFACE TREATMENT IN SEMICONDUCTOR MANUFACTURING |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098112515 | TEST INTERPOSER HAVING ACTIVE CIRCUIT COMPONENT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098112880 | METHOD OF SEALING AN AIR GAP IN A LAYER OF A SEMICONDUCTOR STRUCTURE AND SEMICONDUCTOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 98116022 | BRANCH TARGET BUFFER ALLOCATION |
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| FREESCALE SEMICONDUCTOR, INC. | TW | 98116023 | SEMICONDUCTOR DEVICES WITH EXTENDED ACTIVE REGIONS |
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| FREESCALE SEMICONDUCTOR, INC. | TW | 98117715 | BURIED ASSYMETRIC JUNCTION ESD PROTECTION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098118600 | AN ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT, EQUIPMENT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098119101 | PROVISION OF EXTENDED ADDRESSING MODES IN A SINGLE INSTRUCTION MULTIPLE DATA (SIMD) DATA PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098119969 | DEBUG INSTRUCTION FOR USE IN A MULTI-THREADED DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098120721 | SEMICONDUCTOR DEVICE AND METHOD OF ELECTROSTATIC DISCHARGE PROTECTION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098120723 | MEMORY SYSTEM AND SEMICONDUCTOR DEVICE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098122069 | METHOD OF FORMING A POWER SEMICONDUCTOR DEVICE AND POWER SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098122268 | TRANSISTOR WITH GAIN VARIATION COMPENSATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098122470 | POWER MOSFET WITH A GATE STRUCTURE OF DIFFERENT MATERIAL |
| FREESCALE SEMICONDUCTOR, INC. | TW | 98123882 | MICRO CONTROLLER UNIT INCLUDING AN ERROR INDICATOR MODULE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098125047 | INTEGRATED CIRCUIT AND A METHOD FOR RECOVERING FROM A LOW-POWER PERIOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | 98125356 | SYSTEM AND METHOD FOR FETCHING INFORMATION TO A CACHE MODULE USING A WRITE BACK ALLOCATE ALGORITHM |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098126217 | DATA CONVERSION CIRCUITRY AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098126772 | INTEGRATED CIRCUIT HAVING BOOSTED ARRAY VOLTAGE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098126774 | MEMORY HAVING SELF-TIMED BIT LINE BOOST CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098133745 | ADAPTIVE IIP2 CALIBRATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098134418 | METHOD OF MAKING A SPLIT GATE MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098135303 | TRANSDUCER WITH DECOUPLED SENSING IN MUTUALLY ORTHOGONAL DIRECTIONS |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098135836 | CMOS LATCH-UP IMMUNITY |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098138144 | TECHNIQUE FOR INTERCONNECTING INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | TW | 98138216 | RF DEVICE AND METHOD WITH TRENCH UNDER BOND PAD FEATURE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098138874 | PROGRAMMABLE ERROR ACTIONS FOR A CACHE IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098139022 | METHOD OF FORMING A SEMICONDUCTOR LAYER |
| FREESCALE SEMICONDUCTOR, INC. | TW | 98140377 | TRANSISTOR POWER SWITCH DEVICE RESISTANT AGAINST REPETITIVE AVALANCHE BREAKDOWN |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098140693 | TRANSISTOR POWER SWITCH DEVICE RESISTANT AGAINST REPETITIVE AVALANCHE BREAKDOWN |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098140837 | ERROR DETECTION IN A MULTI-PROCESSOR DATA |

PROCESSING SYSTEM

| FREESCALE SEMICONDUCTOR, INC. | TW | 98142870 | HIGH POWER SEMICONDUCTOR DEVICE FOR WIRELESS APPLICATIONS AND METHOD OF FORMING A HIGH POWER SEMICONDUCTOR DEVICE |
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| FREESCALE SEMICONDUCTOR, INC. | TW | 098145607 | SUBSTRATE BONDING WITH METAL GERMANIUM SILICON MATERIAL |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098145608 | DUAL HIGH-K OXIDES WITH SiGe CHANNEL |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098145617 | CAPACITANCE-TO-VOLTAGE INTERFACE CIRCUIT, AND RELATED OPERATING METHODS |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098145618 | MEMORY HAVING NEGATIVE VOLTAGE WRITE ASSIST CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098146542 | PACKAGE ASSEMBLY AND METHOD OF TUNING A NATURAL RESONANT FREQUENCY OF A PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098146547 | CLOCK GLITCH DETECTION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 098146562 | SEMICONDUCTOR DEVICE WITH APPRAISAL CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | TW | 99100013 | CLOCK GLITCH DETECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | TW | 99100014 | OSCILLATOR CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | TW | 99102997 | SEMICONDUCTOR STRUCTURE, AN INTEGRATED CIRCUIT INCLUDING A SEMICONDUCTOR STRUCTURE AND A METHOD FOR MANUFACTURING A SEMICONDUCTOR STRUCTURE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 099110181 | ELECTRICALLY ALTERABLE CIRCUIT FOR USE IN AN INTEGRATED CIRCUIT DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 099110613 | DEBUG SIGNALING IN A MULTIPLE PROCESSOR DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | TW | 099110775 | SENSOR DEVICE WITH REDUCED PARASITIC-INDUCED ERROR |
| FREESCALE SEMICONDUCTOR, INC. | TW | 099111504 | PEAK DETECTION WITH DIGITAL CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 99111599 | ADDRESS TRANSLATION TRACE MESSAGE GENERATION FOR DEBUG |
| FREESCALE SEMICONDUCTOR, INC. | TW | 099111847 | MEMORY TESTING WITH SNOOP CAPABILITIES IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | TW | 099111861 | THROUGH SUBSTRATE VIAS |
| FREESCALE SEMICONDUCTOR, INC. | TW | 099114547 | METHOD TO CALIBRATE START VALUES FOR WRITE LEVELING IN A MEMORY SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | TW | 99115283 | INTEGRATED CIRCUIT AND INTEGRATED CIRCUIT PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 099115843 | DEVICE WITH PROXIMITY DETECTION CAPABILITY |
| FREESCALE SEMICONDUCTOR, INC. | TW | 099116392 | SILICON NITRIDE HARDSTOP ENCAPSULATION LAYER FOR ST REGION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 099117641 | METHOD AND CIRCUIT FOR CHARGING AND DISCHARGING A CIRCUIT NODE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 099118606 | NON-SNAPBACK SCR FOR ELECTROSTATIC DISCHARGE PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 099118607 | VOLTAGE TRANSLATOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | 099118803 | PROCESSOR AND METHOD FOR DYNAMIC AND SELECTIVE ALTERATION OF ADDRESS TRANSLATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 099133909 | SEMICONDUCTOR WAFER HAVING SCRIBE LANE ALIGNMENT MARKS FOR REDUCING CRACK PROPAGATION |
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| FREESCALE SEMICONDUCTOR, INC. | TW | 099140081 | VERTICAL POWER TRANSISTOR DEVICE, SEMICONDUCTOR DIE AND METHOD OF MANUFACTURING A VERTICAL POWER TRANSISTOR DEVICE |
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| FREESCALE SEMICONDUCTOR, INC. | TW | 099142440 | ELECTRICAL COUPLING OF WAFER STRUCTURES |
| FREESCALE SEMICONDUCTOR, INC. | TW | 99144198 | BOND PAD WITH MULTIPLE LAYER OVER PAD METALLIZATION AND METHOD OF FORMATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 100100687 | METHOD OF MAKING A SEMICONDUCTOR STRUCTURE USEFUL IN MAKING A SPLIT GATE NON-VOLATILE MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | TW | 100102139 | ESD PROTECTION DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | 100102942 | DATA PROCESSING SYSTEM HAVING BROWN-OUT DETECTION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | TW | 100105297 | DC to DC CONVERTER HAVING SWITCH CONTROL AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 100113045 | EMULATED ELECTRICALLY ERASABLE (EEE) MEMORY AND METHOD OF OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 100116722 | METHOD OF ASSEMBLING SEMICONDUCTOR DEVICE WITH HEAT SPREADER |
| FREESCALE SEMICONDUCTOR, INC. | TW | 100117094 | ANGLED ION IMPLANTATION IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 100123734 | CURRENT REDUCTION IN A SINGLE STAGE CYCLIC ANALOG TO DIGITAL CONVERTER WITH VARIABLE RESOLUTION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 100125820 | MONOLITHIC MICROWAVE INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | TW | 100128354 | CHARGE PUMP HAVING RAMP RATE CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | TW | 100128357 | PATTERNING A GATE STACK OF A NON-VOLATILE MEMORY (NVM) WITH SIMULTANEOUS ETCH IN NON-NVM AREA |
| FREESCALE SEMICONDUCTOR, INC. | TW | 100128969 | POLYMER CORE WIRE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 100135668 | METHODS FOR PROCESSING A SEMICONDUCTOR WAFER, A SEMICONDUCTOR WAFER AND A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 100138147 | PRESSURE SENSOR AND METHOD OF ASSEMBLING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | 101101634 | MEMORY CONTROLLER ADDRESS AND DATA PIN MULTIPLEXING |
| FREESCALE SEMICONDUCTOR, INC. | TW | 101101635 | SYNCHRONOUS DATA PROCESSING SYSTEM AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | TW | 101104084 | SEMICONDUCTOR DEVICE AND RELATED FABRICATION METHODS |
| FREESCALE SEMICONDUCTOR, INC. | TW | 101105133 | MEMS DEVICE HAVING VARIABLE GAP WIDTH AND METHOD OF MANUFACTURE |
| FREESCALE SEMICONDUCTOR, INC. | TW | 101112662 | MEMS DEVICE WITH CENTRAL ANCHOR FOR STRESS ISOLATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 101112666 | METHOD OF MAKING A SEMICONDUCTOR STRUCTURE USEFUL IN MAKING A SPLIT GATE NON-VOLATILE MEMORY CELL |
| FREESCALE SEMICONDUCTOR, INC. | TW | 101114262 | ISOLATED CAPACITORS WITHIN SHALLOW TRENCH ISOLATION |
| FREESCALE SEMICONDUCTOR, INC. | TW | 101117337 | DUAL PORT PRESSURE SENSOR |
| FREESCALE SEMICONDUCTOR, INC. | TW | 101119009 | SEMICONDUCTOR SENSOR DEVICE AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW | 101119856 | ACTIVE TILING PLACEMENT FOR IMPROVED LATCH-UP IMMUNITY |

| FREESCALE SEMICONDUCTOR, INC. | TW 101126105 | FUSED BUSS FOR PLATING FEATURES ON A SEMICONDUCTOR DIE |
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| FREESCALE SEMICONDUCTOR, INC. | TW 101126106 | SYSTEMS AND METHODS FOR DATA CONVERSION |
| FREESCALE SEMICONDUCTOR, INC. | TW 101131071 | SEMICONDUCTOR DEVICE PACKAGING HAVING PRE- ENCAPSULATION THROUGH VIA FORMATION USING LEAD FRAMES WITH ATTACHED SIGNAL CONDUITS |
| FREESCALE SEMICONDUCTOR, INC. | TW 101131628 | MOSFET MISMATCH CHARACTERIZATION CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | TW 101137031 | STACKED SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | TW 101137032 | STACKED SEMICONDUCTOR DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | TW 101137515 | METHOD OF PACKAGING SEMICONDUCTOR DIE |
| FREESCALE SEMICONDUCTOR, INC. | TW 101137519 | SEMICONDUCTOR SENSOR DEVICE AND METHOD OF PACKAGING SAME |
| FREESCALE SEMICONDUCTOR, INC. | TW 102130934 | NON-VOLATILE MEMORY (NVM) THAT USES SOFT PROGRAMMING |
| FREESCALE SEMICONDUCTOR, INC. | TW 102131427 | NVM WITH CHARGE PUMP AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | TW 102131428 | NON-VOLATILE MEMORY (NVM) WITH ADAPTIVE WRITE OPERATIONS |
| FREESCALE SEMICONDUCTOR, INC. | TW 102134103 | METHOD OF MAKING A LOGIC TRANSISTOR AND A NON-VOLATILE MEMORY (NVM) CELL |
| FREESCALE SEMICONDUCTOR, INC. | TW PCT/IB2012/052733 | INTEGRATED CIRCUIT COMPRISING AN IO BUFFER DRIVER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/CN2011/000220 | SEMICONDUCTOR DEVICE AND RELATED FABRICATION METHODS |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/EP2011/068916 | RECEIVER CIRCUIT, PHASED-ARRAY RECEIVER AND RADAL SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/FR2013/051736 | CHARGE PUMP CIRCUIT, PHASE LOCKED LOOP APPARATUS INTEGRATED CIRCUIT, AND METHOD OF MANUFACTURE OF A CHARGE PUMP |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/FR2013/051970 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/FR2013/051996 | INTEGRATED SOLID STATE MICROWAVE POWER GENERATION MODULES |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/FR2013/052043 | SAFE OPERATING AREA CHECKING METHOD AND APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/FR2013/052044 | A POWER FIELD EFFECT TRANSISTOR, A POWER FIELD EFFECT TRANSISTOR DEVICE AND A METHOD OF MANUFACTURING A POWER FIELD EFFECT TRANSISTOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/FR2013/052292 | CAN FD END-OF-FRAME DETECTOR, CAN BIT STREAM PROCESSING DEVICE, METHOD FOR DETECTING THE END OF A CAN FD FRAME, AND METHOD OF OPERATING A CAN BIT STREAM PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/FR2013/052305 | Integrated calibration circuit and a method for calibration of a filter circuit |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2010/055331 | METHOD FOR ENABLING CALIBRATION DURING START-UP OF A MICRO CONTROLLER UNIT AND INTEGRATED CIRCUIT THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/001049 | AMPLIFIERS AND RELATED INTEGRATED CIRCUITS |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/001591 | GROUND LOSS MONITORING CIRCUIT AND INTEGRATED CIRCUIT COMPRISING SAME |
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| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/001871 | INTEGRATED CIRCUIT DEVICE AND METHOD OF DYNAMICALLY MODIFYING AT LEAST ONE CHARACTERISTIC WITHIN A DIGITAL TO ANALOGUE CONVERTER MODULE |
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| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/002956 | MEMORY DEVICE AND METHOD FOR ORGANIZING A HOMOGENEOUS MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/003023 | DIRECT SEQUENCE SPREAD SPECTRUM SIGNAL RECEIVING DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/003128 | DATA PROCESSING SYSTEM AND METHOD OF CONTROLLING ACCESS TO A SHARED MEMORY UNIT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/003189 | SELF-BOOTSTRAP DRIVING CIRCUIT AND DC-DC CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/003199 | MEMORY ACCESS CONTROLLER, DATA PROCESSING SYSTEM, AND METHOD FOR MANAGING DATA FLOW BETWEEN A MEMORY UNIT AND A PROCESSING UNIT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/003210 | REFERENCE VOLTAGE GENERATING CIRCUIT, INTEGRATED CIRCUIT AND VOLTAGE OR CURRENT SENSING DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/003298 | POWER SAFETY CIRCUIT, INTEGRATED CIRCUIT DEVICE AND SAFETY CRITICAL SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/003327 | NORMALLY-OFF HIGH ELECTRON MOBILITY TRANSISTOR AND INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/003355 | INTEGRATED CIRCUIT DEVICE, CONTROLLER AREA NETWORK DRIVER MODULE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/052322 | INTEGRATED CIRCUIT DEVICE AND METHOD OF ENABLING THERMAL REGULATION WITHIN AN INTEGRATED CIRCUIT DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/052323 | VOLTAGE REGULATING CIRCUIT AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/052327 | INTEGRATED CIRCUIT DEVICE AND METHOD FOR CONTROLLING AN OPERATING MODE OF AN ON-DIE MEMORY |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/052329 | INTEGRATED CIRCUIT DEVICE AND METHOD FOR SELF- HEATING AN INTEGRATED CIRCUIT DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/052333 | INTEGRATED CIRCUIT DEVICE, VOLTAGE REGULATOR MODULE AND METHOD FOR COMPENSATING A VOLTAGE SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/052601 | INTEGRATED CIRCUIT DEVICE AND METHOD OF PERFORMING CUT-THROUGH FORWARDING OF PACKET DATA |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/052602 | INTEGRATED CIRCUIT DEVICE AND METHOD OF IMPLEMENTING POWER GATING WITHIN AN INTEGRATED CIRCUIT DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/052624 | METHOD AND DEVICE FOR ENCODING AND DECODING AN IMAGE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/053232 | PROCESSING APPARATUS AND METHOD OF SYNCHRONIZING A FIRST PROCESSING UNIT AND A SECOND PROCESSING UNIT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/053235 | SAFETY CRITICAL APPARATUS AND METHOD FOR CONTROLLING DISTRACTION OF AN OPERATOR OF A SAFETY CRITICAL APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/053237 | METHOD AND APPARATUS FOR ENCODING AN IMAGE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/053241 | METHOD AND APPARATUS FOR ENABLING AN EXECUTED CONTROL FLOW PATH THROUGH COMPUTER PROGRAM |

CODE TO BE DETERMINED

| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/053419 | SIGNALLING CIRCUIT, PROCESSING DEVICE AND SAFETY CRITICAL SYSTEM |
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| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/053554 | AN ELECTRONIC DEVICE AND A COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/053811 | INTEGRATED CIRCUIT PACKAGE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/053813 | INTEGRATED CIRCUIT DEVICE AND METHOD OF IDENTIFYING A PRESENCE OF A BROKEN CONNECTION WITHIN AN EXTERNAL SIGNAL PATH |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/053837 | INTEGRATED CIRCUIT DEVICE, MEMORY INTERFACE MODULE, DATA PROCESSING SYSTEM AND METHOD FOR PROVIDING DATA ACCESS CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/053857 | DATA PROCESSING SYSTEM AND METHOD FOR TASK SCHEDULING IN A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/054657 | MULTIMODE RAKE RECEIVER, CELLULAR BASE STATION AND CELLULAR COMMUNICATION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/054917 | METHOD OF CONTROLLING A THERMAL BUDGET OF AN INTEGRATED CIRCUIT DEVICE, AN INTEGRATED CIRCUIT, A THERMAL CONTROL MODULE AND AN ELECTRONIC DEVICE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/054925 | REAL-TIME DISTRIBUTED NETWORK MODULE, REAL-TIME DISTRIBUTED NETWORK AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/054926 | REAL-TIME DISTRIBUTED NETWORK SLAVE DEVICE, REAL- TIME DISTRIBUTED NETWORK AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/054929 | MULTI-LEVEL CLOCK SIGNAL DISTRIBUTION NETWORK AND INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/055213 | CLOCK SIGNAL GENERATOR MODULE, INTEGRATED CIRCUIT, ELECTRONIC DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/055231 | INTEGRATED CIRCUIT, INTEGRATED CIRCUIT PACKAGE AND METHOD OF PROVIDING PROTECTION AGAINST AN ELECTROSTATIC DISCHARGE EVENT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/055253 | SYSTEM-ON-CHIP, METHOD OF MANUFACTURE THEREOF AND METHOD OF CONTROLLING A SYSTEM-ON-CHIP |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/055298 | CONTROLLER, SATA SYSTEM AND METHOD OF OPERATION THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/055326 | INTEGRATED CIRCUIT DEVICE, ASYMMETRIC MULTI-CORE PROCESSING MODULE, ELECTRONIC DEVICE AND METHOD OF MANAGING EXECUTION OF COMPUTER PROGRAM CODE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/055417 | METHOD FOR PLACING OPERATIONAL CELLS IN A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2011/055488 | METHOD, DEVICE AND COMPUTER PROGRAM PRODUCT FOR MEASURING USER PERCEPTION QUALITY OF A PROCESSING SYSTEM COMPRISING A USER INTERFACE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/000246 | OVER-CURRENT PROTECTION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/000247 | AN INTEGRATED CIRCUIT DEVICE AND A METHOD FOR PROVIDING ESD PROTECTION |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/000359 | DC TO DC CONVERTER AND METHOD TO OPERATE A DC TO DC CONVERTER |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/000543 | ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT ARRANGEMENT, ELECTRONIC CIRCUIT AND ESD PROTECTION METHOD |

| FREESCALE SEMICONDUCTOR, INC. | WO_PCT/IB2012/000661 | METHOD AND APPARATUS FOR PERFORMING INTEGRATED |
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| | | CIRCUIT LAYOUT VERIFICATION |
| FREESCALE SEMICONDUCTOR, INC. | | DISPLAY CONTROLLER WITH BLENDING STAGE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001066 | ELECTRONIC DEVICE AND METHOD FOR MAINTAINING FUNCTIONALITY OF AN INTEGRATED CIRCUIT DURING ELECTRICAL AGGRESSIONS |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001185 | ELECTRONIC DEVICE HAVING A PIN FOR SETTING ITS MODE OF OPERATION AND METHOD TO SET A MODE OF OPERATION FOR AN ELECTRONIC DEVICE HAVING A PIN |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001186 | HEATING SYSTEM AND METHOD OF TESTING A SEMICONDUCTOR DEVICE USING A HEATING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001195 | A SIMULATION SYSTEM AND METHOD FOR TESTING A SIMULATION OF A DEVICE AGAINST ONE OR MORE VIOLATION RULES |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001207 | CLOCK FOR SERIAL COMMUNICATION DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001208 | A PACKAGED SEMICONDUCTOR DEVICE, A SEMICONDUCTOR DEVICE AND A METHOD OF MANUFACTURING A PACKAGED SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001209 | A PIN ENTRY DEVICE, A USER IDENTIFICATION TERMINAL AND A METHOD OF OBTAINING A PIN CODE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001270 | METHOD AND APPARATUS FOR CHARGING A BOOTSTRAP CHARGE STORAGE DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001289 | SWITCH MODE POWER SUPPLY |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001449 | A DIGITAL SAMPLE CLOCK GENERATOR, A VIBRATION GYROSCOPE CIRCUITRY COMPRISING SUCH DIGITAL SAMPLE CLOCK GENERATOR, AN ASSOCIATED APPARATUS, AN ASSOCIATED SEMICONDUCTOR DEVICE AND ASSOCIATED METHODS |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001562 | CAPACITIVE ARRANGEMENT FOR FREQUENCY SYNTHESIZERS |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001563 | VOLTAGE RECULATOR CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001565 | LINEAR VOLTAGE REGULATOR DEVICE AND ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001608 | LINEAR POWER REGULATOR DEVICE AND ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001611 | A PROTECTION CIRCUIT AND A GATE DRIVING CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001650 | A SEMICONDUCTOR DEVICE COMPRISING AN ESD PROTECTION DEVICE, AN ESD PROTECTION CIRCUITRY, AN INTEGRATED CIRCUIT AND A METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001660 | CALIBRATION ARRANGEMENT FOR FREQUENCY SYNTHESIZERS |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001774 | A SEMICONDUCTOR DEVICE COMPRISING AN ESD PROTECTION DEVICE, AN ESD PROTECTION CIRCUITRY, AN INTEGRATED CIRCUIT AND A METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001815 | AUDIO UNIT AND METHOD FOR GENERATING A SAFETY CRITICAL AUDIO SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001817 | MICRO-ELECTRO-MECHANICAL SYSTEM DRIVE-MODE OSCILLATOR MODULE AND METHOD THEREFOR |

| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001818 SAMPLE-AND-HOLD CIRCUIT, CAPACITIVE SENSING DEVICE, AND METHOD OF OPERATING A SAMPLE-AND-HOLD CIRCUIT |
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| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/001960 DIFFERENTIAL LINE DRIVER CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/002020 A SIMULATION SYSTEM AND METHOD FOR TESTING A SIMULATION OF A DEVICE AGAINST ONE OR MORE VIOLATION RULES |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/002021 POWER SWITCHING DEVICE, THREE PHASE BRIDGE INVERTER, AND METHOD OF OPERATING A POWER SWITCHING DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/002022 RECEIVER UNIT AND METHOD FOR CORRECTING A VALUE OF A RECEIVE SIGNAL STRENGTH INDICATOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/002023 A SEMICONDUCTOR DEVICE AND AN INTEGRATED CIRCUIT COMPRISING AN ESD PROTECTION DEVICE, ESD PROTECTION DEVICES AND A METHOD OF MANUFACTURING THE SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/002024 A CHARGING CIRCUIT, AN INDUCTIVE LOAD CONTROL CIRCUIT, AN INTERNAL COMBUSTION ENGINE, A VEHICLE AND A METHOD OF CHARGING A BOOTSTRAP STORAGE ELEMENT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/002224 POWER SUPPLY CONTROL DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/002333 METHOD AND SYSTEM FOR TESTING A SEMICONDUCTOR DEVICE AGAINST ELECTROSTATIC DISCHARGE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/002336 METHOD AND APPARATUS FOR REPORTING TRAFFIC INFORMATION |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/002341 AN INDUCTIVE LOAD CONTROL CIRCUIT, A BRAKING SYSTEM FOR A VEHICLE AND A METHOD OF MEASURING CURRENT IN AN INDUCTIVE LOAD CONTROL CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/002427 HIGH BANDWIDTH CURRENT SENSOR AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/002539 INTEGRATED CIRCUIT DEVICE, SAFETY CIRCUIT, SAFETY- CRITICAL SYSTEM AND METHOD OF MANUFACTURING AN INTEGRATED CIRCUIT DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/002652 AMPLIFICATION STAGE AND WIDEBAND POWER AMPLIFIER |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/002653 METHOD AND APPARATUS FOR DRIVING A POWER TRANSISTOR GATE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/002654 SELF-POWERED GATE DRIVE CIRCUIT APPARATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/002655 START-UP TECHNIQUE AND SYSTEM FOR A SELF-POWERED GATE DRIVE CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/002664 METHOD AND APPARATUS FOR GENERATING A PROOF-MASS DRIVE SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/002670 TEMPERATURE COEFFICIENT FACTOR CIRCUIT, SEMICONDUCTOR DEVICE, AND RADAR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/050283 ON-DIE CAPACITANCE MEASUREMENT MODULE AND METHOD FOR MEASURING AN ON-DIE CAPACITIVE LOAD |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/050856 A SEMICONDUCTOR DEVICE COMPRISING AN OUTPUT DRIVER CIRCUITRY, A PACKAGED SEMICONDUCTOR DEVICE AND ASSOCIATED METHODS |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/050867 CLOCK DISTRIBUTION MODULE, SYNCHRONOUS DIGITAL SYSTEM AND METHOD THEREFOR |

| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/050899 | METHOD OF DETECTING IRREGULAR CURRENT FLOW IN AN INTEGRATED CIRCUIT DEVICE AND APPARATUS THEREFOR |
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| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/050901 | MICROPROCESSOR, AND METHOD OF MANAGING RESET EVENTS THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/050948 | DEBUGGING METHOD AND COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/051140 | INTERRUPT SUPERVISION SYSTEM, PROCESSING SYSTEM AND METHOD FOR INTERRUPT SUPERVISON |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/051701 | DIAGNOSTIC DATA GENERATION APPARATUS, INTEGRATED CIRCUIT AND METHOD OF GENERATING DIAGNOSTIC DATA |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/051993 | AN OSCILLATOR CIRCUIT, A SEMICONDUCTOR DEVICE AND AN APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/051997 | A DYNAMIC FREQUENCY DIVIDER CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/051998 | INFORMATION PROCESSING DEVICE AND METHOD FOR PROTECTING DATA IN A CALL STACK |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/052010 | A COMPUTER SYSTEM AND A METHOD FOR GENERATING AN OPTIMIZED PROGRAM CODE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/052024 | A SEMICONDUCTOR DEVICE ARRANGEMENT, A METHOD OF ANALYSING A PERFORMANCE OF A FUNCTIONAL CIRCUIT ON A SEMICONDUCTOR DEVICE AND A DEVICE ANALYSIS SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/052037 | DATA PROCESSING SYSTEM AND METHOD FOR OPERATING A DATA PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/052091 | A CUT-THROUGH FORWARDING MODULE AND A METHOD OF RECEIVING AND TRANSMITTING DATA FRAMES IN A CUT-THROUGH FORWARDING MODE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/052093 | METHOD AND SYSTEM FOR GENERATING A MEMORY TRACE OF A PROGRAM CODE EXECUTABLE ON A PROGRAMMABLE TARGET |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/052180 | SYSTEM-ON-CHIP, METHOD OF MANUFACTURE THEREOF AND METHOD OF COMMUNICATING DIAGNOSTIC DATA |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/052669 | PROCESSING SYSTEM AND METHOD OF INSTRUCTION SET ENCODING SPACE UTILIZATION |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/052682 | ELECTRONIC DEVICE AND METHOD FOR OPERATING A POWER SWITCH |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/052696 | IO DRIVER IMPEDANCE CALIBRATION |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/052700 | SEQUENTIAL LOGIC CIRCUIT AND METHOD OF PROVIDING SETUP TIMING VIOLATION TOLERANCE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/052715 | A SEMICONDUCTOR DEVICE AND A METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/052733 | INTEGRATED CIRCUIT COMPRISING AN IO BUFFER DRIVER AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/052779 | SCHEDULING MODULE AND METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/052879 | BUILT-IN SELF TEST SYSTEM, SYSTEM ON A CHIP AND METHOD FOR CONTROLLING BUILT-IN SELF TESTS |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/053028 | MEMORY CONTROLLER, COMPUTING DEVICE WITH A MEMORY CONTROLLER, AND METHOD FOR CALIBRATING DATA TRANSFER OF A MEMORY SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/053360 | ETHERCAT PACKET FORWARDING WITH DISTRIBUTED |

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| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/053371 PHASE SWITCHABLE BISTABLE MEMORY DEVICE, A FREQUENCY DIVIDER AND A RADIO FREQUENCY TRANSCEIVER |
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| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/053383 CUT THROUGH PACKET FORWARDING DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/053384 A COMMUNICATION DEVICE FOR WIDEBAND CODE DIVISION MULTIPLE ACCESS COMMUNICATION (W-CDMA) SYSTEM, A METHOD FOR USE THEREIN AND AN ASSOCIATED SEMICONDUCTOR DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/053385 METHOD AND APPARATUS FOR MANAGING A THERMAL BUDGET OF AT LEAST A PART OF A PROCESSING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/053386 DATA PATH CONFIGURATION COMPONENT, SIGNAL PROCESSING DEVICE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/053471 INPUT/OUTPUT DRIVER CIRCUIT, INTEGRATED CIRCUIT AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/053472 AN ELECTRONIC DEVICE FOR PROXIMITY DETECTION, A LIGHT EMITTING DIODE FOR SUCH ELECTRONIC DEVICE, A CONTROL UNIT FOR SUCH ELECTRONIC DEVICE, AN APPARATUS COMPRISING SUCH ELECTRONIC DEVICE AND AN ASSOCIATED METHOD |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/053473 A METHOD OF SENSING A USER INPUT TO A CAPACITIVE TOUCH SENSOR, A CAPACITIVE TOUCH SENSOR CONTROLLER, AN INPUT DEVICE AND AN APPARATUS |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/053677 SYSTEM ON A CHIP, APPARATUS AND METHOD FOR VOLTAGE RIPPLE REDUCTION ON A POWER SUPPLY LINE OF AN INTEGRATED CIRCUIT DEVICE OPERABLE IN AT LEAST TWO MODES |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/053682 SYSTEM AND METHOD FOR ON-DIE VOLTAGE DIFFERENCE MEASUREMENT ON A PASS DEVICE, AND INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/053721 REGISTER FILE MODULE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/053864 "METHOD AND APPARATUS FOR IMPLEMENTING INSTRUMENTATION CODE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/053865 CIRCUITRY FOR A COMPUTING SYSTEM AND COMPUTING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/053866 CIRCUITRY FOR A COMPUTING SYSTEM, LSU ARRANGEMENT AND MEMORY ARRANGEMENT AS WELL AS COMPUTING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/053995 METHOD FOR PERFORMING TOUCH DETECTION AND TOUCH DETECTION MODULE THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/054048 A METHOD AND SYSTEM FOR SCROLLING A DATA SET ACROSS A SCREEN |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/054180 DATA BUS NETWORK INTERFACE MODULE AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/054244 A CIRCUIT ARRANGEMENT FOR LOGIC BUILT-IN SELF-TEST OF A SEMICONDUCTOR DEVICE AND A METHOD OF OPERATING SUCH CIRCUIT ARRANGEMENT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/054245 METHOD AND SYSTEM FOR OBTAINING RUN-TIME INFORMATION ASSOCIATED WITH EXECUTING AN EXECUTABLE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/054299 DISPLAY CONTROL UNIT AND METHOD FOR GENERATING A VIDEO SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/054737 SYSTEM-ON-CHIP DEVICE, METHOD OF PERIPHERAL ACCESS AND INTEGRATED CIRCUIT |

| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/05475 | B ELECTRONIC DEVICE AND METHOD FOR PROTECTING AN ELECTRONIC DEVICE AGAINST UNAUTHORIZED USE |
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| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/05479 | VITERBI DECODING DEVICE AND METHOD FOR DECODING A SIGNAL PRODUCED BY A CONVOLUTIONAL ENCODER |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/05480 | METHOD AND APPARATUS FOR SELECTING DATA PATH ELEMENTS FOR CLONING |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/05480 | 7 METHOD OF SIMULATING A SEMICONDUCTOR INTEGRATED CIRCUIT, COMPUTER PROGRAM PRODUCT, AND DEVICE FOR SIMULATING A SEMICONDUCTOR INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/05480 | 3 INTEGRATED CIRCUIT FOR GENERATING OR PROCESSING A RADIO FREQUENCY SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/05515 | 9 SCAN TEST SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/05516 | B DIGITAL DEVICE AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/05546 | 9 METHOD AND APPARATUS FOR MAINTAINING ALERTNESS OF AN OPERATOR OF A MANUALLY-OPERATED SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/05547 | METHOD AND APPARATUS FOR GENERATING AN INDICATOR OF A RISK LEVEL IN OPERATING SYSTEMS |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/05599 | FREQUENCY HOPPING RADIO SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/05601 | 9 METHOD AND APPARATUS FOR AT-SPEED SCAN SHIFT FREQUENCY TEST OPTIMIZATION |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/05621 | 2 METHOD AND APPARATUS FOR MAINTAINING AN ACCURATE I/O CALIBRATION CELL |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/05623 | METHOD AND APPARATUS FOR PERFORMING STATE RETENTION FOR AT LEAST ONE FUNCTIONAL BLOCK WITHIN AN IC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/05663 | PROCESSOR CORE ARRANGEMENT, COMPUTING SYSTEM AND METHODS FOR DESIGNING AND OPERATING A PROCESSOR CORE ARRANGEMENT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/05663 | DATA PROCESSING DEVICE, METHOD OF EXECUTION ERROR DETECTION AND INTEGRATED CIRCUIT |
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| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/05666 | 9 SYSTEM ON CHIP |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/05667 | 1 SYSTEM ON CHIP |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/05667 | 5 DIGITAL DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2012/05676 | 6 REDUNDANT PACKET FORWARDING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/00010 | A HOMOGENEITY DETECTION CIRCUIT, A VALVE DRIVING SYSTEM AND A METHOD OF HOMOGENEITY DETECTION IN A VALVE DRIVING SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/00010 | 4 GROUND-LOSS DETECTION CIRCUIT |
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| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/000431 DISPLAY PROCESS | PROCESSOR AND METHOD FOR DISPLAY SING |
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| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/001610 RADIO S | IGNAL DECODING AND DECODER |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/001763 TRIMMII | NG CIRCUIT FOR A SENSOR AND TRIMMING METHOD |
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| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/050151 | METHOD AND APPARATUS FOR CALCULATING DELAY TIMING VALUES FOR AN INTEGRATED CIRCUIT DESIGN |
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| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/050152 | CLOCK SOURCE, METHOD FOR DISTRIBUTING A CLOCK SIGNAL AND INTEGRATED CIRCUIT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/050153 | METHOD AND APPARATUS FOR PERFORMING LOGIC SYNTHESIS |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/050177 | METHOD AND APPARATUS FOR CALCULATING DELAY TIMING VALUES FOR AN INTEGRATED CIRCUIT DESIGN |
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| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/050181 | A METHOD AND APPARATUS FOR ADAPTIVE GRAPHICS COMPRESSION AND DISPLAY BUFFER SWITCHING |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/050184 | METHOD AND APPARATUS FOR SAMPLING A SIGNAL |
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| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/050194 | VOLTAGE CONTROLLED OSCILLATOR |
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| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/050213 | INTEGRATED CIRCUIT PROCESSOR AND METHOD OF OPERATING A INTEGRATED CIRCUIT PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/050219 | PACKET PROCESSING ARCHITECTURE AND METHOD THEREFOR |
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| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/050223 | A COMMON PUBLIC RADIO INTERFACE LANE CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/050225 | METHOD AND CONTROL DEVICE FOR RECOVERING NBTI/PBTI RELATED PARAMETER DEGRADATION IN MOSFET DEVICES |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/050257 | A METHOD OF ESTABLISHING PRE-FETCH CONTROL INFORMATION FROM AN EXECUTABLE CODE AND AN ASSOCIATED NVM CONTROLLER, A DEVICE, A PROCESSOR SYSTEM AND COMPUTER PROGRAM PRODUCTS |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/051133 | A METHOD OF AND CIRCUITRY FOR CONTROLLING ACCESS BY A MASTER TO A PERIPHERAL, A METHOD OF CONFIGURING SUCH CIRCUITRY, AND ASSOCIATED COMPUTER PROGRAM PRODUCTS |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/051138 | ACTIVE IQ AND QUADRATURE GENERATOR FOR HIGH FREQUENCY APPLICATIONS |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/051140 | CONFIGURATION CONTROLLER FOR AND A METHOD OF CONTROLLING A CONFIGURATION OF A CIRCUITRY |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/051252 | SEARCH METHOD AND APPARATUS FOR A COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/051256 | APPARATUS, SYSTEM AND METHOD FOR CONTROLLING PACKET DATA FLOW |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/051258 | A METHOD OF OPERATING A MULTI-THREAD CAPABLE PROCESSOR SYSTEM, AN AUTOMOTIVE SYSTEM COMPRISING SUCH MULTI-THREAD CAPABLE PROCESSOR SYSTEM, AND A COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/052238 | RADAR DEVICE AND METHOD OF OPERATING A RADAR |

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| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/052302 | A HAAR CALCULATION SYSTEM, AN IMAGE CLASSIFICATION SYSTEM, ASSOCIATED METHODS AND ASSOCIATED COMPUTER PROGRAM PRODUCTS |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/052306 | A MULTI-PORT TRANSMITTER DEVICE FOR TRANSMITTING AT LEAST PARTLY REDUNDANT DATA, AN ASSOCIATED CONTROL SYSTEM, AN ASSOCIATED METHOD AND AN ASSOCIATED COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/052514 | DEVICE FOR DETERMINING A POSITION OF A ROTOR OF AN ELECTRIC MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/052519 | METHOD AND APPARATUS FOR PROCESSING DATA FLOWS |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/053171 | METHOD, COMPUTER PROGRAM PRODUCT AND CONTROLLER FOR STARTING-UP A SWITCHED RELUCTANCE MOTOR, AND ELECTRICAL APPARATUS IMPLEMENTING SAME |
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| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/053400 | DEVICE HAVING A SECURITY MODULE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/053405 | DEVICE FOR CONTROLLING A MULTI-PHASE MOTOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/053406 | CYCLING SAFETY SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/053880 | METHOD AND DEVICE FOR DETECTING A RACE CONDITION AND A COMPUTER PROGRAM PRODUCT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/053883 | MICROCONTROLLER UNIT AND METHOD OF OPERATING A MICROCONTROLLER UNIT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/053885 | METHOD AND APPARATUS FOR ENABLING TEMPORAL ALIGNMENT OF DEBUG INFORMATION |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/054437 | CELL MONITORING APPARATUS, BATTERY MONITORING APPARATUS, INTEGRATED CIRCUIT AND METHOD OF MONITORING A RECHARGEABLE CELL |
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| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/054952 | PROCESSING DEVICE AND METHOD FOR PERFORMING A ROUND OF A FAST FOURIER TRANSFORM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/054956 | DIAGNOSTIC APPARATUS, CONTROL UNIT, INTEGRATED CIRCUIT, VEHICLE AND METHOD OF RECORDING DIAGNOSTIC DATA |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/054961 | EFFICIENT SCHEDULING IN ASYNCHRONOUS CONTENTION-BASED SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/054973 | DETECTION OF DATA CORRUPTION IN A DATA PROCESSING DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/054974 | DEVICE AND METHOD FOR EXECUTING A PROGRAM, AND METHOD FOR STORING A PROGRAM |
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| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/054994 | SIGNAL PROCESSING DEVICE AND METHOD OF PERFORMING A PACK-INSERT OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/054997 | SIGNAL PROCESSING DEVICE AND METHOD OF PERFORMING A BIT-EXPAND OPERATION |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/054999 | METHOD AND APPARATUS FOR OFFLOADING FUNCTIONAL DATA FROM AN INTERCONNECT COMPONENT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/055468 | OSCILLATOR CIRCUIT AND METHOD OF GENERATING A CLOCK SIGNAL |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/055472 | METHOD AND DEVICE FOR STREAMING CONTROL DATA IN A MOBILE COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/055473 | METHOD AND DEVICE FOR DATA STREAMING IN A MOBILE COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/055637 | METHOD AND APPARATUS FOR CONTROLLING AN OPERATING MODE OF A PROCESSING MODULE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/055907 | SYSTEM ON CHIP AND METHOD THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/055911 | APPARATUS AND METHOD FOR DETERMINING IMPEDANCE CHARACTERISTICS OF AN ELECTRICAL LOAD |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/055914 | ILLEGAL MESSAGE DESTROYER |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/055918 | METHOD AND COMPUTER PROGRAM PRODUCT FOR DISASSEMBLING A MIXED MACHINE CODE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/055921 | FAULT DETECTION APPARATUS AND METHOD |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/056073 | PROCESSING DEVICE AND METHOD FOR PROTECTING A DATA PROCESSING DEVICE AGAINST TAMPERING |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/058120 | METHOD OF ESTIMATING BER VALUES IN A WIRELESS COMMUNICATION SYSTEM |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/058637 | METHOD AND APPARATUS FOR PERFORMING REGISTER ALLOCATION |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/058638 | ELECTRONIC DEVICE HAVING MULTIPLEXED INPUT/OUTPUT TERMINALS |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/058639 | METHOD OF RESETTING A PROCESSOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/058921 | LOW JITTER PULSE OUTPUT FOR POWER METER |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/058929 | HEAD-UP DISPLAY WARPING CONTROLLER |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/058935 | ELECTRONIC DEVICE AND APPARATUS AND METHOD FOR POWER MANAGEMENT OF AN ELECTRONIC DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/058937 | A SELECTIVELY POWERED LAYERED NETWORK AND A METHOD THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/IB2013/058938 | APPARATUS AND METHOD FOR OPTIMISING A CONFIGURATION OF A COMMUNICATIONS NETWORK DEVICE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/RU2011/000412 | CIRCUIT ARRANGEMENT, LIGHTING APPARATUS AND METHOD OF CROSSTALK-COMPENSATED CURRENT SENSING |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/RU2012/000160 | REFERENCE VOLTAGE SOURCE AND METHOD FOR PROVIDING A CURVATURE-COMPENSATED REFERENCE VOLTAGE |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/RU2013/000118 | VOLTAGE REGULATOR WITH IMPROVED LOAD REGULATION |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/RU2013/000272 | AUTOMATIC GENERATION OF TEST LAYOUTS FOR TESTING A DESIGN RULE CHECKING TOOL |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/RU2013/000275 | A CURRENT GENERATOR CIRCUIT AND METHOD OF CALIBRATION THEREOF |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/RU2013/000468 | METHOD OF GENERATING A TARGET LAYOUT ON THE BASIS OF A SOURCE LAYOUT |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/RU2013/000469 | PHASE DETECTOR AND PHASE-LOCKED LOOP |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/RU2013/000664 | SPREAD-SPECTRUM CLOCK GENERATION CIRCUIT, INTEGRATED CIRCUIT AND APPARATUS THEREFOR |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/US2010/041187 | RECEIVER WITH AUTOMATIC GAIN CONTROL |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/US2010/045583 | CAPACITIVE TOUCH SENSOR DEVICE CONFIGURATION SYSTEMS AND METHODS |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/US2010/049636 | SEMICONDUCTOR WAFER HAVING SCRIBE LANE ALIGNMENT MARKS FOR REDUCING CRACK PROPAGATION |
| FREESCALE SEMICONDUCTOR, INC. | WO PCT/US2013/038435 | VOLTAGE INITIALIZATION OF A MEMORY |
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SigmaTel, LLC – Registered Patents; United States

| <u>Owner</u> | Patent # | Description |
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| SIGMATEL, LLC | 5617058 | DIGITAL SIGNAL PROCESSING FOR LINEARIZATION OF SMALL INPUT SIGNALS TO A TRI-STATE POWER SWITCH |
| SIGMATEL, LLC | 5714909 | TRANSIMPEDANCE AMPLIFIER AND METHOD FOR CONSTRUCTING SAME |
| SIGMATEL, LLC | 5892800 | DATA DETECTION CIRCUIT HAVING A PRE-AMPLIFIER CIRCUIT |
| SIGMATEL, LLC | 5933040 | METHO AND APPARATUS FOR A DATA DETECTION CIRCUIT OPERATING FROM A LOW VOLTAGE POWER SOURCE |
| SIGMATEL, LLC | 5977822 | METHOD AND APPARATUS OF PULSE POSITION DEMODULATION |
| SIGMATEL, LLC | 6055283 | DATA DETECTION CIRCUIT |
| SIGMATEL, LLC | 6128354 | DATA DETECTION PRE-AMPLIFIER CIRCUIT |
| SIGMATEL, LLC | 6144473 | METHOD AND APPARATUS FOR TRANSCEIVING INFRARED SIGNALS |
| SIGMATEL, LLC | 6147634 | METHOD AND APPARATUS FOR DIGITAL TO ANALOG CONVERSION WITH REDUCED NOISE |
| SIGMATEL, LLC | 6151149 | METHOD AND APPARATUS FOR PULSE PATTERN MODULATION |
| SIGMATEL, LLC | 6163580 | METHOD AND APPARATUS FOR DATA DETECTION WITH AN ENHANCED ADAPTIVE THRESHOLD |
| SIGMATEL, LLC | 6175601 | INFRA-RED DATA PROCESSING CIRCUIT |
| SIGMATEL, LLC | 6204651 | METHOD AND APPARATUS FOR REGULATING AN OUTPUT VOLTAGE OF A SWITCH MODE CONVERTER |
| SIGMATEL, LLC | 6212230 | METHOD AND APPARATUS FOR PULSE POSITION MODULATION |
| SIGMATEL, LLC | 6329800 | METHOD AND APPARATUS FOR REDUCING POWER CONSUMPTION IN DRIVER CIRCUITS |
| SIGMATEL, LLC | 6362605 | METHOD AND APPARATUS FOR PROVIDING POWER TO AN INTEGRATED CIRCUIT |
| SIGMATEL, LLC | 6362755 | METHOD AND APPARATUS FOR SAMPLE RATE CONVERSION AND APPLICANTS THEREOF |
| SIGMATEL, LLC | 6366522 | METHOD AND APPARATUS FOR CONTROLLING POWER CONSUMPTION OF AN INTEGRATED CIRCUIT |
| SIGMATEL, LLC | 6373277 | LINE DRIVER HAVING VARIABLE IMPEDANCE TERMINATION |
| SIGMATEL, LLC | 6404172 | METHOD AND APPARATUS FOR PROVIDING INTEGRATED BUCK OR BOOST CONVERSION |
| SIGMATEL, LLC | 6430220 | DISTORTION REDUCTION METHOD AND APPARATUS FOR LINEARIZATION OF DIGITAL PULSE WIDTH MODULATION BY EFFICIENT CALCULATION |
| SIGMATEL, LLC | 6507223 | DIFFERENTIAL LINE DRIVER HAVING ADJUSTABLE COMMON MODE OPERATION |
| SIGMATEL, LLC | 6522275 | METHOD AND APPARATUS FOR SAMPLE RATE CONVERSION FOR USE IN AN ANALOG TO DIGITAL CONVERTER |
| SIGMATEL, LLC | 6522511 | HIGH SPEED ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT |
| SIGMATEL, LLC | 6526111 | METHOD AND APPARATUS FOR PHASE LOCKED LOOP HAVING REDUCED JITTER AND/OR FREQUENCY BIASING |

| SIGMATEL, LLC 6633167 METHOD AND APPRAEATUS FOR ENABLING A STAND ALONE INTEGRATE CRICUIT SIGMATEL, LLC 675306 FOR 675805 FOR 6758175 FOR 6758175 FOR ENABLING A STAND ALONE INTEGRATE CRICUIT SIGMATEL, LLC 6819677 METHOD AND APPRAEATUS FOR ENABLING DATA THAT WAS TRANSPORTED ITTILIZING MILITIPLE DATA TRANSPORT PROTOCOLS. SIGMATEL, LLC 6857031 COMPUTER PERIPHERAL DEVICE INCORPORATING INTEGRATED SIGMATEL, LLC 687468 SIGMATEL, LLC 687468 OVERVOLTAGE AND BACKFLOW CURRENT PROTECTION FOR A BATTER CHARGET SIGMATEL, LLC 687747 METHOD AND APPRAEATUS FOR RECOVERING DATA THAT WAS TRANSMISSIONS SIGMATEL, LLC 687747 METHOD AND APPRAEATUS FOR REGULATING MILITIPLE DATA TRANSPORT PROTOCOLS. SIGMATEL, LLC 687747 METHOD AND APPRAEATUS FOR REGULATING MILITIPLE OUTPUTS OF A SINGLE INDUCTURE DCTO DC CONVERTER SIGMATEL, LLC 7019895 SIGMATEL, LLC 7019895 SIGMATEL, LLC 7019896 SIGMATEL, LLC 7019895 SIGMATEL, LLC 7019895 | | | |
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| SIGMATEL, LLC SIGMAT | SIGMATEL, LLC | 6584162 | METHOD AND APPARATUS SAMPLE RATE CONVERSIONS IN AN ANALOG TO DIGITAL CONVERTER |
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| SIGMATEL, LLC 6819677 METHOD AND APPARATUS FOR RECOVERING DATA THAT WAS TRANSPORTED UTLIZED ADAT TRANSPORT PROTOCOLS SIGMATEL, LLC 682934 COMPUTER PERIPHERAL DEVICE INCORPORATING INFRARED TRANSMISSIONS OVERVOLTAGE AND BACKFLOW CURRENT PROTECTION FOR A BATTER CHARGER SIGMATEL, LLC 693139 COMPUTER AUDIO SYSTEM OVERVOLTAGE AND BACKFLOW CURRENT PROTECTION FOR A BATTER CHARGER SIGMATEL, LLC 697447 METHOD AND APPARATUS FOR REGULATING MULTIPLE OUTPUTS OF A SINGLE INDUCTOR DC TO DC CONVERTER SIGMATEL, LLC 703995 LOW THRESHOLD VOLTAGE CIRCUIT EMPLOYING A HIGH THRESHOLD VOLTAGE OUTPUT STAGE SIGMATEL, LLC 704329 PILLES EXIPPING PETH DATA OF MEDIA CONTENT SIGMATEL, LLC 705280 PILLES EXIPPING PETH DATA OF MEDIA CONTENT SIGMATEL, LLC 711622 SYSTEM AND METHOD TO RECEIVE DATA SIGMATEL, LLC 714622 INTERLEAVING OF INFORMATION INTO COMPRESSED DIGITAL AUDIO SIGMATEL, LLC 714622 INTERLEAVING OF INFORMATION INTO COMPRESSED DIGITAL AUDIO SIGMATEL, LLC 7164320 CURRENT THRESHOLD CIRCUIT SIGMATEL, LLC 7164320 CURRENT STERRED DIGITAL TO ANALOG CONVERTER WITH SIGMATEL, LLC 7164320 MEMORY PROCESSING SYSTEM AND METHODS FOR USE THEREWITH THE SIGMATEL, LLC 7164321 MEMORY PROCESSING SYSTEM AND METHODS FOR USE THEREWITH THE SIGMATEL, LLC 7164321 MEMORY PROCESSING SYSTEM AND METHODS FOR USE THEREWITH THE SIGMATEL, LLC 7164321 MEMORY PROCESSING SYSTEM AND METHODS FOR USE THEREWITH THE SIGMATEL, LLC 7164321 MEMORY PROCESSING SYSTEM AND METHODS FOR USE THEREWITH THE SIGMATEL, LLC | SIGMATEL, LLC | 6753705 | EDGE SENSITIVE DETECTION CIRCUIT |
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| TRANSMISSIONS GIGMATEL, LLC GIGMAT | SIGMATEL, LLC | 6819677 | |
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| CHARGER GEMATEL, LLC 6973447 MEHOD AND APPARATUS FOR REGULATING MULTIPLE OUTPUTS OF A SINGLE INDUCTOR DC TO DC CONVERTER GIGMATEL, LLC 703695 LOW THRESHOLD VOLTAGE CIRCUIT EMPLOYING A HIGH THRESHOLD VOLTAGE CULTUR STAGE REMOTE-DIRECTED MANAGEMENT OF MEDIA CONTENT AUDIO STREAMS REMOTE-DIRECTED MANAGEMENT OF INFORMATION INTO COMPRESSED DIGITAL AUDIO STREAMS REMOTE-DIRECTED MANAGEMENT INTERFERENCE (RFI) PRODUCED BY STREAMS REMOTE-DIRECTED AND INTERFERENCE (RFI) PRODUCED BY STREAMS REMOTE-DIRECTED AND INTERFERENCE (RFI) PRODUCED BY STREAMS REMOTE-LILC 7209069 SUCCESSIVE APPROXIMATION ANALOG-TO-DIGITAL CONVERTER WITH CURRENT STEERED DIGITAL-TO-ANALOG CONVERTER WITH SEGMATEL, LLC 721445 METHOD AND SYSTEM OF OPERATING MODE DETECTION SIGMATEL, LLC 722478 SAMPLE RATE CONVERTER WITH SELECTABLE SAMPLING RATE AND TIMEN REFERENCE SIGMATEL, LLC 723657 AUDIO CODEC ADAPTED TO DUAL BIT-STREAMS AND METHODS FOR US THEREWITH SIGMATEL, LLC 724602 FORMATEL, LLC 724602 FORMATEL, LLC 724602 FORME OF THIRZATION OF A MIXED-SIGNAL SYSTEM ON AN INTEGRATE GROWER UP AND POWER DOWN PROCESSING SYSTEM AND A PAPARATUS FOR REGULATION AND AND AND AND AND AND AND AND AND AN | SIGMATEL, LLC | 6931139 | COMPUTER AUDIO SYSTEM |
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| SIGMATEL, LLC | 7518661 | SYSTEM AND METHOD OF AUDIO DETECTION |
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| SIGMATEL, LLC | 7555591 | METHOD AND SYSTEM OF MEMORY MANAGEMENT |
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| SIGMATEL, LLC | 7599451 | SAMPLE RATE CONVERSION MODULE AND APPLICATIONS THEREOF |
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| SIGMATEL, LLC | 7620131 | DIGITAL CLOCK CONTROLLER, RADIO RECEIVER, AND METHODS FOR USE THEREWITH |
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| SIGMATEL, LLC | 7629709 | REGULATION OF A DC TO DC CONVERTER |
| SIGMATEL, LLC | 7630645 | DETECTING AN INFRARED TRANSCEIVER TYPE |
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| SIGMATEL, LLC | 7634696 | SYSTEM AND METHOD FOR TESTING MEMORY |
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| SIGMATEL, LLC | 7656968 | RADIO RECEIVER, SYSTEM ON A CHIP INTEGRATED CIRCUIT AND METHODS FOR USE THEREWITH |
| SIGMATEL, LLC | 7657725 | INTEGRATED CIRCUIT WITH MEMORY-LESS PAGE TABLE |
| SIGMATEL, LLC | 7664027 | INFRARED ADAPTER WITH DATA PACKET THROTTLE |

| SIGMATEL, LLC | 7672403 | RADIO RECEIVER, SYSTEM ON A CHIP INTEGRATED CIRCUIT AND METHODS FOR USE THEREWITH |
|---------------|---------|---|
| SIGMATEL, LLC | 7676206 | LOW NOISE, LOW DISTORTION RADIO RECEIVER FRONT-END |
| SIGMATEL, LLC | 7684515 | RADIO RECEIVER, SYSTEM ON A CHIP INTEGRATED CIRCUIT AND METHODS FOR USE THEREWITH |
| SIGMATEL, LLC | 7685333 | METHOD AND SYSTEM FOR COMMUNICATING WITH MEMORY DEVICES UTILIZING SELECTED TIMING PARAMETERS FROM A TIMING TABLE |
| SIGMATEL, LLC | 7686621 | INTEGRATED CIRCUIT TEST SOCKET HAVING ELASTIC CONTACT SUPPORTAND METHODS FOR USE THEREWITH |
| SIGMATEL, LLC | 7689807 | MASS STORAGE DEVICE, MASS STORAGE CONTROLLER AND METHODS FOR USE THEREWITH |
| SIGMATEL, LLC | 7697912 | METHOD TO ADJUSTABLY CONVERT A FIRST DATA SIGNAL HAVING A FIRST TIME DOMAIN TO A SECOND DATA SIGNAL HAVING A SECOND TIMI DOMAIN |
| SIGMATEL, LLC | 7720456 | ADJUST SWITCHING RATE OF A POWER SUPPLY TO MITIGATE INTERFERENCE |
| SIGMATEL, LLC | 7724843 | CLOCK ADJUSTMENT FOR A HANDHELD AUDIO SYSTEM |
| SIGMATEL, LLC | 7724861 | SAMPLE RATE CONVERTER |
| SIGMATEL, LLC | 7725759 | SYSTEM AND METHOD OF MANAGING CLOCK SPEED IN AN ELECTRONIC DEVICE |
| SIGMATEL, LLC | 7728660 | AUDIO SIGNAL PROCESSING SYSTEM AND METHOD |
| SIGMATEL, LLC | 7729461 | SYSTEM AND METHOD OF SIGNAL PROCESSING |
| SIGMATEL, LLC | 7729682 | RECEIVER AND METHODS FOR USE THEREWITH |
| SIGMATEL, LLC | 7739469 | PATCHING ROM CODE |
| SIGMATEL, LLC | 7752049 | INTERLEAVING OF INFORMATION INTO COMPRESSED DIGITAL AUDIO STREAMS |
| SIGMATEL, LLC | 7752373 | SYSTEM AND METHOD FOR CONTROLLING MEMORY OPERATIONS |
| SIGMATEL, LLC | 7761773 | SEMICONDUCTOR DEVICE INCLUDING A UNIQUE IDENTIFIER AND ERROR CORRECTION CODE |
| SIGMATEL, LLC | 7774079 | METHOD AND SYSTEM FOR RECEIVING AND DECODING AUDIO SIGNALS |
| SIGMATEL, LLC | 7778074 | SYSTEM AND METHOD TO CONTROL ONE TIME PROGRAMMABLE MEMORY |
| SIGMATEL, LLC | 7786698 | CHARGING A SECONDARY BATTERY |
| SIGMATEL, LLC | 7792220 | DEMODULATOR SYSTEM AND METHOD |
| SIGMATEL, LLC | 7801311 | RADIO RECEIVER WITH STEREO DECODER AND METHOD FOR USE THEREWITH |
| SIGMATEL, LLC | 7809345 | DIGITAL PLL AND APPLICATIONS THEREOF |
| SIGMATEL, LLC | 7813823 | COMPUTER AUDIO SYSTEM AND METHOD |
| SIGMATEL, LLC | 7817807 | AUDIO OUTPUT DRIVER AND METHODS FOR USE THEREWITH |
| SIGMATEL, LLC | 7821501 | TOUCH SCREEN DRIVER AND METHODS FOR USE THEREWITH |
| SIGMATEL, LLC | 7843271 | AUDIO AMPLIFIER AND METHODS FOR USE THEREWITH |
| SIGMATEL, LLC | 7844307 | WIRELESS HANDSET AND METHODS FOR USE THEREWITH |
| SIGMATEL, LLC | 7856073 | DIGITAL GAIN ADJUSTMENT IN A WIRELESS RECEIVER |
| SIGMATEL, LLC | 7856283 | DIGITAL MICROPHONE INTERFACE, AUDIO CODEC AND METHODS FOR USE THEREWITH |
| SIGMATEL, LLC | 7856464 | DECIMATION FILTER |
| SIGMATEL, LLC | 7864962 | SYSTEM AND METHOD OF ROUTING AUDIO SIGNALS TO MULTIPLE SPEAKERS |
| SIGMATEL, LLC | 7882383 | SYSTEM ON A CHIP WITH RTC POWER SUPPLY |
| SIGMATEL, LLC | 7890071 | HANDHELD AUDIO SYSTEM |
| SIGMATEL, LLC | 7894560 | PILOT TRACKING MODULE OPERABLE TO ADJUST INTERPOLATOR SAMPLE TIMING WITHIN A HANDHELD AUDIO SYSTEM |
| SIGMATEL, LLC | 7899135 | DIGITAL DECODER AND APPLICATIONS THEREOF |
| SIGMATEL, LLC | 7907664 | DIGITAL ADAPTIVE FEEDFORWARD HARMONIC DISTORTION COMPENSATION FOR DIGITALLY CONTROLLED POWER STAGE |
| SIGMATEL, LLC | 7911839 | SYSTEM AND METHOD TO CONTROL ONE TIME PROGRAMMABLE MEMORY |
| SIGMATEL, LLC | 7917788 | SOC WITH LOW POWER AND PERFORMANCE MODES |
| SIGMATEL, LLC | 7929868 | INFRARED RECEIVER, INFRARED BRIDGE DEVICE AND METHODS FOR USE THEREWITH |
| | | |

| SICMATEL LLC | 7940132 | CLOCK SYSTEM AND APPLICATIONS THEREOF |
|---------------|---------|--|
| SIGMATEL, LLC | | |
| SIGMATEL, LLC | 7949131 | DIGITAL SECURITY SYSTEM |
| SIGMATEL, LLC | 7953991 | PROCESSING SYSTEM AND METHODS FOR USE THEREWITH |
| SIGMATEL, LLC | 7966085 | AUDIO SOURCE SYSTEM AND METHOD |
| SIGMATEL, LLC | 8014533 | AUDIO OUTPUT DRIVER FOR REDUCING ELECTROMAGNETIC INTERFERENCE AND IMPROVING AUDIO CHANNEL PERFORMANCE |
| SIGMATEL, LLC | 8035368 | INTEGRATED CIRCUIT, UNIVERSAL SERIAL BUS ON-THE-GO POWER SOURCE AND METHODS FOR USE THEREWITH |
| SIGMATEL, LLC | 8055982 | ERROR CORRECTION SYSTEM AND METHOD |
| SIGMATEL, LLC | 8106892 | TOUCH SCREEN DRIVER FOR RESOLVING PLURAL CONTEMPORANEOUS TOUCHES AND METHODS FOR USE THEREWITH |
| SIGMATEL, LLC | 8130871 | INTEGRATED CIRCUIT HAVING RADIO RECEIVER AND METHODS FOR USE THEREWITH |
| SIGMATEL, LLC | 8189384 | SYSTEM AND METHOD TO CONTROL ONE TIME PROGRAMMABLE MEMORY |
| SIGMATEL, LLC | 8379730 | METHOD FOR DETERMINING DISPLAY ORDER OF VOPS IN DECODER END OF MPEG IMAGE SYSTEM AND DEVICE FOR EXECUTING THE SAME |
| SIGMATEL, LLC | 8477248 | SYSTEM AND METHOD FOR DEMODULATING AUDIO SIGNALS |
| SIGMATEL, LLC | D451899 | AUDIO PLAYER APPARATUS |
| SIGMATEL, LLC | D451900 | AUDIO PLAYER APPARATUS |
| | | |

SCHEDULE 1B (Patents)

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SigmaTel, LLC – Patent Applications; United States

| OwnerName | PatNumber | Title |
|---------------|-----------|--|
| SIGMATEL, LLC | 10/066552 | EXPANSION PERIPHERAL TECHNIQUES FOR PORTABLE AUDIO PLAYER |
| SIGMATEL, LLC | 10/614409 | METHOD FOR DETERMINING DISPLAY ORDER OF VOPS IN DECODER END OF MPEG IMAGE SYSTEM AND DEVICE FOR EXECUTING THE SAME |
| SIGMATEL, LLC | 10/865585 | FLEXIBLE MEMORY INTERFACE SYSTEM |
| SIGMATEL, LLC | 11/166872 | SYSTEM AND METHOD OF USING A PROTECTED NON-VOLATILE MEMORY |
| SIGMATEL, LLC | 11/241682 | SYSTEM AND METHOD FOR SYSTEM RESOURCE ACCESS |
| SIGMATEL, LLC | 11/265867 | POWER MANAGEMENT FOR A BETTERY-POWERED HANDHELD AUDIO DEVICE |
| SIGMATEL, LLC | 11/402648 | BUFFER CONTROLLER, CODEC AND METHODS FOR USE THEREWITH |
| SIGMATEL, LLC | 11/732737 | AUTOMATED PLAYLIST GENERATION |
| SIGMATEL, LLC | 11/796979 | GAIN CONTROL MODULE AND APPLICATIONS THEREOF |
| SIGMATEL, LLC | 12/022973 | EXPANSION PERIPHERAL TECHNIQUES FOR PORTABLE AUDIO PLAYER |
| SIGMATEL, LLC | 12/945259 | DECIMATION FILTER |
| SIGMATEL, LLC | 13/107126 | AUDIO SOURCE SYSTEM AND METHOD |
| SIGMATEL, LLC | 13/114655 | AUDIO OUTPUT DRIVER FOR REDUCING ELECTROMAGNETIC INTERFERENCE AND IMPROVING AUDIO CHANNEL PERFORMANCE |

SigmaTel, LLC – Registered Patents; Foreign

| Owner | Country | Patent # | Title |
|----------|---------|----------------|--|
| SIGMATEL | FR | 007430 | AUDIO PLAYER APPARATUS |
| SIGMATEL | FR | 012258 | AUDIO PLAYER APPARATUS |
| SIGMATEL | KR | 675414 | SYSTEM AND METHOD FOR CONFIGURING DIRECT CURRENT CONVERTER |
| SIGMATEL | KR | 743201 | HANDHELD AUDIO SYSTEM |
| SIGMATEL | KR | 747714 | SYSTEM AND METHOD OF MANAGING CLOCK SPEED IN AN ELECTRONIC DEVICE |
| SIGMATEL | KR | 842021 | SYSTEMS AND METHODS FOR DIRECT MEMORY ACCESS |
| SIGMATEL | JP | 1130523 | AUDIO PLAYER APPARATUS |
| SIGMATEL | GB | 2097902 | AUDIO PLAYER APPARATUS |
| SIGMATEL | GB | 2100567 | AUDIO PLAYER APPARATUS |
| SIGMATEL | JP | 4185456 | TIME DIVISION MULTIPLEXED PWM AMPLIFIER |
| SIGMATEL | JP | 4212647 | DIGITAL SIGNAL PROCESSING FOR LINEARIZATION OF SMALL INPUT SIGNALS TO A TRI-STATE POWER SWITCH |
| SIGMATEL | JP | 4938077 | SEMICONDUCTOR DEVICE AND SYSTEM AND METHOD OF CRYSTAL SHARING |
| SIGMATEL | JP | 5032386 | TIME DIVISION MULTIPLEXED PWM AMPLIFIER |
| SIGMATEL | DE | 40011821.1 | AUDIO PLAYER APPARATUS |
| SIGMATEL | DE | 40103345.7 | AUDIO PLAYER APPARATUS |
| SIGMATEL | CN | 200580017568.3 | SYSTEM, METHOD AND SEMICONDUCTOR DEVICR FOR CHARGING A SECONDARY BATTERY |
| SIGMATEL | CN | 200580017569 | HANDHELD AUDIO SYSTEM |
| SIGMATEL | CN | 200580017570.0 | SYSTEM AND METHOD FOR CONFIGURING DIRECT CURRENT CONVERTER |
| SIGMATEL | CN | 200580017571 | DIGITAL DECODER AND APPLICATIONS THEREOF |
| SIGMATEL | CN | 200580017574.9 | INTEGRATED CIRCUIT WITH MEMORY-LESS PAGE TABLE |
| SIGMATEL | CN | 200580020290.5 | SYSTEMS AND METHODS FOR DIRECT MEMORY ACCESS |
| SIGMATEL | CN | 200580020294.3 | SYSTEM AND METHOD OF MANAGING CLOCK SPEED IN AN ELECTRONIC DEVICE |
| SIGMATEL | CN | 200580033148 | INFRARED ADAPTER WITH DATA PACKET THROTTLE |
| SIGMATEL | CN | 200680000294 | SEMICONDUCTOR DEVICE AND SYSTEM AND METHOD OF CRYSTAL SHARING |
| SIGMATEL | CN | 200680000372.8 | SYSTEM AND METHOD TO RECEIVE DATA |
| SIGMATEL | CN | 200680000373.2 | NON-VOLATILE MEMORY |
| SIGMATEL | CN | 200680000374 | SYSTEM AN A CHIP INTEGRATED CIRCUIT, PROCESSING SYSTEM AND METHODS FOR USE THEREWITH |
| SIGMATEL | CN | 200680000375 | DIGITAL CLOCK CONTROLLER, RADIO RECEIVER, AND METHODS FOR USE THEREWITH |
| SIGMATEL | KR | 3002947490000 | AUDIO PLAYER APPARATUS |
| SIGMATEL | KR | 3003052320000 | AUDIO PLAYER APPARATUS |
| SIGMATEL | KR | 10-675418 | DIGITAL DECODER AND APPLICATIONS THEREOF |
| SIGMATEL | KR | 10-675419 | SAMPLE RATE CONVERSION MODULE AND APPLICATIONS THEREOF |
| SIGMATEL | CN | 200580017572.X | SAMPLE RATE CONVERSION MODULE AND APPLICATIONS THEREOF |
| SIGMATEL | GB | EP0859976 | ISOCHRONOUS BUFFERS FOR MMX-EQUIPPED MICROPROCESSORS |
| SIGMATEL | DE | EP0861520 | DIGITAL SIGNAL PROCESSING FOR LINEARIZATION OF SMALL INPUT SIGNALS TO A TRI-STATE POWER SWITCH |
| SIGMATEL | FR | EP0861520 | DIGITAL SIGNAL PROCESSING FOR LINEARIZATION OF SMALL INPUT SIGNALS TO A TRI-STATE POWER SWITCH |

| SIGMATEL | GB | EP0861520 | DIGITAL SIGNAL PROCESSING FOR LINEARIZATION OF SMALL INPUT SIGNALS TO A TRI-STATE POWER SWITCH |
|----------|----|-----------|---|
| SIGMATEL | FR | EP0924708 | MPEG PORTABLE SOUND REPRODUCING SYSTEM AND A REPRODUCING METHOD THEREOF |
| SIGMATEL | GB | EP0924708 | MPEG PORTABLE SOUND REPRODUCING SYSTEM AND A REPRODUCING METHOD THEREOF |
| SIGMATEL | GB | EP1000398 | ISOCHRONOUS BUFFERS FOR MMX-EQUIPPED MICROPROCESSORS |
| SIGMATEL | GB | GB2419440 | INFRARED ADAPTER WITH DATA PACKET THROTTLE |
| SIGMATEL | GB | GB2423200 | SYSTEM, METHOD AND SEMICONDUCTOR DEVICR FOR CHARGING A SECONDARY BATTERY |
| SIGMATEL | GB | GB2426162 | SAMPLE RATE CONVERSION MODULE AND APPLICATIONS THEREOF |
| SIGMATEL | GB | GB2426170 | DIGITAL DECODER AND APPLICATIONS THEREOF |
| SIGMATEL | GB | GB2426171 | HANDHELD AUDIO SYSTEM |
| SIGMATEL | GB | GB2427719 | INTEGRATED CIRCUIT WITH MEMORY-LESS PAGE TABLE |
| SIGMATEL | GB | GB2427720 | SYSTEM AND METHOD OF USING A PROTECTED NON-VOLATILE MEMORY |
| SIGMATEL | GB | GB2427723 | SYSTEM AND METHOD OF MANAGING CLOCK SPEED IN AN ELECTRONIC DEVICE |
| SIGMATEL | GB | GB2427764 | SYSTEM AND METHOD FOR CONFIGURING DIRECT CURRENT CONVERTER |
| SIGMATEL | GB | GB2431749 | SYSTEMS AND METHODS FOR DIRECT MEMORY ACCESS |
| SIGMATEL | GB | GB2444658 | SYSTEM, METHOD AND SEMICONDUCTOR DEVICR FOR CHARGING A SECONDARY BATTERY |
| SIGMATEL | GB | GB2444659 | SYSTEM, METHOD AND SEMICONDUCTOR DEVICR FOR CHARGING A SECONDARY BATTERY |
| SIGMATEL | TW | I302319 | DIGITAL DECODER AND APPLICATIONS THEREOF |
| SIGMATEL | TW | I311710 | INFRARED ADAPTER WITH DATA PACKET THROTTLE |
| SIGMATEL | TW | I312604 | SYSTEM, METHOD AND SEMICONDUCTOR DEVICR FOR CHARGING A SECONDARY BATTERY |
| SIGMATEL | TW | I312966 | SYSTEMS AND METHODS FOR DIRECT MEMORY ACCESS |
| SIGMATEL | TW | I313141 | HANDHELD AUDIO SYSTEM |
| SIGMATEL | TW | I315616 | SAMPLE RATE CONVERSION MODULE AND APPLICATIONS THEREOF |
| SIGMATEL | TW | I316782 | SYSTEM AND METHOD FOR CONFIGURING DIRECT CURRENT CONVERTER |
| SIGMATEL | TW | I321277 | SYSTEM AND METHOD OF USING A PROTECTED NON-VOLATILE MEMORY |
| SIGMATEL | TW | I331715 | INTEGRATED CIRCUIT WITH MEMORY-LESS PAGE TABLE |
| SIGMATEL | TW | I335497 | SYSTEM AND METHOD OF MANAGING CLOCK SPEED IN AN ELECTRONIC DEVICE |
| SIGMATEL | TW | I335507 | SYSTEM AND METHOD FOR ACCESSING DATA FROM A MEMORY DEVICE |
| SIGMATEL | TW | I388114 | SYSTEM AND METHOD FOR CONFIGURING DIRECT CURRENT CONVERTER |
| | | | |

${\bf SigmaTel, LLC-Patent\ Applications;\ Foreign}$

| <u>Owner</u> | Country | Application # | Description |
|--------------|---------|----------------|--|
| SIGMATEL | CN | 200680000376.6 | HANDHELD AUDIO SYSTEM WITH RADIO RECEIVER AND METHOD FOR USE THEREWITH |
| SIGMATEL | CN | 200880113890.X | TOUCH SCREEN DRIVER FOR RESOLVING PLURAL CONTEMPORANEOUS TOUCHES AND METHODS FOR USE THEREWITH |
| SIGMATEL | EP | 03771843.4 | AUTOMATED PLAYLIST GENERATION |
| SIGMATEL | JP | 2010-532105 | TOUCH SCREEN DRIVER FOR RESOLVING PLURAL CONTEMPORANEOUS TOUCHES AND METHODS FOR USE THEREWITH |

SCHEDULE 1B (Patents)

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TRADEMARKS

Freescale Semiconductor, Inc. – Registered Trademarks; United States

| <u>Owner</u> | Title | Reg. No. |
|-------------------------------|---|-----------|
| Freescale Semiconductor, Inc. | METROWERKS | 1,655.296 |
| Freescale Semiconductor, Inc. | Design (Stylized M resembling Road Barrier) | 1,676,605 |
| Freescale Semiconductor, Inc. | CODEWARRIOR | 1,981,365 |
| Freescale Semiconductor, Inc. | COLDFIRE | 2,053,242 |
| Freescale Semiconductor, Inc. | CODETEST | 2,079,931 |
| Freescale Semiconductor, Inc. | C-5 | 2,399,754 |
| Freescale Semiconductor, Inc. | C-WARE | 2,399,755 |
| Freescale Semiconductor, Inc. | PEG | 2,407,740 |
| Freescale Semiconductor, Inc. | C-PORT | 2,824,229 |
| Freescale Semiconductor, Inc. | MOBILEGT | 2,860,558 |
| Freescale Semiconductor, Inc. | POWERPARTS | 2,908,899 |
| Freescale Semiconductor, Inc. | STARCORE | 3,030,024 |
| Freescale Semiconductor, Inc. | SEAWAY NETWORKS | 3,128,609 |

| Freescale Semiconductor, Inc. | ALTIVEC | 3,142,787 |
|-------------------------------|--|-----------|
| Freescale Semiconductor, Inc. | STREAMWISE | 3,150,419 |
| Freescale Semiconductor, Inc. | STREAMWISE | 3,197,979 |
| Freescale Semiconductor, Inc. | FREESCALE | 3,259,075 |
| Freescale Semiconductor, Inc. | POWERQUICC | 3,276,522 |
| Freescale Semiconductor, Inc. | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 3,358,102 |
| Freescale Semiconductor, Inc. | Design (Rectangle) | 3,411,019 |
| Freescale Semiconductor, Inc. | CODEWARRIOR | 3,444,193 |
| Freescale Semiconductor, Inc. | Design (Rectangle) | 3,538,548 |
| Freescale Semiconductor, Inc. | SYMPHONY | 3,684,432 |
| Freescale Semiconductor, Inc. | QORIQ | 3,775,471 |
| Freescale Semiconductor, Inc. | Design (Windmill) | 3,857,413 |
| Freescale Semiconductor, Inc. | FREESCALE | 3,864,663 |
| Freescale Semiconductor, Inc. | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 3,865,943 |
| Freescale Semiconductor, Inc. | VORTIQA | 4,032,066 |
| Freescale Semiconductor, Inc. | PROCESSOR EXPERT | 4,047,406 |
| Freescale Semiconductor, Inc. | KINETIS | 4,050,155 |
| Freescale Semiconductor, Inc. | QORIVVA | 4,084,867 |
| Freescale Semiconductor, Inc. | COLDFIRE+ | 4,096,771 |
| Freescale Semiconductor, Inc. | XTRINSIC | 4,298,546 |
| Freescale Semiconductor, Inc. | FREESCALE | 4,368,539 |
| | | |

Freescale Semiconductor, Inc. – Trademark Applications; United States

| <u>Owner</u> | Title | Application. No. |
|-------------------------------|---|---------------------|
| Freescale Semiconductor, Inc. | QORIQ QONVERGE | 85/233,451 |
| Freescale Semiconductor, Inc. | READY PLAY | 85/342,240 |
| Freescale Semiconductor, Inc. | AIRFAST | 85/348,149 |
| Freescale Semiconductor, Inc. | MAGNIV | 85/348,157 |
| Freescale Semiconductor, Inc. | SAFEASSURE | 85/422,149 |
| Freescale Semiconductor, Inc. | SAFE ASSURE BY FREESCALE & Design (Horizontal Diamonds) | 85/433,915 |
| Freescale Semiconductor, Inc. | SAFE ASSURE BY FREESCALE & Design (Vertical Diamonds) | 85/433,928 |
| Freescale Semiconductor, Inc. | FREESCALE & Design (Rectangle) | 85/497,099 |
| Freescale Semiconductor, Inc. | VYBRID | 85/536,246 |
| Freescale Semiconductor, Inc. | LAYERSCAPE | 85/654,069 |
| Freescale Semiconductor, Inc. | TOWER | 85/792,032 |

Freescale Semiconductor, Inc. – Registered Trademarks; Foreign

| <u>Owner</u> | Country | Title | Reg. No. |
|-------------------------------|---|--|----------|
| Freescale Semiconductor, Inc. | African Intellectual Property Organisation | FREESCALE | 50237 |
| Freescale Semiconductor, Inc. | African Intellectual Property Organisation | FREESCALE | 50238 |
| Freescale Semiconductor, Inc. | Algeria | FREESCALE | 68028 |
| Freescale Semiconductor, Inc. | Andorra | Design (Rectangle) | 21044 |
| Freescale Semiconductor, Inc. | Andorra | FREESCALE | 21046 |
| Freescale Semiconductor, Inc. | Andorra | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 21048 |
| Freescale Semiconductor, Inc. | Argentina | DIGITAL DNA | 1708185 |
| Freescale Semiconductor, Inc. | Argentina | DIGITAL DNA | 1708188 |
| Freescale Semiconductor, Inc. | Argentina | DIGITAL DNA | 1738646 |
| Freescale Semiconductor, Inc. | Argentina | DIGITAL DNA & Design (Small Asterisk) | 1769506 |
| Freescale Semiconductor, Inc. | Argentina | LATINCHIP | 1796090 |
| Freescale Semiconductor, Inc. | Argentina | LATINCHIP | 1796091 |
| Freescale Semiconductor, Inc. | Argentina | LATINCHIP | 1796092 |
| Freescale Semiconductor, Inc. | Argentina | M.CORE | 1814168 |
| Freescale Semiconductor, Inc. | Argentina | ALTIVEC (Stylized) | 1987513 |
| Freescale Semiconductor, Inc. | Argentina | STARCORE | 1999721 |
| Freescale Semiconductor, Inc. | Argentina | Design (Rectangle) | 2043010 |
| Freescale Semiconductor, Inc. | Argentina | FREESCALE | 2064965 |
| Freescale Semiconductor, Inc. | Argentina | FREESCALE | 2064966 |
| Freescale Semiconductor, Inc. | Argentina | Design (Rectangle) | 2071986 |

| Freescale Semiconductor, Inc. | Argentina | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 2077928 |
|-------------------------------|-------------------------|--|--------------|
| Freescale Semiconductor, Inc. | Argentina | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 2134984 |
| Freescale Semiconductor, Inc. | Armenia | FREESCALE | 9576 |
| Freescale Semiconductor, Inc. | Australia | STARCORE | 609819 |
| Freescale Semiconductor, Inc. | Australia | STARCORE | 609821 |
| Freescale Semiconductor, Inc. | Australia | STARCORE | 609822 |
| Freescale Semiconductor, Inc. | Australia | STARCORE | 609823 |
| Freescale Semiconductor, Inc. | Australia | MOBILEOS | 739952 |
| Freescale Semiconductor, Inc. | Australia | DIGITAL DNA | 746023 |
| Freescale Semiconductor, Inc. | Australia | M-CORE | 753373 |
| Freescale Semiconductor, Inc. | Australia | Design (Asterisk) | 764370 |
| Freescale Semiconductor, Inc. | Australia | STARCORE | 864674 |
| Freescale Semiconductor, Inc. | Australia | ALTIVEC (Stylized) | 930965 |
| Freescale Semiconductor, Inc. | Australia | FREESCALE | 1005371 |
| Freescale Semiconductor, Inc. | Australia | Design (Rectangle) | 1018466 |
| Freescale Semiconductor, Inc. | Australia | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 1018467 |
| Freescale Semiconductor, Inc. | Azerbaijan | FREESCALE | N 2005 0178 |
| Freescale Semiconductor, Inc. | Bahrain | FREESCALE | 41755 |
| Freescale Semiconductor, Inc. | Bahrain | FREESCALE | 41756 |
| Freescale Semiconductor, Inc. | Belarus | FREESCALE | 24457 |
| Freescale Semiconductor, Inc. | Benelux | M.CORE | 624683 |
| Freescale Semiconductor, Inc. | Bolivia | FREESCALE | 99947-C |
| Freescale Semiconductor, Inc. | Bolivia | FREESCALE | 99948-C |
| Freescale Semiconductor, Inc. | Bosnia & Herzegovina | FREESCALE | BAZ047861 |
| Freescale Semiconductor, Inc. | Botswana | FREESCALE | BW/M/04/0033 |
| Freescale Semiconductor, Inc. | Brazil | DIGITAL DNA | 200047841 |
| Freescale Semiconductor, Inc. | Brazil | DIGITAL DNA | 200047850 |
| Freescale Semiconductor, Inc. | Brazil | DIGITAL DNA | 200054643 |
| Freescale Semiconductor, Inc. | Brazil | DIGITAL DNA | 200054651 |
| Freescale Semiconductor, Inc. | Brazil | STARCORE | 817448721 |
| Freescale Semiconductor, Inc. | Brazil | STARCORE | 817449264 |
| | | | |

| Freescale Semiconductor, Inc. | Brazil | STARCORE | 817449400 |
|-------------------------------|----------------------|--|-----------|
| Freescale Semiconductor, Inc. | Brazil | STARCORE | 817449418 |
| Freescale Semiconductor, Inc. | Brazil | DIGITAL DNA | 820422185 |
| Freescale Semiconductor, Inc. | Brazil | DIGITAL DNA | 820422207 |
| Freescale Semiconductor, Inc. | Brazil | DIGITAL DNA | 820442291 |
| Freescale Semiconductor, Inc. | Brazil | DIGITAL DNA & Design (Large Asterisk) | 820829234 |
| Freescale Semiconductor, Inc. | Brazil | DIGITAL DNA & Design (Small Asterisk) | 820829250 |
| Freescale Semiconductor, Inc. | Brazil | Design (Asterisk) | 820829269 |
| Freescale Semiconductor, Inc. | Brazil | Design (Asterisk) | 820829277 |
| Freescale Semiconductor, Inc. | Brazil | STARCORE | 823544516 |
| Freescale Semiconductor, Inc. | Brazil | ALTIVEC (Stylized) | 824946081 |
| Freescale Semiconductor, Inc. | Brazil | FREESCALE | 826654274 |
| Freescale Semiconductor, Inc. | Brazil | FREESCALE | 826654282 |
| Freescale Semiconductor, Inc. | Brazil | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 826714650 |
| Freescale Semiconductor, Inc. | Brazil | Design (Rectangle) | 826714668 |
| Freescale Semiconductor, Inc. | Brazil | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 826714692 |
| Freescale Semiconductor, Inc. | Brazil | Design (Rectangle) | 826714706 |
| Freescale Semiconductor, Inc. | Brazil | QORIQ | 829974750 |
| Freescale Semiconductor, Inc. | Brazil | Design (Windmill) | 830079564 |
| Freescale Semiconductor, Inc. | Brazil | Design (Windmill) | 830079572 |
| Freescale Semiconductor, Inc. | Brazil | KINETIS | 830626093 |
| Freescale Semiconductor, Inc. | Brazil | XTRINSIC | 830644989 |
| Freescale Semiconductor, Inc. | Brunei Darussalam | FREESCALE | 36308 |
| Freescale Semiconductor, Inc. | Bulgaria | FREESCALE | 54837 |
| Freescale Semiconductor, Inc. | Bulgaria | Design (Rectangle) | 55522 |
| Freescale Semiconductor, Inc. | Bulgaria | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 55793 |
| Freescale Semiconductor, Inc. | Cambodia | FREESCALE | 20206/04 |
| Freescale Semiconductor, Inc. | Cambodia | FREESCALE | 20212/04 |
| Freescale Semiconductor, Inc. | Canada | METROWERKS & M Design | 377335 |
| Freescale Semiconductor, Inc. | Canada | METROWERKS MODULA -2 | 377686 |

| Freescale Semiconductor, Inc. | Canada | STARCORE | 432880 |
|-------------------------------|-------------------|--|----------------|
| Freescale Semiconductor, Inc. | Canada | VETHER | 533182 |
| Freescale Semiconductor, Inc. | Canada | SUPERTAP | 538601 |
| Freescale Semiconductor, Inc. | Canada | M-CORE | 549245 |
| Freescale Semiconductor, Inc. | Canada | CODEOPTIX | 550816 |
| Freescale Semiconductor, Inc. | Canada | Design (Asterisk) | 563861 |
| Freescale Semiconductor, Inc. | Canada | STARCORE | 603100 |
| Freescale Semiconductor, Inc. | Canada | FREESCALE | 640267 |
| Freescale Semiconductor, Inc. | Canada | Design (Rectangle) | 640442 |
| Freescale Semiconductor, Inc. | Canada | ALTIVEC (Stylized) | 651,844 |
| Freescale Semiconductor, Inc. | Canada | FREESCALE SEMICONDUCTOR & Design (Rectangle) | TMA 652,553 |
| Freescale Semiconductor, Inc. | Canada | LIVECODE | TMA538,317 |
| Freescale Semiconductor, Inc. | Canada | SEAWAY NETWORKS | TMA633,417 |
| Freescale Semiconductor, Inc. | Canada | STREAMWISE | TMA639,136 |
| Freescale Semiconductor, Inc. | Canada | FREESCALE | TMA756,987 |
| Freescale Semiconductor, Inc. | Canada | FREESCALE | TMA756,988 |
| Freescale Semiconductor, Inc. | Canada | FREESCALE SEMICONDUCTOR & Design (Rectangle) | TMA762,026 |
| Freescale Semiconductor, Inc. | Canada | Design (Rectangle) | TMA762,424 |
| Freescale Semiconductor, Inc. | Canada | QORIQ | TMA807,840 |
| Freescale Semiconductor, Inc. | Canada | Design (Windmill) | TMA815,133 |
| Freescale Semiconductor, Inc. | Cayman Islands | FREESCALE | 2366159 |
| Freescale Semiconductor, Inc. | Cayman Islands | FREESCALE | 2366159B |
| Freescale Semiconductor, Inc. | Chile | FREESCALE | 712.025 |
| Freescale Semiconductor, Inc. | Chile | FREESCALE | 719.265 |
| Freescale Semiconductor, Inc. | Chile | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 719.266 |
| Freescale Semiconductor, Inc. | Chile | Design (Rectangle) | 719.267 |
| Freescale Semiconductor, Inc. | Chile | DIGITAL DNA | 527783 |
| Freescale Semiconductor, Inc. | Chile | DIGITAL DNA & Design (Large Asterisk) | 530660 |
| Freescale Semiconductor, Inc. | Chile | DIGITAL DNA & Design (Small Asterisk) | 530661 |
| Freescale Semiconductor, Inc. | Chile | Design (Asterisk) | 530662 |
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| Freescale Semiconductor, Inc. | Chile | Design (Asterisk) | 530663 |
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| Freescale Semiconductor, Inc. | Chile | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 714071 |
| Freescale Semiconductor, Inc. | Chile | Design (Rectangle) | 714771 |
| Freescale Semiconductor, Inc. | China | FREESCALE & Design (Rectangle) | 1132971 |
| Freescale Semiconductor, Inc. | China | M.CORE | 1286163 |
| Freescale Semiconductor, Inc. | China | Design (Asterisk) | 1366193 |
| Freescale Semiconductor, Inc. | China | DIGITAL DNA & Design (Small Asterisk) | 1366194 |
| Freescale Semiconductor, Inc. | China | DIGITAL DNA & Design (Largel Asterisk) | 1366195 |
| Freescale Semiconductor, Inc. | China | DIGITAL DNA & Device (in Chinese Characters; large asterisk) | 1393104 |
| Freescale Semiconductor, Inc. | China | DIGITAL DNA & Device (in Chinese Characters; large asterisk) | 1402124 |
| Freescale Semiconductor, Inc. | China | CCPLATFORM | 1533913 |
| Freescale Semiconductor, Inc. | China | DIGITAL DNA & Device (in Chinese Characters; small asterisk) | 1746944 |
| Freescale Semiconductor, Inc. | China | DIGITAL DNA & Device (in Chinese Characters; small asterisk) | 1746945 |
| Freescale Semiconductor, Inc. | China | ALTIVEC (Stylized) | 3357112 |
| Freescale Semiconductor, Inc. | China | FREESCALE (Simplified Chinese Characters) | 4019860 |
| Freescale Semiconductor, Inc. | China | FREESCALE (Simplified Chinese Characters) | 4019861 |
| Freescale Semiconductor, Inc. | China | FREESCALE SEMICONDUCTOR (Simplified Chinese Characters) | 4020209 |
| Freescale Semiconductor, Inc. | China | FREESCALE SEMICONDUCTOR (Simplified Chinese Characters) | 4020860 |
| Freescale Semiconductor, Inc. | China | FREESCALE | 4114568 |
| Freescale Semiconductor, Inc. | China | FREESCALE | 4114569 |
| Freescale Semiconductor, Inc. | China | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 4182594 |
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| Freescale Semiconductor, Inc. | China | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 4182595 |
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| Freescale Semiconductor, Inc. | China | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 4239509 |
| Freescale Semiconductor, Inc. | China | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 4239510 |
| Freescale Semiconductor, Inc. | China | POWERQUICC | 4774348 |
| Freescale Semiconductor, Inc. | China | STARCORE | 4973986 |
| Freescale Semiconductor, Inc. | China | STARCORE | 4973987 |
| Freescale Semiconductor, Inc. | China | STARCORE | 4973989 |
| Freescale Semiconductor, Inc. | China | CODEWARRIOR | 6513765 |
| Freescale Semiconductor, Inc. | China | QORIQ | 6939336 |
| Freescale Semiconductor, Inc. | China | Design (Windmill) | 7015798 |
| Freescale Semiconductor, Inc. | China | Design (Windmill) | 7015969 |
| Freescale Semiconductor, Inc. | China | VORTIQA | 7542127 |
| Freescale Semiconductor, Inc. | China | XTRINSIC | 8409997 |
| Freescale Semiconductor, Inc. | China | QORIVVA | 8786452 |
| Freescale Semiconductor, Inc. | China | COLDFIRE | 9314562 |
| Freescale Semiconductor, Inc. | China | Design (Rectangle) | 9358624 |
| Freescale Semiconductor, Inc. | China | Design (Rectangle) | 9358625 |
| Freescale Semiconductor, Inc. | China | READY PLAY | 9590568 |
| Freescale Semiconductor, Inc. | China | MAGNIV | 9626411 |
| Freescale Semiconductor, Inc. | China | AIRFAST | 9626412 |
| Freescale Semiconductor, Inc. | China | QORIQ QONVERGE | 9794274 |
| Freescale Semiconductor, Inc. | China | VYBRID | 10476069 |
| Freescale Semiconductor, Inc. | Colombia | M.CORE | 211362 |
| Freescale Semiconductor, Inc. | Colombia | FREESCALE | 297244 |
| Freescale Semiconductor, Inc. | Colombia | Design (Rectangle) | 297297 |
| Freescale Semiconductor, Inc. | Colombia | Design (Rectangle) | 297298 |
| Freescale Semiconductor, Inc. | Colombia | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 299032 |
| Freescale Semiconductor, Inc. | Colombia | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 299033 |
| Freescale Semiconductor, Inc. | Colombia | FREESCALE | 308768 |
| Freescale Semiconductor, Inc. | Costa Rica | DIGITAL DNA | 118564 |

| Freescale Semiconductor, Inc. | Costa Rica | Design (Rectangle) | 152170 |
|-------------------------------|-----------------------|--|------------|
| Freescale Semiconductor, Inc. | Costa Rica | FREESCALE | 153815 |
| Freescale Semiconductor, Inc. | Costa Rica | Design (Rectangle) | 154192 |
| Freescale Semiconductor, Inc. | Costa Rica | FREESCALE | 154948 |
| Freescale Semiconductor, Inc. | Costa Rica | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 154949 |
| Freescale Semiconductor, Inc. | Costa Rica | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 154951 |
| Freescale Semiconductor, Inc. | Croatia | FREESCALE | Z 20040960 |
| Freescale Semiconductor, Inc. | Cyprus | FREESCALE | 70299 |
| Freescale Semiconductor, Inc. | Cyprus | FREESCALE | 70300 |
| Freescale Semiconductor, Inc. | Cyprus | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 70411 |
| Freescale Semiconductor, Inc. | Cyprus | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 70412 |
| Freescale Semiconductor, Inc. | Cyprus | Design (Rectangle) | 70413 |
| Freescale Semiconductor, Inc. | Cyprus | Design (Rectangle) | 70414 |
| Freescale Semiconductor, Inc. | Czech Republic | PROCESSOR EXPERT | 226524 |
| Freescale Semiconductor, Inc. | Czech Republic | ALTIVEC (Stylized) | 256706 |
| Freescale Semiconductor, Inc. | Czech Republic | FREESCALE | 270918 |
| Freescale Semiconductor, Inc. | Czech Republic | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 271281 |
| Freescale Semiconductor, Inc. | Czech Republic | Design (Rectangle) | 271282 |
| Freescale Semiconductor, Inc. | Dominican Republic | FREESCALE | 145020 |
| Freescale Semiconductor, Inc. | Dominican Republic | Design (Rectangle) | 145293 |
| Freescale Semiconductor, Inc. | Dominican Republic | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 145294 |
| Freescale Semiconductor, Inc. | Ecuador | FREESCALE | 321-05 |
| Freescale Semiconductor, Inc. | Ecuador | FREESCALE | 701-05 |
| Freescale Semiconductor, Inc. | Egypt | FREESCALE | 167702 |
| Freescale Semiconductor, Inc. | Egypt | FREESCALE | 167703 |
| Freescale Semiconductor, Inc. | Egypt | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 168462 |
| Freescale Semiconductor, Inc. | Egypt | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 168463 |
| Freescale Semiconductor, Inc. | Egypt | Design (Rectangle) | 168464 |
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| Europeanla Comingradurates Inc | E | Design (Bestangle) | 100465 |
|---|-----------------------|--|----------------------|
| Freescale Semiconductor, Inc. Freescale Semiconductor, Inc. | Egypt El Salvador | Design (Rectangle) FREESCALE | 168465 17 Book 40 |
| Freescale Semiconductor, Inc. | El Salvador | FREESCALE | 72 BOOK 40 |
| Freescale Semiconductor, Inc. | Estonia | FREESCALE | 41750 |
| Freescale Semiconductor, Inc. | Estonia | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 41762 |
| Freescale Semiconductor, Inc. | Estonia | Design (Rectangle) | 41763 |
| Freescale Semiconductor, Inc. | European Community | DNA | 000294579 |
| Freescale Semiconductor, Inc. | European Community | DIGITAL DNA | 000661645 |
| Freescale Semiconductor, Inc. | European Community | CODEWARRIOR | 765,537 |
| Freescale Semiconductor, Inc. | European Community | VETHER | 830745 |
| Freescale Semiconductor, Inc. | European Community | LIVECODE | 000830752 |
| Freescale Semiconductor, Inc. | European Community | SUPERTAP | 830760 |
| Freescale Semiconductor, Inc. | European Community | DIGITAL DNA & Design (Small Asterisk) | 859058 |
| Freescale Semiconductor, Inc. | European Community | Design (Asterisk) | 859074 |
| Freescale Semiconductor, Inc. | European Community | M.CORE | 001050038 |
| Freescale Semiconductor, Inc. | European Community | FREESCALE & Design (Rectangle) | 1132971 |
| Freescale Semiconductor, Inc. | European Community | SYMPHONY | 1558204 |
| Freescale Semiconductor, Inc. | European Community | STARCORE | 2069979 |
| Freescale Semiconductor, Inc. | European Community | ALTIVEC (Stylized) | 2890879 |
| Freescale Semiconductor, Inc. | European Community | FREESCALE | 003810793 |
| Freescale Semiconductor, Inc. | European Community | Design (Rectangle) | 3810801 |
| Freescale Semiconductor, Inc. | European Community | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 3998416 |
| Freescale Semiconductor, Inc. | European Community | POWERQUICC | 4529681 |
| Freescale Semiconductor, Inc. | European Community | QORIQ | 7215701 |
| Freescale Semiconductor, Inc. | European Community | Design (Windmill) | 7334601 |
| Freescale Semiconductor, Inc. | European Community | VORTIQA | 008413148 |
| Freescale Semiconductor, Inc. | European Community | PROCESSOR EXPERT | 009087818 |
| Freescale Semiconductor, Inc. | European Community | KINETIS | 9110099 |
| Freescale Semiconductor, Inc. | European Community | XTRINSIC | 9192626 |
| Freescale Semiconductor, Inc. | European Community | QORIVVA | 9487018 |
| Freescale Semiconductor, Inc. | European | COLDFIRE | 9863697 |

| Freescale Semiconductor, Inc. | European Community | AIRFAST | 10056299 |
|-------------------------------|-----------------------|---|------------|
| Freescale Semiconductor, Inc. | European Community | MAGNIV | 10056356 |
| Freescale Semiconductor, Inc. | European Community | QORIQ QONVERGE | 10155951 |
| Freescale Semiconductor, Inc. | European Community | SAFEASSURE | 010723278 |
| Freescale Semiconductor, Inc. | European Community | LAYERSCAPE | 010971811 |
| Freescale Semiconductor, Inc. | European Community | FREESCALE TOWER SYSTEM | 011393865 |
| Freescale Semiconductor, Inc. | France | M.CORE | 97709770 |
| Freescale Semiconductor, Inc. | France | CODETEST | 96 610 447 |
| Freescale Semiconductor, Inc. | Georgia | FREESCALE | 16091 |
| Freescale Semiconductor, Inc. | Germany | SYMPHONY | 2080004 |
| Freescale Semiconductor, Inc. | Germany | MOBILEOS | 39744291 |
| Freescale Semiconductor, Inc. | Germany | M-CORE | 398038694 |
| Freescale Semiconductor, Inc. | Guatemala | DIGITAL DNA | 109725 |
| Freescale Semiconductor, Inc. | Guatemala | DIGITAL DNA | 112624 |
| Freescale Semiconductor, Inc. | Guatemala | DIGITAL DNA | 112993 |
| Freescale Semiconductor, Inc. | Guatemala | DIGITAL DNA | 114822 |
| Freescale Semiconductor, Inc. | Guatemala | DIGITAL DNA | 117843 |
| Freescale Semiconductor, Inc. | Guatemala | FREESCALE | 136322 |
| Freescale Semiconductor, Inc. | Guatemala | FREESCALE | 136327 |
| Freescale Semiconductor, Inc. | Honduras | FREESCALE | 10636 |
| Freescale Semiconductor, Inc. | Honduras | FREESCALE | 93871 |
| Freescale Semiconductor, Inc. | Hong Kong | STARCORE | 200204867 |
| Freescale Semiconductor, Inc. | Hong Kong | ALTIVEC (Stylized) | 200306870 |
| Freescale Semiconductor, Inc. | Hong Kong | FREESCALE (Traditional & Simplified Chinese Characters) | 300198441 |
| Freescale Semiconductor, Inc. | Hong Kong | FREESCALE SEMICONDUCTOR (Traditional & Simplified Chinese Characters) | 300198450 |
| Freescale Semiconductor, Inc. | Hong Kong | FREESCALE | 300231083 |
| Freescale Semiconductor, Inc. | Hong Kong | Design (Rectangle) | 300274644 |
| Freescale Semiconductor, Inc. | Hong Kong | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 300274653 |
| Freescale Semiconductor, Inc. | Hong Kong | FREESCALE & Design (Rectangle) | 302155455 |
| Freescale Semiconductor, Inc. | Hong Kong | DIGITAL DNA | B97612002 |

| Freescale Semiconductor, Inc. | Hungary | FREESCALE | 184412 |
|-------------------------------|-----------|--|--------------|
| Freescale Semiconductor, Inc. | Hungary | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 184 426 |
| Freescale Semiconductor, Inc. | Hungary | Design (Rectangle) | 184 472 |
| Freescale Semiconductor, Inc. | Iceland | FREESCALE | 183/2005 |
| Freescale Semiconductor, Inc. | India | Design (Rectangle) | 725350 |
| Freescale Semiconductor, Inc. | India | STARCORE | 741441 |
| Freescale Semiconductor, Inc. | India | QORIQ | 924707 |
| Freescale Semiconductor, Inc. | India | ALTIVEC (Stylized) | 1144726 |
| Freescale Semiconductor, Inc. | India | FREESCALE | 1291974 |
| Freescale Semiconductor, Inc. | India | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 1305967 |
| Freescale Semiconductor, Inc. | India | Design (Windmill) | 1763477 |
| Freescale Semiconductor, Inc. | India | VORTIQA | 1870316 |
| Freescale Semiconductor, Inc. | India | QORIVVA | 2046069 |
| Freescale Semiconductor, Inc. | Indonesia | FREESCALE | IDM000069200 |
| Freescale Semiconductor, Inc. | Indonesia | FREESCALE | IDM000069840 |
| Freescale Semiconductor, Inc. | Indonesia | FREESCALE SEMICONDUCTOR & Design (Rectangle) | IDM000078403 |
| Freescale Semiconductor, Inc. | Indonesia | FREESCALE SEMICONDUCTOR & Design (Rectangle) | IDM000078404 |
| Freescale Semiconductor, Inc. | Indonesia | Design (Rectangle) | IDM000078405 |
| Freescale Semiconductor, Inc. | Indonesia | Design (Rectangle) | IDM000078406 |
| Freescale Semiconductor, Inc. | Indonesia | ALTIVEC (Stylized) | IDM000369074 |
| Freescale Semiconductor, Inc. | Iran | FREESCALE | 119031 |
| Freescale Semiconductor, Inc. | Ireland | M-CORE | 207352 |
| Freescale Semiconductor, Inc. | Israel | DIGITAL DNA | 115366 |
| Freescale Semiconductor, Inc. | Israel | ALTIVEC (Stylized) | 159785 |
| Freescale Semiconductor, Inc. | Israel | FREESCALE | 172608 |
| Freescale Semiconductor, Inc. | Israel | FREESCALE | 172609 |
| Freescale Semiconductor, Inc. | Israel | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 173597 |
| Freescale Semiconductor, Inc. | Israel | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 173598 |
| Freescale Semiconductor, Inc. | Israel | Design (Rectangle) | 173599 |
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| Freescale Semiconductor, Inc. | Israel | Design (Rectangle) | 173600 |
|-------------------------------|--------|--------------------------------|---------|
| Freescale Semiconductor, Inc. | Israel | POWERQUICC | 182267 |
| Freescale Semiconductor, Inc. | Israel | STARCORE | 202000 |
| Freescale Semiconductor, Inc. | Israel | STARCORE | 202001 |
| Freescale Semiconductor, Inc. | Israel | FREESCALE & Design (Rectangle) | 1132971 |
| Freescale Semiconductor, Inc. | Italy | M.CORE | 1298343 |
| Freescale Semiconductor, Inc. | Japan | FREESCALE & Design (Rectangle) | 1132971 |
| Freescale Semiconductor, Inc. | Japan | DNA | 2063225 |
| Freescale Semiconductor, Inc. | Japan | IMB | 2627743 |
| Freescale Semiconductor, Inc. | Japan | INTER MODULE BUS | 2636299 |
| Freescale Semiconductor, Inc. | Japan | AMCU | 2655757 |
| Freescale Semiconductor, Inc. | Japan | SMARTMOS | 2673554 |
| Freescale Semiconductor, Inc. | Japan | SMARTPOWER | 2695856 |
| Freescale Semiconductor, Inc. | Japan | X-DUCER | 2720706 |
| Freescale Semiconductor, Inc. | Japan | KWI | 3188870 |
| Freescale Semiconductor, Inc. | Japan | LDMOS | 3188871 |
| Freescale Semiconductor, Inc. | Japan | MCCI | 3188873 |
| Freescale Semiconductor, Inc. | Japan | POR | 3188875 |
| Freescale Semiconductor, Inc. | Japan | PRU | 3188876 |
| Freescale Semiconductor, Inc. | Japan | QSM | 3188877 |
| Freescale Semiconductor, Inc. | Japan | QSPI | 3188878 |
| Freescale Semiconductor, Inc. | Japan | SCIM | 3188881 |
| Freescale Semiconductor, Inc. | Japan | XIRQ | 3188882 |
| Freescale Semiconductor, Inc. | Japan | LVI | 3195035 |
| Freescale Semiconductor, Inc. | Japan | STARCORE | 3204234 |
| Freescale Semiconductor, Inc. | Japan | PULSE ACCUMLATOR | 3205797 |
| Freescale Semiconductor, Inc. | Japan | STARCORE | 3225432 |
| Freescale Semiconductor, Inc. | Japan | DRAGONBALL | 3243189 |
| Freescale Semiconductor, Inc. | Japan | QADC | 3274397 |
| Freescale Semiconductor, Inc. | Japan | RMCU | 3279460 |
| Freescale Semiconductor, Inc. | Japan | RWU | 3279461 |
| Freescale Semiconductor, Inc. | Japan | CONFIG REGISTER (in Japanese) | 3296081 |
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| Freescale Semiconductor, Inc. | Japan | COLDFIRE | 3300650 |
|-------------------------------|-------|---|---------|
| Freescale Semiconductor, Inc. | Japan | MTPROM | 3324801 |
| Freescale Semiconductor, Inc. | Japan | PEPROM | 3324802 |
| Freescale Semiconductor, Inc. | Japan | BALL GRID ARRAY | 3370248 |
| Freescale Semiconductor, Inc. | Japan | XDUCER | 4000958 |
| Freescale Semiconductor, Inc. | Japan | SENSEON | 4100135 |
| Freescale Semiconductor, Inc. | Japan | MC68000 | 4109581 |
| Freescale Semiconductor, Inc. | Japan | ALTIVEC (Stylized) | 4292776 |
| Freescale Semiconductor, Inc. | Japan | ALTIVEC/TECHNOLOGY design | 4320455 |
| Freescale Semiconductor, Inc. | Japan | POWERQUICC | 4340764 |
| Freescale Semiconductor, Inc. | Japan | DIGITALPOWER | 4359031 |
| Freescale Semiconductor, Inc. | Japan | CODEOPTIX | 4422658 |
| Freescale Semiconductor, Inc. | Japan | FLASH MCU | 4537259 |
| Freescale Semiconductor, Inc. | Japan | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 4895180 |
| Freescale Semiconductor, Inc. | Japan | Design (Rectangle) | 4896646 |
| Freescale Semiconductor, Inc. | Japan | FREESCALE | 4911094 |
| Freescale Semiconductor, Inc. | Japan | QORIQ | 5190666 |
| Freescale Semiconductor, Inc. | Japan | Design (Windmill) | 5221707 |
| Freescale Semiconductor, Inc. | Japan | CODETEST | 5241972 |
| Freescale Semiconductor, Inc. | Japan | CODEWARRIOR | 5286675 |
| Freescale Semiconductor, Inc. | Japan | VORTIQA | 5305977 |
| Freescale Semiconductor, Inc. | Japan | PROCESSOR EXPERT | 5320081 |
| Freescale Semiconductor, Inc. | Japan | KINETIS | 5365872 |
| Freescale Semiconductor, Inc. | Japan | COLDFIRE+ | 5376771 |
| Freescale Semiconductor, Inc. | Japan | FSL | 5388156 |
| Freescale Semiconductor, Inc. | Japan | QORIVVA | 5406174 |
| Freescale Semiconductor, Inc. | Japan | READY PLAY | 5448079 |
| Freescale Semiconductor, Inc. | Japan | AIRFAST | 5448082 |
| Freescale Semiconductor, Inc. | Japan | XTRINSIC | 5449608 |
| Freescale Semiconductor, Inc. | Japan | SAFEASSURE | 5521260 |
| Freescale Semiconductor, Inc. | Japan | SAFE ASSURE BY FREESCALE & Design (Horizontal Diamonds) | 5521261 |

| Freescale Semiconductor, Inc. | Japan | VYBRID | 5530675 |
|-------------------------------|--------------------|--|---------------|
| Freescale Semiconductor, Inc. | Japan | QORIQ QONVERGE (in Katakana) | 5535724 |
| Freescale Semiconductor, Inc. | Japan | MAGNIV | 5560930 |
| Freescale Semiconductor, Inc. | Japan | LAYERSCAPE | 5577869 |
| Freescale Semiconductor, Inc. | Jordan | FREESCALE | 76087 |
| Freescale Semiconductor, Inc. | Jordan | FREESCALE | 76088 |
| Freescale Semiconductor, Inc. | Jordan | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 77343 |
| Freescale Semiconductor, Inc. | Jordan | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 77344 |
| Freescale Semiconductor, Inc. | Jordan | Design (Rectangle) | 77345 |
| Freescale Semiconductor, Inc. | Jordan | Design (Rectangle) | 77346 |
| Freescale Semiconductor, Inc. | Kazakhstan | FREESCALE | 19720 |
| Freescale Semiconductor, Inc. | Kenya | FREESCALE | 56160 |
| Freescale Semiconductor, Inc. | Kosovo | Design (Rectangle) | 3461 |
| Freescale Semiconductor, Inc. | Kosovo | FREESCALE | 3462 |
| Freescale Semiconductor, Inc. | Kosovo | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 3463 |
| Freescale Semiconductor, Inc. | Kuwait | FREESCALE | 58110 |
| Freescale Semiconductor, Inc. | Kuwait | FREESCALE | 58508 |
| Freescale Semiconductor, Inc. | Kyrgyz Republic | FREESCALE | 7429 |
| Freescale Semiconductor, Inc. | Laos | FREESCALE | 10886 |
| Freescale Semiconductor, Inc. | Laos | FREESCALE | 10887 |
| Freescale Semiconductor, Inc. | Latvia | Design (Rectangle) | M 55592 |
| Freescale Semiconductor, Inc. | Latvia | FREESCALE SEMICONDUCTOR & Design (Rectangle) | M 55593 |
| Freescale Semiconductor, Inc. | Latvia | FREESCALE | M55668 |
| Freescale Semiconductor, Inc. | Lebanon | FREESCALE | 98392 |
| Freescale Semiconductor, Inc. | Lebanon | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 98966 |
| Freescale Semiconductor, Inc. | Lebanon | Design (Rectangle) | 98967 |
| Freescale Semiconductor, Inc. | Lesotho | FREESCALE | LS/M/04/00192 |
| Freescale Semiconductor, Inc. | Liechtenstein | FREESCALE | 13320 |
| Freescale Semiconductor, Inc. | Lithuania | FREESCALE | 52464 |
| Freescale Semiconductor, Inc. | Lithuania | Design (Rectangle) | 52470 |
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| Freescale Semiconductor, Inc. | Lithuania | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 52471 |
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| Freescale Semiconductor, Inc. | Macao | FREESCALE | N/014129 |
| Freescale Semiconductor, Inc. | Macao | FREESCALE | N/014130 |
| Freescale Semiconductor, Inc. | Macedonia (F.Y.R.O.M) | FREESCALE | 14057 |
| Freescale Semiconductor, Inc. | Madrid Protocol (TM) | FREESCALE & Design (Rectangle) | 1132971 |
| Freescale Semiconductor, Inc. | Malawi | FREESCALE | 298/2004 |
| Freescale Semiconductor, Inc. | Malaysia | ALTIVEC (Stylized) | 02013175 |
| Freescale Semiconductor, Inc. | Malaysia | FREESCALE SEMICONDUCTOR (Traditional Chinese Characters) | 04005144 |
| Freescale Semiconductor, Inc. | Malaysia | FREESCALE | 04007939 |
| Freescale Semiconductor, Inc. | Malaysia | FREESCALE | 04007940 |
| Freescale Semiconductor, Inc. | Malaysia | Design (Rectangle) | 04011153 |
| Freescale Semiconductor, Inc. | Malaysia | Design (Rectangle) | 04011154 |
| Freescale Semiconductor, Inc. | Malaysia | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 04011155 |
| Freescale Semiconductor, Inc. | Malaysia | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 04011156 |
| Freescale Semiconductor, Inc. | Malaysia | FREESCALE & Design (Rectangle) | 2012001456 |
| Freescale Semiconductor, Inc. | Malaysia | FREESCALE & Design (Rectangle) | 2012001457 |
| Freescale Semiconductor, Inc. | Malaysia | FREESCALE & Design (Rectangle) | 2012001459 |
| Freescale Semiconductor, Inc. | Malaysia | FREESCALE SEMICONDUCTOR (Traditional Chinese Characters) | 2004/05145 |
| Freescale Semiconductor, Inc. | Malaysia | FREESCALE (Traditional Chinese Characters) | 2004/05146 |
| Freescale Semiconductor, Inc. | Malaysia | FREESCALE (Traditional Chinese Characters) | 2004/05147 |
| Freescale Semiconductor, Inc. | Malta | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 42240 |
| Freescale Semiconductor, Inc. | Malta | FREESCALE | 42283 |
| Freescale Semiconductor, Inc. | Malta | FREESCALE | 42284 |
| Freescale Semiconductor, Inc. | Malta | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 42441 |
| Freescale Semiconductor, Inc. | Malta | Design (Rectangle) | 42442 |
| Freescale Semiconductor, Inc. | Malta | Design (Rectangle) | 42443 |
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| Freescale Semiconductor, Inc. | Mexico | M-CORE | 577520 |
|-------------------------------|--------|--|---------|
| Freescale Semiconductor, Inc. | Mexico | DIGITAL DNA & Design (Small Asterisk) | 592139 |
| Freescale Semiconductor, Inc. | Mexico | DIGITAL DNA & Design (Large Asterisk) | 592140 |
| Freescale Semiconductor, Inc. | Mexico | Design (Asterisk) | 592141 |
| Freescale Semiconductor, Inc. | Mexico | Design (Asterisk) | 596254 |
| Freescale Semiconductor, Inc. | Mexico | DIGITAL DNA & Design (Small Asterisk) | 597740 |
| Freescale Semiconductor, Inc. | Mexico | ALTIVEC (Stylized) | 770388 |
| Freescale Semiconductor, Inc. | Mexico | SYMPHONY | 792878 |
| Freescale Semiconductor, Inc. | Mexico | FREESCALE | 854716 |
| Freescale Semiconductor, Inc. | Mexico | FREESCALE | 857007 |
| Freescale Semiconductor, Inc. | Mexico | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 879423 |
| Freescale Semiconductor, Inc. | Mexico | Design (Rectangle) | 879424 |
| Freescale Semiconductor, Inc. | Mexico | Design (Rectangle) | 886286 |
| Freescale Semiconductor, Inc. | Mexico | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 886287 |
| Freescale Semiconductor, Inc. | Mexico | QORIQ | 1065797 |
| Freescale Semiconductor, Inc. | Mexico | Design (Windmill) | 1076244 |
| Freescale Semiconductor, Inc. | Mexico | Design (Windmill) | 1087642 |
| Freescale Semiconductor, Inc. | Mexico | VORTIQA | 1129875 |
| Freescale Semiconductor, Inc. | Mexico | XTRINSIC | 1175926 |
| Freescale Semiconductor, Inc. | Mexico | QORIQ QONVERGE | 1256202 |
| Freescale Semiconductor, Inc. | Mexico | FREESCALE & Design (Rectangle) | 1295042 |
| Freescale Semiconductor, Inc. | Mexico | FREESCALE & Design (Rectangle) | 1295884 |
| Freescale Semiconductor, Inc. | Mexico | FREESCALE & Design (Rectangle) | 1295885 |
| Freescale Semiconductor, Inc. | Mexico | VYBRID | 1299449 |
| Freescale Semiconductor, Inc. | Mexico | LAYERSCAPE | 1320081 |
| Freescale Semiconductor, Inc. | Mexico | FREESCALE & Design (Rectangle) | 1344137 |
| Freescale Semiconductor, Inc. | Mexico | FREESCALE | 1356174 |
| Freescale Semiconductor, Inc. | Mexico | FREESCALE | 1356175 |
| Freescale Semiconductor, Inc. | Mexico | FREESCALE | 1356176 |
| Freescale Semiconductor, Inc. | Mexico | FREESCALE | 1360202 |

| Freescale Semiconductor, Inc. | Mexico | FREESCALE TOWER SYSTEM | 1363993 |
|-------------------------------|-------------|--|-----------|
| Freescale Semiconductor, Inc. | Moldova | FREESCALE | 12595 |
| Freescale Semiconductor, Inc. | Monaco | FREESCALE | 04.24182 |
| Freescale Semiconductor, Inc. | Mongolia | FREESCALE | 4822 |
| Freescale Semiconductor, Inc. | Montenegro | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 01807PP |
| Freescale Semiconductor, Inc. | Montenegro | Design (Rectangle) | 01808PP |
| Freescale Semiconductor, Inc. | Montenegro | FREESCALE | 01982PP |
| Freescale Semiconductor, Inc. | Morocco | FREESCALE | 92529 |
| Freescale Semiconductor, Inc. | Myanmar | FREESCALE | 49712004 |
| Freescale Semiconductor, Inc. | Namibia | FREESCALE | 2004/0579 |
| Freescale Semiconductor, Inc. | Namibia | FREESCALE | 2004/0580 |
| Freescale Semiconductor, Inc. | New Zealand | DIGITAL DNA | 283478 |
| Freescale Semiconductor, Inc. | New Zealand | ALTIVEC (Stylized) | 666707 |
| Freescale Semiconductor, Inc. | New Zealand | FREESCALE | 713533 |
| Freescale Semiconductor, Inc. | New Zealand | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 715677 |
| Freescale Semiconductor, Inc. | New Zealand | Design (Rectangle) | 715678 |
| Freescale Semiconductor, Inc. | Nicaragua | FREESCALE | 81,398 LM |
| Freescale Semiconductor, Inc. | Nigeria | FREESCALE | 78195 |
| Freescale Semiconductor, Inc. | Norway | ALTIVEC (Stylized) | 219211 |
| Freescale Semiconductor, Inc. | Norway | FREESCALE | 227532 |
| Freescale Semiconductor, Inc. | Norway | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 228022 |
| Freescale Semiconductor, Inc. | Norway | Design (Rectangle) | 228388 |
| Freescale Semiconductor, Inc. | Norway | POWERQUICC | 232075 |
| Freescale Semiconductor, Inc. | Oman | FREESCALE | 33556 |
| Freescale Semiconductor, Inc. | Oman | FREESCALE | 33557 |
| Freescale Semiconductor, Inc. | Pakistan | FREESCALE | 192386 |
| Freescale Semiconductor, Inc. | Pakistan | Design (Rectangle) | 193126 |
| Freescale Semiconductor, Inc. | Pakistan | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 193127 |
| Freescale Semiconductor, Inc. | Pakistan | FREESCALE | 195470 |
| Freescale Semiconductor, Inc. | Pakistan | FREESCALE | 195471 |

| Freescale Semiconductor, Inc. | Pakistan | Design (Rectangle) | 195472 |
|-------------------------------|-------------|--|--------------|
| Freescale Semiconductor, Inc. | Pakistan | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 195473 |
| Freescale Semiconductor, Inc. | Panama | DIGITAL DNA | 111102 |
| Freescale Semiconductor, Inc. | Panama | DIGITAL DNA | 111103 |
| Freescale Semiconductor, Inc. | Panama | DIGITAL DNA | 111104 |
| Freescale Semiconductor, Inc. | Panama | DIGITAL DNA | 111105 |
| Freescale Semiconductor, Inc. | Panama | DIGITAL DNA | 111110 |
| Freescale Semiconductor, Inc. | Panama | DIGITAL DNA | 111111 |
| Freescale Semiconductor, Inc. | Panama | FREESCALE | 135,942 |
| Freescale Semiconductor, Inc. | Panama | FREESCALE | 135,946 |
| Freescale Semiconductor, Inc. | Paraguay | FREESCALE | 276167 |
| Freescale Semiconductor, Inc. | Paraguay | FREESCALE | 276168 |
| Freescale Semiconductor, Inc. | Paraguay | Design (Rectangle) | 277083 |
| Freescale Semiconductor, Inc. | Paraguay | Design (Rectangle) | 277084 |
| Freescale Semiconductor, Inc. | Paraguay | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 279465 |
| Freescale Semiconductor, Inc. | Paraguay | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 280706 |
| Freescale Semiconductor, Inc. | Peru | FREESCALE | 36645 |
| Freescale Semiconductor, Inc. | Peru | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 36808 |
| Freescale Semiconductor, Inc. | Peru | Design (Rectangle) | 37212 |
| Freescale Semiconductor, Inc. | Peru | M.CORE | 045235 |
| Freescale Semiconductor, Inc. | Peru | FREESCALE | 101354 |
| Freescale Semiconductor, Inc. | Peru | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 101845 |
| Freescale Semiconductor, Inc. | Peru | Design (Rectangle) | 103026 |
| Freescale Semiconductor, Inc. | Philippines | FREESCALE | 4-2004-00545 |
| Freescale Semiconductor, Inc. | Philippines | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 4-2004-00697 |
| Freescale Semiconductor, Inc. | Philippines | Design (Rectangle) | 4-2004-00697 |
| Freescale Semiconductor, Inc. | Poland | ALTIVEC (Stylized) | R-167374 |
| Freescale Semiconductor, Inc. | Poland | FREESCALE | R-186772 |
| Freescale Semiconductor, Inc. | Poland | Design (Rectangle) | R-193753 |
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| Freescale Semiconductor, Inc. | Poland | FREESCALE SEMICONDUCTOR & Design (Rectangle) | R-194414 |
|-------------------------------|-----------------------|--|-----------|
| Freescale Semiconductor, Inc. | Portugal | M.CORE | 328079 |
| Freescale Semiconductor, Inc. | Qatar | FREESCALE | 32796 |
| Freescale Semiconductor, Inc. | Qatar | FREESCALE | 32797 |
| Freescale Semiconductor, Inc. | Republic of Korea | FREESCALE (Traditional Chinese Characters) | 13073 |
| Freescale Semiconductor, Inc. | Republic of Korea | FREESCALE SEMICONDUCTOR (Traditional Chinese Characters) | 13074 |
| Freescale Semiconductor, Inc. | Republic of Korea | FREESCALE | 14052 |
| Freescale Semiconductor, Inc. | Republic of Korea | Design (Rectangle) | 14053 |
| Freescale Semiconductor, Inc. | Republic of Korea | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 15032 |
| Freescale Semiconductor, Inc. | Republic of Korea | STARCORE | 21916 |
| Freescale Semiconductor, Inc. | Republic of Korea | FREESCALE & Design (Rectangle) | 1132971 |
| Freescale Semiconductor, Inc. | Republic of Korea | ALTIVEC (Stylized) | 40-573480 |
| Freescale Semiconductor, Inc. | Republic of Korea | QORIQ | 40-801354 |
| Freescale Semiconductor, Inc. | Republic of Korea | Design (Windmill) | 40-803742 |
| Freescale Semiconductor, Inc. | Republic of Korea | VORTIQA | 40-838417 |
| Freescale Semiconductor, Inc. | Republic of Korea | KINETIS | 40-876849 |
| Freescale Semiconductor, Inc. | Republic of Korea | QORIVVA | 40-896799 |
| Freescale Semiconductor, Inc. | Republic of Korea | COLDFIRE | 40-913924 |
| Freescale Semiconductor, Inc. | Republic of Korea | XTRINSIC | 40-916565 |
| Freescale Semiconductor, Inc. | Republic of Korea | MAGNIV | 40-927159 |
| Freescale Semiconductor, Inc. | Republic of Korea | AIRFAST | 40-927168 |
| Freescale Semiconductor, Inc. | Republic of Korea | SAFEASSURE | 40-957874 |
| Freescale Semiconductor, Inc. | Republic of Korea | QORIQ QONVERGE | 40-967908 |
| Freescale Semiconductor, Inc. | Republic of Korea | VYBRID | 40-971942 |
| Freescale Semiconductor, Inc. | Romania | FREESCALE | 62106 |
| Freescale Semiconductor, Inc. | Romania | Design (Rectangle) | 62853 |
| Freescale Semiconductor, Inc. | Romania | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 64105 |
| Freescale Semiconductor, Inc. | Russian Federation | Design (Asterisk) | 194850 |
| Freescale Semiconductor, Inc. | Russian Federation | DIGITAL DNA & Design (Small Asterisk) | 204585 |

Federation

| Freescale Semiconductor, Inc. | Russian Federation | DIGITAL DNA & Design (Large Asterisk) | 226625 |
|-------------------------------|-----------------------|---|------------|
| Freescale Semiconductor, Inc. | Russian Federation | ALTIVEC (Stylized) | 256365 |
| Freescale Semiconductor, Inc. | Russian Federation | FREESCALE | 292049 |
| Freescale Semiconductor, Inc. | Russian Federation | Design (Rectangle) | 293558 |
| Freescale Semiconductor, Inc. | Russian Federation | FREESCALE & Design (Rectangle) | 293798 |
| Freescale Semiconductor, Inc. | Russian Federation | QORIVVA | 441841 |
| Freescale Semiconductor, Inc. | Saudi Arabia | FREESCALE | 836/58 |
| Freescale Semiconductor, Inc. | Saudi Arabia | FREESCALE | 836/59 |
| Freescale Semiconductor, Inc. | Saudi Arabia | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 849/23 |
| Freescale Semiconductor, Inc. | Saudi Arabia | Design (Rectangle) | 849/26 |
| Freescale Semiconductor, Inc. | Saudi Arabia | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 849/45 |
| Freescale Semiconductor, Inc. | Saudi Arabia | Design (Rectangle) | 849/46 |
| Freescale Semiconductor, Inc. | Serbia | FREESCALE | 50104 |
| Freescale Semiconductor, Inc. | Serbia | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 50352 |
| Freescale Semiconductor, Inc. | Serbia | Design (Rectangle) | 50353 |
| Freescale Semiconductor, Inc. | Singapore | FREESCALE & Design (Rectangle) | 1132971 |
| Freescale Semiconductor, Inc. | Singapore | ALTIVEC (Stylized) | T0215663J |
| Freescale Semiconductor, Inc. | Singapore | FREESCALE (Simplified Chinese Characters) | T04/05992F |
| Freescale Semiconductor, Inc. | Singapore | FREESCALE (Simplified Chinese Characters) | T04/05995J |
| Freescale Semiconductor, Inc. | Singapore | FREESCALE SEMICONDUCTOR (Simplified Chinese Characters) | T04/05996I |
| Freescale Semiconductor, Inc. | Singapore | FREESCALE SEMICONDUCTOR (Simplified Chinese Characters) | T04/05997G |
| Freescale Semiconductor, Inc. | Singapore | FREESCALE | T04/09608B |
| Freescale Semiconductor, Inc. | Singapore | FREESCALE | T04/09610D |
| Freescale Semiconductor, Inc. | Singapore | FREESCALE SEMICONDUCTOR & Design (Rectangle) | T04/12366G |
| Freescale Semiconductor, Inc. | Singapore | Design (Rectangle) | T04/12372A |
| Freescale Semiconductor, Inc. | Singapore | Design (Rectangle) | T04/12375F |

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| Freescale Semiconductor, Inc. | Singapore | FREESCALE SEMICONDUCTOR & Design (Rectangle) | T0412365I |
| Freescale Semiconductor, Inc. | Singapore | VYBRID | T1201662I |
| Freescale Semiconductor, Inc. | Singapore | DIGITAL DNA | T97/12954G |
| Freescale Semiconductor, Inc. | Singapore | DIGITAL DNA | T9712953I |
| Freescale Semiconductor, Inc. | Singapore | DIGITAL DNA | T9712955E |
| Freescale Semiconductor, Inc. | Singapore | DIGITAL DNA & Design (Small Asterisk) | T9805963A |
| Freescale Semiconductor, Inc. | Slovakia | FREESCALE | 211019 |
| Freescale Semiconductor, Inc. | Slovakia | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 211912 |
| Freescale Semiconductor, Inc. | Slovakia | Design (Rectangle) | 211913 |
| Freescale Semiconductor, Inc. | Slovenia | FREESCALE | 200471102 |
| Freescale Semiconductor, Inc. | Slovenia | Design (Rectangle) | 200471565 |
| Freescale Semiconductor, Inc. | Slovenia | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 200471566 |
| Freescale Semiconductor, Inc. | South Africa | ALTIVEC (Stylized) | 2002/16159 |
| Freescale Semiconductor, Inc. | South Africa | FREESCALE | 2004/09265 |
| Freescale Semiconductor, Inc. | South Africa | FREESCALE | 2004/09266 |
| Freescale Semiconductor, Inc. | South Africa | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 2004/14982 |
| Freescale Semiconductor, Inc. | South Africa | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 2004/14983 |
| Freescale Semiconductor, Inc. | South Africa | Design (Rectangle) | 2004/14984 |
| Freescale Semiconductor, Inc. | South Africa | Design (Rectangle) | 2004/14985 |
| Freescale Semiconductor, Inc. | Swaziland | FREESCALE | 211/2004 |
| Freescale Semiconductor, Inc. | Sweden | STARCORE | 259139 |
| Freescale Semiconductor, Inc. | Sweden | M.CORE | 332279 |
| Freescale Semiconductor, Inc. | Switzerland | M.CORE | 453341 |
| Freescale Semiconductor, Inc. | Switzerland | ALTIVEC (Stylized) | 505296 |
| Freescale Semiconductor, Inc. | Switzerland | FREESCALE | 527425 |
| Freescale Semiconductor, Inc. | Switzerland | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 528081 |
| Freescale Semiconductor, Inc. | Switzerland | Design (Rectangle) | 528082 |
| Freescale Semiconductor, Inc. | Switzerland | FREESCALE & Design (Rectangle) | 1132971 |

| Freescale Semiconductor, Inc. | Taiwan | STARCORE | 71252 |
|-------------------------------|------------|--|---------|
| Freescale Semiconductor, Inc. | Taiwan | M.CORE | 871469 |
| Freescale Semiconductor, Inc. | Taiwan | DIGITAL DNA | 879327 |
| Freescale Semiconductor, Inc. | Taiwan | DIGITAL DNA | 879428 |
| Freescale Semiconductor, Inc. | Taiwan | DIGITAL DNA | 881708 |
| Freescale Semiconductor, Inc. | Taiwan | DIGITAL DNA & Design (Small Asterisk) | 885267 |
| Freescale Semiconductor, Inc. | Taiwan | DIGITAL DNA (Shu Zi Ji Yin & Asterisk) in Chinese Char & Dev | 913950 |
| Freescale Semiconductor, Inc. | Taiwan | DIGITAL DNA (Shu Zi Ji Yin & Asterisk) in Chinese Char & Dev | 913951 |
| Freescale Semiconductor, Inc. | Taiwan | STARCORE | 989898 |
| Freescale Semiconductor, Inc. | Taiwan | ALTIVEC (Stylized) | 1053638 |
| Freescale Semiconductor, Inc. | Taiwan | FREESCALE SEMICONDUCTOR (Traditional Chinese Characters) | 1135435 |
| Freescale Semiconductor, Inc. | Taiwan | FREESCALE (Traditional Chinese Characters) | 1135436 |
| Freescale Semiconductor, Inc. | Taiwan | FREESCALE SEMICONDUCTOR (Traditional Chinese Characters) | 1160850 |
| Freescale Semiconductor, Inc. | Taiwan | FREESCALE (Traditional Chinese Characters) | 1160851 |
| Freescale Semiconductor, Inc. | Taiwan | FREESCALE | 1169882 |
| Freescale Semiconductor, Inc. | Taiwan | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 1176653 |
| Freescale Semiconductor, Inc. | Taiwan | Design (Rectangle) | 1212928 |
| Freescale Semiconductor, Inc. | Taiwan | VORTIQA | 1404982 |
| Freescale Semiconductor, Inc. | Taiwan | XTRINSIC | 1441357 |
| Freescale Semiconductor, Inc. | Taiwan | COLDFIRE | 1476377 |
| Freescale Semiconductor, Inc. | Taiwan | KINETIS | 1494991 |
| Freescale Semiconductor, Inc. | Taiwan | VYBRID | 1538751 |
| Freescale Semiconductor, Inc. | Tajikistan | FREESCALE | TJ 6337 |
| Freescale Semiconductor, Inc. | Thailand | FREESCALE | SM28253 |
| Freescale Semiconductor, Inc. | Thailand | Design (Rectangle) | SM28266 |
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| Freescale Semiconductor, Inc. | Thailand | FREESCALE SEMICONDUCTOR & Design (Rectangle) | SM32350 |
|-------------------------------|-----------------------------|--|-------------|
| Freescale Semiconductor, Inc. | Thailand | ALTIVEC (Stylized) | TM193043 |
| Freescale Semiconductor, Inc. | Thailand | FREESCALE | TM221898 |
| Freescale Semiconductor, Inc. | Thailand | Design (Rectangle) | TM228589 |
| Freescale Semiconductor, Inc. | Thailand | FREESCALE SEMICONDUCTOR & Design (Rectangle) | TM282244 |
| Freescale Semiconductor, Inc. | Tunisia | FREESCALE | EE04.1326 |
| Freescale Semiconductor, Inc. | Turkey | ALTIVEC (Stylized) | 2002 028132 |
| Freescale Semiconductor, Inc. | Turkey | FREESCALE | 2004 018270 |
| Freescale Semiconductor, Inc. | Turkey | Design (Rectangle) | 2004 023407 |
| Freescale Semiconductor, Inc. | Turkey | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 2004 23406 |
| Freescale Semiconductor, Inc. | Turkmenistan | FREESCALE | 8824 |
| Freescale Semiconductor, Inc. | Uganda | FREESCALE | 26796 |
| Freescale Semiconductor, Inc. | Ukraine | FREESCALE | 60164 |
| Freescale Semiconductor, Inc. | Ukraine | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 75211 |
| Freescale Semiconductor, Inc. | Ukraine | Design (Rectangle) | 75212 |
| Freescale Semiconductor, Inc. | United Arab Emirates | Design (Rectangle) | 52345 |
| Freescale Semiconductor, Inc. | United Arab Emirates | Design (Rectangle) | 52346 |
| Freescale Semiconductor, Inc. | United Arab Emirates | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 52347 |
| Freescale Semiconductor, Inc. | United Arab Emirates | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 52348 |
| Freescale Semiconductor, Inc. | United Arab Emirates | FREESCALE | 53308 |
| Freescale Semiconductor, Inc. | United Arab Emirates | FREESCALE | 53309 |
| Freescale Semiconductor, Inc. | United Kingdom | SYMPHONY | 1504688 |
| Freescale Semiconductor, Inc. | United Kingdom | STARCORE | 1545327 |
| Freescale Semiconductor, Inc. | United Kingdom | M-CORE (Series) | 2157478 |
| Freescale Semiconductor, Inc. | United Kingdom | M CORE & Design | 2159127 |
| Freescale Semiconductor, Inc. | United Kingdom | FREESCALE | 2366159 |
| Freescale Semiconductor, Inc. | Uruguay | FREESCALE | 355558 |
| Freescale Semiconductor, Inc. | Uzbekistan | FREESCALE | MGU13329 |
| Freescale Semiconductor, Inc. | Venezuela | DIGITAL DNA | P-208623 |
| Freescale Semiconductor, Inc. | Venezuela | DIGITAL DNA | P-208624 |
| Freescale Semiconductor, Inc. | Venezuela | Design (Asterisk) | P-243,076 |
| Freescale Semiconductor, Inc. | Venezuela | FREESCALE | P-282921 |
| Freescale Semiconductor, Inc. | Venezuela | FREESCALE SEMICONDUCTOR & Design (Rectangle) | P292042 |
| Freescale Semiconductor, Inc. | Venezuela | Design (Rectangle) | P-292706 |
| Freescale Semiconductor, Inc. | Venezuela | LATINCHIP | S-014054 |
| Freescale Semiconductor, Inc. | Venezuela | FREESCALE | S-029713 |
| Freescale Semiconductor, Inc. | Venezuela | Design (Rectangle) | S-031404 |
| Freescale Semiconductor, Inc. | Venezuela | FREESCALE SEMICONDUCTOR & Design (Rectangle) | S-031405 |
| Freescale Semiconductor, Inc. | Vietnam | FREESCALE SEMICONDUCTOR & Design (Rectangle) | 68126 |
| Freescale Semiconductor, Inc. | Vietnam | Design (Rectangle) | 68127 |
| Freescale Semiconductor, Inc. | Vietnam | FREESCALE | 68129 |
| Freescale Semiconductor, Inc. | Virgin Islands (British) | FREESCALE | 2263 |
| Freescale Semiconductor, Inc. | Zambia | FREESCALE | 321/2004 |
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$Free scale\ Semiconductor,\ Inc.-Trademark\ Applications;\ For eign$

| <u>Owner</u> | Country | Title | Application # |
|-------------------------------|---------|---|---------------|
| Freescale Semiconductor, Inc. | Brazil | DIGITAL DNA (see surviving record FRES:048-BR1) | 820422193 |
| Freescale Semiconductor, Inc. | Brazil | LATINCHIP | 821427245 |
| Freescale Semiconductor, Inc. | Brazil | QORIVVA | 830835440 |
| Freescale Semiconductor, Inc. | Brazil | COLDFIRE | 831000945 |
| Freescale Semiconductor, Inc. | Brazil | MAGNIV | 831079630 |
| Freescale Semiconductor, Inc. | Brazil | QORIQ QONVERGE | 831180838 |
| Freescale Semiconductor, Inc. | Brazil | SAFEASSURE | 831225904 |
| Freescale Semiconductor, Inc. | Brazil | FREESCALE & Design (Rectangle) | 840027338 |
| Freescale Semiconductor, Inc. | Brazil | FREESCALE & Design (Rectangle) | 840027354 |
| Freescale Semiconductor, Inc. | Brazil | FREESCALE & Design (Rectangle) | 840027370 |
| Freescale Semiconductor, Inc. | Brazil | FREESCALE & Design (Rectangle) | 840027397 |
| Freescale Semiconductor, Inc. | Brazil | VYBRID | 840034130 |
| Freescale Semiconductor, Inc. | Brazil | LAYERSCAPE | 840165056 |
| Freescale Semiconductor, Inc. | Brazil | FREESCALE TOWER SYSTEM | 840353200 |
| Freescale Semiconductor, Inc. | Brazil | FREESCALE | 840374852 |

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| 840374887 |
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| cal Diamonds) 840520670 |
| zontal Diamonds) 840520700 |
| 1,454,133 |
| 1,485,966 |
| 1,537,965 |
| 1,561,995 |
| 1,563,478 |
| 1,582,342 |
| 1,605,748 |
| 1,605,749 |
| 8280506 |
| 8306452 |
| 9965716 |
| 11087464 |
| 11988475 |
| 9800063304 |
| 9800063305 |
| zontal Diamonds) Not yet available |
| cal Diamonds) Not yet available |
| etangle) 003811874 |
| 010634401 |
| zontal Diamonds) 011803962 |
| |

| Freescale Semiconductor, Inc. | European Community | SAFE ASSURE BY FREESCALE & Design (Vertical Diamonds) | 011803996 |
|-------------------------------|----------------------------|---|-----------------|
| Freescale Semiconductor, Inc. | Guatemala | DIGITAL DNA | M98932000 |
| Freescale Semiconductor, Inc. | Hong Kong | FREESCALE | 302472002 |
| Freescale Semiconductor, Inc. | India | CODEWARRIOR | 1645599 |
| Freescale Semiconductor, Inc. | India | PROCESSOR EXPERT | 1914573 |
| Freescale Semiconductor, Inc. | India | KINETIS | 1968756 |
| Freescale Semiconductor, Inc. | India | XTRINSIC | 1983292 |
| Freescale Semiconductor, Inc. | India | COLDFIRE | 2126622 |
| Freescale Semiconductor, Inc. | India | MAGNIV | 2163234 |
| Freescale Semiconductor, Inc. | India | QORIQ QONVERGE | 2185220 |
| Freescale Semiconductor, Inc. | India | SAFEASSURE | 2207401 |
| Freescale Semiconductor, Inc. | India | VYBRID | 2282777 |
| Freescale Semiconductor, Inc. | India | LAYERSCAPE | 2349771 |
| Freescale Semiconductor, Inc. | India | FREESCALE TOWER SYSTEM | 2437754 |
| Freescale Semiconductor, Inc. | India | SAFE ASSURE BY FREESCALE & Design (Horizontal Diamonds) | 2551292 |
| Freescale Semiconductor, Inc. | India | SAFE ASSURE BY FREESCALE & Design (Vertical Diamonds) | 2551293 |
| Freescale Semiconductor, Inc. | Iraq | FREESCALE | 46180 |
| Freescale Semiconductor, Inc. | Japan | FREESCALE TOWER SYSTEM | 2012-97618 |
| Freescale Semiconductor, Inc. | Madrid Protocol (TM) | FREESCALE | Not yet availab |
| Freescale Semiconductor, Inc. | Malaysia | FREESCALE & Design (Rectangle) | 2012001458 |
| Freescale Semiconductor, Inc. | Malaysia | FREESCALE | 2012020996 |
| Freescale Semiconductor, Inc. | Malaysia | FREESCALE | 2012020997 |
| Freescale Semiconductor, Inc. | Malaysia | FREESCALE | 2012020998 |
| Freescale Semiconductor, Inc. | Malaysia | FREESCALE | 2012020999 |
| Freescale Semiconductor, Inc. | Malaysia | FREESCALE | 2012021000 |
| Freescale Semiconductor, Inc. | Mexico | FREESCALE | 1333791 |
| Freescale Semiconductor, Inc. | Republic of Korea | LAYERSCAPE | 40-2012-3883 |
| Freescale Semiconductor, Inc. | Republic of Korea | FREESCALE TOWER SYSTEM | 40-2012-75372 |
| Freescale Semiconductor, Inc. | Republic of Korea | SAFE ASSURE BY FREESCALE & Design (Horizontal Diamonds) | 40-2013-31830 |
| | | | |

| • | | | |
|-------------------------------|----------------------|---|---------------|
| Freescale Semiconductor, Inc. | Republic of Korea | SAFE ASSURE BY FREESCALE & Design (Vertical Diamonds) | 40-2013-31838 |
| Freescale Semiconductor, Inc. | Sri Lanka | FREESCALE | 119863 |
| Freescale Semiconductor, Inc. | Sri Lanka | FREESCALE | 119864 |
| Freescale Semiconductor, Inc. | Taiwan | FREESCALE & Design (Rectangle) | 101006048 |
| Freescale Semiconductor, Inc. | Taiwan | FREESCALE TOWER SYSTEM | 101068386 |
| Freescale Semiconductor, Inc. | Taiwan | FREESCALE | 101070040 |
| | | COURDING AC (T. 1. 1.) | |

FREESCALE SEMICONDUCTOR HOLDINGS 2011 OMNIBUS INCENTIVE PLAN FORM PERFORMANCE RESTRICTED SHARE UNIT AWARD AGREEMENT (Senior Management)

THIS AGREEMENT (the "**Agreement**"), is made effective as of the date indicated in the grant summary in the Freescale equity recordkeeping system (the "**Date of Grant**"), by and among Freescale Semiconductor, Ltd., a Bermuda exempted limited liability company (the "**Company**"), the recipient's employing subsidiary and the recipient of the grant (the "**Executive**"):

RECITALS:

WHEREAS, the Company has adopted the Freescale Semiconductor Holdings 2011 Omnibus Incentive Plan (the "**Plan**"), which Plan is incorporated herein by reference and made a part of this Agreement. Capitalized terms used but not otherwise defined herein shall have meanings ascribed to such terms in the Plan; and

WHEREAS, the Administrator has determined that it would be in the best interests of the Company and its shareholders to grant the Restricted Share Units provided for herein to the Executive pursuant to the Plan and the terms set forth herein.

NOW THEREFORE, in consideration of the mutual covenants hereinafter set forth, the parties agree as follows:

- 1. <u>Grant of Restricted Share Units</u>. The Company hereby grants to the Executive, on the terms and conditions hereinafter set forth, units evidencing a right to receive a target number of Common Shares (or a lesser or greater number of Common Shares, or no Common Shares whatsoever) as indicated in the grant summary in the Freescale equity recordkeeping system, based on the Company's achievement of the performance goals set forth on <u>Appendix A</u> hereto (the "**Performance Goals**"), which <u>Appendix A</u> is incorporated herein by reference and made a part hereof, all in accordance with the terms and conditions of this Agreement (the "**Restricted Share Units**" or "**Restricted Share Unit Award**"). Shares corresponding to the Restricted Share Units, if any, are to be delivered to the Executive only after the Performance Goals have been achieved and certified as described in <u>Section 3</u> and the Executive has become vested in the Restricted Share Units pursuant to <u>Section 4</u> or <u>Section 5</u> below.
- 2. <u>Performance Period</u>. For purposes of this Agreement, the term "**Performance Period**" shall refer to January 1, 20 through December 31, 20 , subject to <u>Section 4(c) below</u>.
 - 3. Performance Goals.
- (a) To the extent, if any, the applicable Performance Goals have been achieved for the Performance Period, and subject to compliance with the requirements of <u>Section 4</u>, the Executive will be entitled to receive from 0 to 1.5 (such number, the "**Share Delivery Factor**") Common Shares for each of the Restricted Share Units under this Agreement.

(b) The Compensation and Leadership Committee of the Company's Board (the "Committee") shall, as soon as practicable following the last day of the Performance Period, and in any event prior to January 31, 20 , certify (i) the extent to which the Performance Goals have been achieved, if at all, and (ii) the number of whole Common Shares, if any, which the Executive shall be entitled to receive with respect to each Restricted Share Unit granted under this Agreement. In the event the Share Delivery Factor equals zero, the Restricted Share Units granted under this Agreement shall be cancelled. Such certification shall be final, conclusive and binding on the Executive, and on all other persons, to the maximum extent permitted by law.

4. Restrictions and Vesting.

- (a) <u>Restrictions and Transferability</u>. The Restricted Share Unit Award may not be assigned, alienated, pledged, attached, sold or otherwise transferred or encumbered by the Executive otherwise than by will or by the laws of descent and distribution, and any such purported assignment, alienation, pledge, attachment, sale, transfer or encumbrance shall be void and unenforceable against the Company or any Affiliate; provided that the designation of a beneficiary shall not constitute an assignment, alienation, pledge, attachment, sale, transfer or encumbrance. No such permitted transfer of the Restricted Share Unit Award to heirs or legatees of the Executive shall be effective to bind the Company unless the Administrator shall have been furnished with written notice thereof and a copy of such evidence as the Administrator may deem necessary to establish the validity of the transfer and the acceptance by the transferees of the terms and conditions hereof.
- (b) <u>Vesting</u>. Subject to the Executive's continued employment with the Company, or except as otherwise provided herein, to the extent that the Performance Goals for the Performance Period have been achieved, the Restricted Share Units delivered under this Agreement, if any, shall vest on the date that the Committee certifies that the Performance Goals have been achieved in accordance with <u>Section 3(b)</u> above.

(c) Change in Control.

- (i) Notwithstanding anything to the contrary contained in the Plan or in this Agreement, in the event of a Change in Control that occurs before December 31, 20 , the Performance Period shall end on the date of the Change in Control, or another date established at the discretion of the Committee, and the Share Delivery Factor shall be calculated based on the Performance Period as adjusted by this Section 4(c).
- (ii) Notwithstanding any other provisions of the Plan or this Agreement to the contrary, in the event that the Executive's employment with the Company is terminated by the Company without Cause or by the Executive for Good Reason, in either case within twelve months following a Change in Control, after the application of Section 4(c)(i) above, all unvested Restricted Share Units shall become immediately vested. For purposes of this Agreement, "Cause" and "Good Reason" shall have the meanings set forth in the Executive's employment agreement, of if the Executive does not have an employment agreement in which these terms are defined, then Cause shall have the meaning set forth in the Plan and Good Reason shall have the meaning set forth below.

- (iii) If the Restricted Share Unit Award is not assumed or substituted in connection with a Change in Control, immediately upon the occurrence of the Change in Control, all unvested Restricted Share Units shall become immediately vested. For purposes of this Section 4(c)(iii), the Restricted Share Unit Award shall be considered assumed or substituted if, following the Change in Control, the Restricted Share Unit Award is of comparable value and remains subject to the same terms and conditions that were applicable to the Restricted Share Unit Award immediately prior to the Change in Control except that the Restricted Share Unit Award instead confers the right to receive common stock of the acquiring entity or in the case of an amalgamation, the amalgamated company or its parent. If the Executive does not have an employment agreement in which Good Reason is defined, "Good Reason" means, in the absence of the Executive's written consent, any of the following: (i) a material reduction by the Company in the Executive's base salary or target bonus unless the base salary or target bonus of all senior executives is reduced by a similar percentage or amount as part of company-wide cost reductions; (ii) a material reduction in the aggregate level of employee benefits made available to the Executive when compared to the benefits made available to the Executive at any time during the Executive's employment with the Company, unless the reduction is applicable to senior executives of the Company generally; (iii) a material diminution in the Executive's duties or responsibilities (other than as a result of the Executive's physical or mental incapacity which impairs his ability to materially perform his duties or responsibilities as confirmed by a doctor reasonably acceptable to the Executive or his representative and such diminution lasts only for so long as such doctor determines such incapacity impairs the Executive's ability to materially perform his duties or responsibilities). A lateral job change that does not materially diminish the Executive's duties or responsibilities and does not affect the Executive's reporting relationship will not constitute Good Reason; or (iv) the Company requiring the Executive's principal location of employment to be at any office or location more than 75 miles from the principal headquarters of the Company (other than any such change in location which is not materially adverse to the Executive, and other than to the extent agreed to or requested by the Executive) on the Date of Grant.
- (d) <u>Settlement of Restricted Share Units</u>. Shares shall be delivered (provided, that such delivery is otherwise in accordance with federal and state securities laws) with respect to the Restricted Share Units, to the extent then vested, as soon as practicable following the vesting date, but in no event later than the 60th day following the vesting date.
- (e) No Shareholder Rights. The Executive shall have no rights of a shareholder of the Company with respect to the Restricted Share Units, including, but not limited to, the rights to vote and receive ordinary dividends, until the settlement date of the Restricted Share Units. In the event that the Administrator approves an adjustment to the Restricted Share Unit Award pursuant to Section 5 of the Plan, then in such event, any and all new, substituted or additional securities to which Executive is entitled by reason of the Restricted Share Unit Award shall be immediately subject to the restrictions and the Vesting Period set forth in Sections 4(a) and (b) above with the same force and effect as the Restricted Share Unit Award subject to such restrictions immediately before such event.

5. Termination of Employment.

- (a) <u>General</u>. If the Executive's employment is terminated for any reason, other than death, Disability or after a Change in Control, the Restricted Share Unit Award shall, to the extent not then vested (after giving effect to the provisions of this Section 5), terminate upon such termination of employment.
- (b) <u>Death or Disability</u>. Upon the Executive's termination of employment due to the Executive's death or Disability, (i) prior to the first anniversary of the Date of Grant, the entire Restricted Share Unit Award shall be forfeited; and (ii) after the first anniversary of the Date of Grant, the Restricted Share Unit Award shall become vested for a number of Shares equal to the number of Shares subject to the Restricted Share Unit Award multiplied by a fraction, the numerator of which equals the number of days elapsed from the grant date and the denominator of which equals 1,096, with a deemed Share Delivery Factor of 1.0 for the Performance Period, subject to the maximum of the total number of Shares subject to the Restricted Share Unit Award.
- (c) <u>Forfeiture.</u> Notwithstanding anything herein to the contrary, if the Executive breaches any Restrictive Covenants applicable to the Executive (including, without limitation, the Restrictive Covenants set forth in <u>Exhibit A</u> hereto) at any time during the two year period following the Executive's termination of employment for any reason then the Executive shall immediately repay to the Company the Fair Market Value of Shares acquired pursuant to the Restricted Share Unit Award on any vesting date within the three year period prior to termination. The Company reserves the right to reduce or waive any amounts payable to the Company pursuant to this provision, in its sole discretion.
- 6. <u>Certain Covenants.</u> The Executive hereby agrees and covenants to perform all of the obligations set forth in <u>Exhibit A</u> hereto (which is incorporated by reference hereby) and acknowledges that the Executive's obligations set forth in <u>Exhibit A</u> constitute a material inducement for the Company's grant of the Restricted Share Unit Award to the Executive.
- 7. No Right to Continued Employment. The granting of the Restricted Share Unit Award evidenced hereby and this Agreement shall impose no obligation on the Company or any Affiliate to continue the employment of the Executive and shall not lessen or affect the Company's or any Affiliate's right to terminate the employment of such Executive. The granting of the Restricted Share Unit Award does not form part of and should in no way be construed as a term or condition of employment. At all times, the Restricted Share Unit Award granted hereunder is discretionary and does not imply that additional Restricted Share Unit Awards will be awarded in the future.
- 8. <u>Restricted Share Unit Award Not Wages</u>. The value of any Restricted Share Unit Award granted to Executive does not constitute and will not be included as wages for the purposes of calculating any benefit or bonus provided by the Company or the Executive's employing subsidiary.

- 9. Withholding. The Executive will be required to pay to the Company or any Affiliate and the Company shall have the right and is hereby authorized to withhold from any payment due or transfer made under the Restricted Share Unit Award or under the Plan or from any compensation or other amount owing to the Executive the amount (in cash, Shares, other securities or other property) of any applicable withholding taxes in respect of the Restricted Share Unit Award or any payment or transfer under or with respect to the Restricted Share Unit Award or the Plan and to take such other action as may be necessary in the opinion of the Administrator to satisfy all obligations for the payment of such withholding taxes.
- 10. <u>Securities Laws</u>. The issuance of any Shares hereunder shall be subject to the Executive making or entering into such written representations, warranties and agreements as the Administrator may reasonably request in order to comply with applicable securities laws and government regulations.
- 11. No Public Offering. The Restricted Share Units awarded under the Plan and this Agreement will not be publicly issued, placed, distributed or offered. The issuance of any Restricted Share Units hereunder does not constitute a public offering of securities.
- 12. <u>Consent to Transfer of Data</u>. By accepting the Restricted Share Unit Award, Executive consents to the transfer of personal data (including but not limited to the employee's name, address, birth date and hire date) and to the processing of this personal data by the Company and the provider of the Freescale equity recordkeeping system.
- 13. <u>Notices</u>. Any notice necessary under this Agreement shall be addressed to the Company in care of its Secretary at the principal executive office of the Company and to the Executive at the address appearing in the personnel records of the Company for the Executive or to either party at such other address as either party hereto may hereafter designate in writing to the other. Any such notice shall be deemed effective upon receipt thereof by the addressee.
- 14. <u>Governing Law</u>. This Agreement and all claims arising out of or based upon this Agreement or relating to the subject matter hereof shall be governed by and construed in accordance with the domestic substantive laws of the State of Delaware without giving effect to any choice or conflict of laws provision or rule that would cause the application of the domestic substantive laws of any other jurisdiction.
- 15. <u>Consent to Jurisdiction</u>. All actions arising out of or relating to this Agreement shall be heard and determined exclusively in any New York state or federal court sitting in the Borough of Manhattan in The City of New York. The parties hereto hereby (a) submit to the exclusive jurisdiction of any state or federal court sitting in the Borough of Manhattan of The City of New York for the purpose of any action arising out of or relating to this Agreement brought by any party hereto, and (b) irrevocably waive, and agree not to assert by way of motion, defense, or otherwise, in any such action, any claim that it is not subject personally to the jurisdiction of the above-named courts, that its property is exempt or immune of from attachment or execution, that the action is brought in an inconvenient forum, that the venue of the action is improper, or that this Agreement or the transactions contemplated hereby may not be enforced in or by any of the above-named courts.

- 16. The Restricted Share Unit Award Subject to Plan. By entering into this Agreement, the Executive agrees and acknowledges that the Executive has received and read a copy of the Plan. The Restricted Share Unit Award is subject to the Plan, as may be amended from time to time, and the terms and provisions of the Plan are hereby incorporated herein by reference.
- 17. <u>Acceptance</u>. This Agreement must be accepted by electronic signature of the Executive in the Freescale equity recordkeeping system or the Executive will have no right to the Restricted Share Unit Award provided for in this Agreement. By accepting this Agreement the Executive consents to the electronic delivery through the Freescale equity recordkeeping system of all documents related to this Restricted Share Unit Award.
- 18. <u>Clawback</u>. The Restricted Share Unit Award shall be subject to the Company's clawback policy, as it may be amended from time to time. The Company will amend its clawback policy, as needed, to the extent that the Securities and Exchange Commission adopts the final implementing rules regarding compensation clawbacks mandated by the Dodd-Frank Wall Street Reform and Consumer Protection Act of 2010.

Appendix A

Performance Goals

| | Share Delivery |
|------------------------------|----------------|
| Relative TSR Percentile Rank | Factor |
| < 25% | 0% |
| 25% | 0.25 |
| 50% | 1.00 |
| 75% | 1.50 |
| > 75% | 1.50 |

1) Definitions.

The following definitions shall be applicable to the Performance Goals and Agreement. Capitalized terms used but not otherwise defined herein shall have meanings ascribed to such terms in the Plan.

- (a) <u>"Relative Total Shareholder Return" or "Relative TSR"</u> means the Company's TSR compared to the Peer Companies TSR on a relative basis. The Company and the Peer Companies from highest to lowest according to their respective TSRs will determine Relative TSR. After this ranking, the percentile performance of the Company relative to the Peer Companies will be determined using the *Percentrank* formula in Microsoft Excel.
- (b) "Total Shareholder Return" or "TSR" means for the Company and each of the Peer Companies, the company's Total Shareholder Return, which will be calculated by dividing (i) the Closing Average Share Value by (ii) the Opening Average Share Value, and then subtracting one (1).
- (c) "Closing Average Share Value" means for the Company and each of the Peer Companies, the average, over the days in the Closing Average Period, of the closing price of its common stock or common shares, multiplied by the Accumulated Shares for each day during the Closing Average Period.

- (d) "Closing Average Period" means (i) in the absence of a Change in Control, the one month period ending on the last day of the Performance Period, or (ii) in the case of a Change in Control, the one month period ending five (5) days prior to Change in Control, or another date established at the discretion of the Committee.
- (e) "Opening Average Share Value" means for each of the Peer Companies and the Company, the average, over the days in the Opening Average Period, of the closing price of its common stock or common shares, multiplied by the Accumulated Shares for each day during the Opening Average Period.
 - (f) "Opening Average Period" means the one month period ending prior to the first day of the Performance Period.
- (g) "Accumulated Shares" means, for a given day, and for the Company or a given Peer Company, the sum of (i) one share of common stock of the applicable Company, plus (ii) a cumulative number of shares of common stock purchased with dividends declared on the common stock, assuming same day reinvestment of the dividends into shares of common stock at the closing price on the ex-dividend date, for ex-dividend dates during the Opening Average Period or for the period between December 31, 2012 and the last day of the Closing Averaging Period, as the case may be.
- (h) "Peer Companies" means the companies established by the Committee for purposes of calculating TSR, to include Advanced Micro Devices, Inc., Altera Corporation, Analog Devices, Inc., Applied Materials, Inc., Atmel Corporation, Avago Technologies, Broadcom Corporation, Infineon Technologies, Linear Technology Corporation, LSI Corporation, Marvel Technology Group, Maxim Integrated Products, Inc., Microchip Technology, Inc., Micron Technology, Inc., NXP Semiconductors, NVIDIA Corporation, On Semiconductor, Sandisk Corporation, ST Microelectronics, Texas Instruments and Xilinx, Inc. Any peer company shares traded on a foreign exchange will be converted to US dollars. In the event of a merger, acquisition or business combination transaction of a Peer Company with or by another Peer Company, the surviving entity shall remain a Peer Company. In the event of a merger of a Peer Company with an entity that is not a Peer Company, or the acquisition or business combination transaction by or with a Peer Company, or with an entity that is not a Peer Company, in each case where the Peer Company is the surviving entity and remains publicly traded, the surviving entity shall remain a Peer Company. In the event of a merger or acquisition or business combination transaction of a Peer Company by or with an entity that is not a Peer Company, a "going private" transaction involving a Peer Company or the liquidation of a Peer Company, where the Peer Company is not the surviving entity or is otherwise no longer publicly traded, the company shall no longer be a Peer Company.

Exhibit A – Restrictive Covenants

- (a) Confidential Information. The Executive recognizes and agrees that the Affiliated Group (defined below) has provided Confidential Information to the Executive and has an interest in protecting this information from disclosure. The Executive shall hold in a fiduciary capacity for the benefit of the Company and its Affiliates (collectively, the "Affiliated Group"), all secret or confidential information, knowledge or data relating to the Affiliated Group and its businesses (including, without limitation, any proprietary and not publicly available information concerning any processes, methods, trade secrets, research or secret data, costs, names of users or purchasers of their respective products or services, business methods, operating procedures or programs or methods of promotion and sale) that the Executive obtains during the Executive's employment that is not public knowledge (other than as a result of the Executive's violation of this Section (a)) ("Confidential Information"). The Executive shall not communicate, divulge or disseminate Confidential Information at any time during or after the Executive's employment, except with the prior written consent of the Company, or as otherwise required by law or legal process or as such disclosure or use may be required in the course of the Executive performing his duties and responsibilities with the Affiliated Group. Notwithstanding the foregoing provisions, if the Executive is required to disclose any such confidential or proprietary information pursuant to applicable law or a subpoena or court order, the Executive shall promptly notify the Company in writing of any such requirement prior to disclosure so that the Company or the appropriate member of the Affiliated Group may seek an appropriate protective order or other appropriate remedy or waive compliance with the provisions hereof. The Executive shall reasonably cooperate with the Company or the appropriate member of the Affiliated Group to obtain such a protective order or other remedy. If such order or other remedy is not obtained prior to the time the Executive is required to make the disclosure, or the Company waives compliance with the provisions hereof, the Executive shall disclose only that portion of the confidential or proprietary information which he is advised by counsel in writing (either his or the Company's) that he is legally required to so disclose. Upon his termination of employment for any reason, the Executive shall promptly return to the Company all records, files, memoranda, correspondence, notebooks, notes, reports, customer lists, drawings, plans, documents, and other documents and the like relating to the business of the Affiliated Group or containing any trade secrets relating to the Affiliated Group or that the Executive uses, prepares or comes into contact with during the course of the Executive's employment with the Affiliated Group, and all keys, credit cards and passes, and such materials shall remain the sole property of the Affiliated Group. The Executive agrees to execute any standard-form confidentiality agreements with the Company that the Company in the future generally enters into with similarly situated employees.
- (b) <u>Work Product and Inventions</u>. The Affiliated Group and/or its nominees or assigns shall own all right, title and interest in and to any and all inventions, ideas, trade secrets, technology, devices, discoveries, improvements, processes, developments, designs, know how, show-how, data, computer programs, algorithms, formulae, works of authorship, works modifications, trademarks, trade names, documentation, techniques, designs, methods, trade secrets, technical specifications, technical data, concepts, expressions, patents, patent rights, copyrights, moral rights, and all other intellectual property rights or other developments whatsoever (collectively, "**Developments**"), whether or not patentable, reduced to practice or

registerable under patent, copyright, trademark or other intellectual property law anywhere in the world, made, authored, discovered, reduced to practice, conceived, created, developed or otherwise obtained by the Executive (alone or jointly with others) during the Executive's employment with the Affiliated Group, and arising from or relating to such employment or the business of the Affiliated Group (whether during business hours or otherwise, and whether on the premises of using the facilities or materials of the Affiliated Group or otherwise). The Executive shall promptly and fully disclose to the Affiliated Group and to no one else all Developments, and hereby assigns to the Affiliated Group without further compensation all right, title and interest the Executive has or may have in any Developments, and all patents, copyrights, or other intellectual property rights relating thereto, and agrees that the Executive has not acquired and shall not acquire any rights during the course of his employment with the Affiliated Group or thereafter with respect to any Developments.

- (c) <u>Company Goodwill</u>. The Executive recognizes and acknowledges that the Affiliated Group has and continues to develop goodwill of substantial value through efforts of employees, including the Executive. This goodwill includes, but is not limited to, the identity and skill sets of its employees, its relationships with employees and customers, intangible value attributable to its products created by Executive and others, and the Affiliated Group's brand and reputation within the industry. Executive shall take no action to damage the goodwill of the Affiliated Group (including disparaging the Affiliated Group or any of their respective directors, officers, executives, employees, agents or other representatives) or use it for personal benefit or the benefit of competitors of the Affiliated Group.
- (d) Non-Recruitment of Affiliated Group Employees. The Executive acknowledges that employees are a significant part of the goodwill of the Affiliated Group, such as, without limitation, their relationships and contacts with customers and suppliers as well as the training and knowledge they receive from the Affiliated Group in the course of their employment. The Executive shall not, at any time during the Non-solicitation Restricted Period (as defined below), other than in the ordinary exercise of his duties while employed by the Affiliate Group, without the prior written consent of the Affiliated Group, directly or indirectly, solicit, recruit, or employ (whether as an employee, officer, agent, consultant or independent contractor) any person who is or was at any time during the previous 12 months, an employee, representative, officer or director of any member of the Affiliated Group. Further, during the Non-solicitation Restricted Period, the Executive shall not take any action that could reasonably be expected to have the effect of directly encouraging or inducing any person to cease their relationship with any member of the Affiliated Group for any reason. A general employment advertisement by an entity of which the Executive is a part will not constitute solicitation or recruitment. The "Non-solicitation Restricted Period" shall mean the period from the Date of Grant through the second anniversary of the Executive's termination of employment.
- (e) Non-Competition Solicitation of Business. The Executive recognizes and agrees that the Affiliated Group has provided Confidential Information to Executive and has an interest in protecting this information from disclosure. Executive further understands that the goodwill of the Affiliated Group is an interest worthy of protection. For the protection of these and other interests, during the Non-competition Restricted Period (as defined below), the Executive shall not, either directly or indirectly, compete with the business of the Affiliated Group by (i) becoming an officer, agent, employee, partner or director of any other corporation,

partnership or other entity, or otherwise render services to or assist or hold an interest (except as a less than 3-percent shareholder of a publicly traded corporation or as a less than 5-percent shareholder of a corporation that is not publicly traded) in any Competitive Business (as defined below), or (ii) soliciting, servicing, or accepting the business of (A) any active customer of any member of the Affiliated Group, or (B) any person or entity who is or was at any time during the previous twelve months a customer of any member of the Affiliated Group, provided that such business is competitive with any significant business of any member of the Affiliated Group. "Competitive Business" shall mean any person or entity (including any joint venture, partnership, firm, corporation, or limited liability company) that conducts a business that is competitive with any significant business of the Affiliated Group as of the date of termination (or any significant business that is being actively pursued as of the date of termination by the Affiliated Group). The Affiliated Group designs, manufactures, sells and licenses its products and technology worldwide. In addition, Competitive Businesses, as defined above, are not tied or limited to any specific geographic location. Accordingly, the scope of this Non-Competition provision is worldwide. The "Noncompetition Restricted Period" shall mean the period from the Date of Grant through the second anniversary of the date of termination of the Executive's employment.

- (f) Assistance. The Executive agrees that during and after his employment by the Affiliated Group, upon request by the Company, the Executive will assist the Affiliated Group in the defense of any claims, or potential claims that may be made or threatened to be made against any member of the Affiliated Group in any action, suit or proceeding, whether civil, criminal, administrative, investigative or otherwise (a "**Proceeding**"), and will assist the Affiliated Group in the prosecution of any claims that may be made by any member of the Affiliated Group in any Proceeding, to the extent that such claims may relate to the Executive's employment or the period of the Executive's employment by the Affiliated Group. The Executive agrees, unless precluded by law, to promptly inform the Company if the Executive also agrees, unless precluded by law, to promptly inform the Company if the Executive is asked to assist in any investigation (whether governmental or otherwise) of any member of the Affiliated Group (or their actions), regardless of whether a lawsuit has then been filed against any member of the Affiliated Group with respect to such investigation. The Company agrees to reimburse the Executive for all of the Executive's reasonable out-of-pocket expenses associated with such assistance, including travel expenses and any attorneys' fees and shall pay a reasonable per diem fee for the Executive's service. In addition, the Executive agrees to provide such services as are reasonably requested by the Company to assist any successor to the Executive in the transition of duties and responsibilities to such successor. Any services or assistance contemplated in this Section (f) shall be at mutually agreed to and convenient times.
- (g) Remedies. The Executive acknowledges and agrees that the terms of this Exhibit A: (i) are reasonable in geographic and temporal scope, (ii) are necessary to protect legitimate proprietary and business interests of the Affiliated Group in, inter alia, near permanent customer relationships and confidential information. The Executive further acknowledges and agrees that the Executive's breach of the provisions of this Exhibit A will cause the Affiliated Group irreparable harm, which cannot be adequately compensated by money damages. The Executive consents and agrees that the forfeiture provisions contained in the Agreement are

reasonable remedies in the event the Executive commits any such breach. If any of the provisions of this Exhibit A are determined to be wholly or partially unenforceable, the Executive hereby agrees that Exhibit A or any provision hereof may be reformed so that it is enforceable to the maximum extent permitted by law. If any of the provisions of this Exhibit A are determined to be wholly or partially unenforceable in any jurisdiction, such determination shall not be a bar to or in any way diminish the Affiliated Group's right to enforce any such covenant in any other jurisdiction.

FREESCALE SEMICONDUCTOR HOLDINGS 2011 OMNIBUS INCENTIVE PLAN FORM NONQUALIFIED STOCK OPTION AGREEMENT

(Senior Management)

THIS AGREEMENT (the "**Agreement**"), is made effective as of the date indicated in the grant summary in the Freescale equity recordkeeping system (the "**Date of Grant**"), by and among Freescale Semiconductor, Ltd., a Bermuda exempted limited liability company (the "**Company**"), the recipient's employing subsidiary and the recipient of the grant (the "**Executive**"):

RECITALS:

WHEREAS, the Company has adopted the Freescale Semiconductor Holdings 2011 Omnibus Incentive Plan (the "**Plan**"), which Plan is incorporated herein by reference and made a part of this Agreement. Capitalized terms used but not otherwise defined herein shall have meanings ascribed to such terms in the Plan; and

WHEREAS, the Administrator has determined that it would be in the best interests of the Company and its shareholders to grant the Option provided for herein to the Executive pursuant to the Plan and the terms set forth herein.

NOW THEREFORE, in consideration of the mutual covenants hereinafter set forth, the parties agree as follows:

1. <u>Grant of the Option</u>. The Company hereby grants to the Executive the right and option (the "**Option**") to purchase, on the terms and conditions hereinafter set forth, all or any part of an aggregate of Common Shares as indicated in the grant summary in the Freescale equity recordkeeping system (each a "**Share**" and collectively, the "**Shares**"). The purchase price of the Shares subject to the Option shall be at the price indicated in the grant summary in the Freescale equity recordkeeping system (the "**Exercise Price**"). The Option is intended to be a non-qualified stock option, and is not intended to be treated as an option that complies with Section 422 of the Code.

2. Vesting.

- (a) *General*. Except as otherwise provided in this Section 2, the Option shall vest and become exercisable with respect to twenty-five percent (25%) of the Shares initially covered by the Option on each of the first, second, third and fourth anniversaries of the Date of Grant, subject to the Executive's continued employment with the Company or an Affiliate on each such vesting date. At any time, the portion of the Option which has become vested as described above (or pursuant to Section 2(b) or 2(d)) is hereinafter referred to as the "Vested Portion."
- (b) <u>Death or Disability</u>. Notwithstanding any other provisions of the Plan or this Agreement to the contrary, in the event that the Executive's employment with the Company is terminated due to the Executive's death or Disability, the portion of the Option that would have become vested and exercisable on the next scheduled vesting date shall become vested and exercisable as of immediately prior to such termination.

(c) <u>Termination for Cause</u>. Notwithstanding any other provisions of the Plan or this Agreement to the contrary, the Option (including any Vested Portion thereof) shall terminate and be forfeited immediately upon the Company's notification to the Executive of the Executive's termination of employment by the Company for Cause.

(d) Change in Control.

- (i) Notwithstanding any other provisions of the Plan or this Agreement to the contrary, in the event that the Executive's employment with the Company is terminated by the Company without Cause or by the Executive for Good Reason, in either case within twelve months following a Change in Control, all unvested Options shall become immediately vested and exercisable. For purposes of this Agreement, "Cause" and "Good Reason" shall have the meanings set forth in the Executive's employment agreement, or if the Executive does not have an employment agreement in which these terms are defined, then Cause shall have the meaning set forth in the Plan and Good Reason shall have the meaning set forth below.
- (ii) If the Option Award is not assumed or substituted in connection with a Change in Control, immediately upon the occurrence of the Change in Control, all unvested Options shall become immediately vested and exercisable. For purposes of this Section 2(d)(ii), the Option Award shall be considered assumed or substituted if, following the Change in Control, the Option Award is of comparable value and remains subject to the same terms and conditions that were applicable to the Option Award immediately prior to the Change in Control except that the Option Award instead confers the right to purchase common stock of the acquiring entity or in the case of an amalgamation, the amalgamated company or its parent.
- (iii) If the Executive does not have an employment agreement with the Company in which Good Reason is defined, "Good Reason" means, in the absence of the Executive's written consent, any of the following: (i) a material reduction by the Company in the Executive's base salary or target bonus unless the base salary or target bonus of all senior executives is reduced by a similar percentage or amount as part of company-wide cost reductions; (ii) a material reduction in the aggregate level of employee benefits made available to the Executive when compared to the benefits made available to the Executive at any time during the Executive's employment with the Company, unless the reduction is applicable to senior executives of the Company generally; (iii) a material diminution in the Executive's duties or responsibilities (other than as a result of the Executive's physical or mental incapacity which impairs his ability to materially perform his duties or responsibilities as confirmed by a doctor reasonably acceptable to the Executive or his representative and such diminution lasts only for so long as such doctor determines such incapacity impairs the Executive's ability to materially perform his duties or responsibilities). A lateral job change that does not materially diminish the Executive's duties or responsibilities and does not affect the Executive's reporting relationship will not constitute Good Reason; or (iv) the Company requiring the Executive's principal location of employment to be at any office or location more than 75 miles from the principal headquarters of the Company (other than any such change in location which is not materially adverse to the Executive, and other than to the extent agreed to or requested by the Executive) on the Date of Grant.

- (e) <u>Forfeiture</u>. Notwithstanding anything herein to the contrary, if the Executive breaches any Restrictive Covenants applicable to the Executive (including, without limitation, the Restrictive Covenants set forth in Exhibit A hereto) at any time during the two year period following the Executive's termination of employment for any reason then (y) any Vested Portion then held by the Executive shall be automatically forfeited and (z) Executive shall immediately repay the Company any gain (defined as the difference between the Exercise Price and the Fair Market Value on the date of exercise) resulting from the exercise of an Option within the three year period prior to termination or after termination. The Company reserves the right to reduce or waive any amounts payable to the Company pursuant to this provision, in its sole discretion.
- 3. <u>Certain Covenants</u>. The Executive hereby agrees and covenants to perform all of the obligations set forth in Exhibit A hereto (which is incorporated by reference hereby) and acknowledges that the Executive's obligations set forth in Exhibit A constitute a material inducement for the Company's grant of the Option to the Executive.

4. Exercise of Option.

- (a) <u>Period of Exercise</u>. Subject to the provisions of the Plan and this Agreement, the Executive may exercise all or any part of the Vested Portion of the Option at any time prior to the earliest to occur of:
 - (i) the seventh (7th) anniversary of the Date of Grant;
 - (ii) twelve (12) months following the date of the Executive's termination of employment due to the Executive's Retirement, death, or Disability;
- (iii) ninety (90) days following the date of the Executive's termination of employment for any reason other than for Cause or due to the Executive's Retirement, death or Disability; and
 - (iv) the date that the Company notifies the Executive of the Executive's termination of employment for Cause.
 - (b) Method of Exercise.
- (i) Each election to exercise the Vested Portion shall be subject to the terms and conditions of the Plan and shall be made using the Freescale equity recordkeeping system or in writing, signed by the Executive or by his or her executor, administrator, or permitted transferee (subject to any restrictions provided under the Plan), made pursuant to and in accordance with the terms and conditions set forth in the Plan and received by the Company at its principal offices, accompanied by payment in full as provided in the Plan or in this Agreement.

- (ii) The Exercise Price may be paid (A) by the delivery of cash or check acceptable to the Administrator, (B) by any cashless exercise procedure approved by the Administrator (including the withholding of Shares otherwise issuable upon exercise), (C) in the form of unrestricted Shares already owned by the Executive which, (x) in the case of unrestricted Shares acquired upon exercise of an Option, have been owned by the Executive for more than six (6) months on the date of surrender, and (y) have a Fair Market Value on the date of surrender equal to the aggregate exercise price of the Shares as to which such Option shall be exercised, (D) any other method approved by the Administrator and permitted by applicable law or (E) any combination of the foregoing.
- (iii) In the event of the Executive's death, the Option shall remain exercisable by the Executive's executor or administrator, or the person or persons to whom the Executive's rights under this Agreement shall pass by will or by the laws of descent and distribution as the case may be, to the extent set forth in Section 4(a). Any heir or legatee of the Executive shall take rights herein granted subject to the terms and conditions hereof.
- 5. No Right to Continued Employment. The granting of the Option evidenced hereby and this Agreement shall impose no obligation on the Company or any Affiliate to continue the employment of the Executive and shall not lessen or affect the Company's or any Affiliate's right to terminate the employment of such Executive. The granting of the Option does not form part of and should in no way be construed as a term or condition of employment. At all times, the Option granted hereunder is discretionary and does not imply that additional Options will be awarded in the future.
- 6. Options Not Wages. The value of any Options granted to Executive does not constitute and will not be included as wages for the purposes of calculating any benefit or bonus provided by the Company or the Executive's employing subsidiary.
- 7. <u>Transferability</u>. Unless otherwise permitted in writing by the Administrator in its sole discretion, the Option granted hereunder may not be assigned, alienated, pledged, attached, sold or otherwise transferred or encumbered by the Executive other than by will or by the laws of descent and distribution, and any such purported assignment, alienation, pledge, attachment, sale, transfer or encumbrance shall be void and unenforceable against the Company or any Affiliate; provided, that the designation of a beneficiary shall not constitute an assignment, alienation, pledge, attachment, sale, transfer or encumbrance. During the Executive's lifetime, the Vested Portion is exercisable only by the Executive.
- 8. Withholding. The Executive will be required to pay to the Company or any Affiliate and the Company shall have the right and is hereby authorized to withhold from any payment due or transfer made under the Option or under the Plan or from any compensation or other amount owing to the Executive the amount (in cash, Shares, other securities or other property) of any applicable withholding taxes in respect of the Option, its exercise or any payment or transfer under or with respect to the Option or the Plan and to take such other action as may be necessary in the opinion of the Administrator to satisfy all obligations for the payment of such withholding taxes.

- 9. <u>Securities Laws</u>. The issuance of any Options hereunder shall be subject to the Executive making or entering into such written representations, warranties and agreements as the Administrator may reasonably request in order to comply with applicable securities laws and government regulations.
- 10. No Public Offering. The Options awarded under the Plan and this Agreement will not be publicly issued, placed, distributed or offered. The issuance of any Option hereunder does not constitute a public offering of securities.
- 11. <u>Consent to Transfer of Data</u>. By accepting the Option, Executive consents to the transfer of personal data (including but not limited to the employee's name, address, birth date and hire date) and to the processing of this personal data by the Company and the provider of the Freescale equity recordkeeping system.
- 12. <u>Notices</u>. Any notice necessary under this Agreement shall be addressed to the Company in care of its Secretary at the principal executive office of the Company and to the Executive at the address appearing in the personnel records of the Company for the Executive or to either party at such other address as either party hereto may hereafter designate in writing to the other. Any such notice shall be deemed effective upon receipt thereof by the addressee.
- 13. <u>Governing Law</u>. This Agreement and all claims arising out of or based upon this Agreement or relating to the subject matter hereof shall be governed by and construed in accordance with the domestic substantive laws of the State of Delaware without giving effect to any choice or conflict of laws provision or rule that would cause the application of the domestic substantive laws of any other jurisdiction.
- 14. <u>Consent to Jurisdiction</u>. All actions arising out of or relating to this Agreement shall be heard and determined exclusively in any New York state or federal court sitting in the Borough of Manhattan in The City of New York. The parties hereto hereby (a) submit to the exclusive jurisdiction of any state or federal court sitting in the Borough of Manhattan of The City of New York for the purpose of any action arising out of or relating to this Agreement brought by any party hereto, and (b) irrevocably waive, and agree not to assert by way of motion, defense, or otherwise, in any such action, any claim that it is not subject personally to the jurisdiction of the above-named courts, that its property is exempt or immune of from attachment or execution, that the action is brought in an inconvenient forum, that the venue of the action is improper, or that this Agreement or the transactions contemplated hereby may not be enforced in or by any of the above-named courts.
- 15. <u>Option Subject to Plan</u>. By entering into this Agreement, the Executive agrees and acknowledges that the Executive has received and read a copy of the Plan. The Option is subject to the Plan, as may be amended from time to time, and the terms and provisions of the Plan are hereby incorporated herein by reference.
- 16. <u>Acceptance</u>. This Agreement must be accepted by electronic signature of the Executive in the Freescale equity recordkeeping system or the Executive will have no right to the Option provided for in this Agreement. By accepting this Agreement the Executive consents to the electronic delivery through the Freescale equity recordkeeping system of all documents related to this Option.

17. <u>Clawback.</u> The Option Award shall be subject to the Company's clawback policy, as it may be amended from time to time. The Company will amend its clawback policy, as needed, to the extent that the Securities and Exchange Commission adopts the final implementing rules regarding compensation clawbacks mandated by the Dodd-Frank Wall Street Reform and Consumer Protection Act of 2010.

Exhibit A – Restrictive Covenants

(a) Confidential Information. The Executive recognizes and agrees that the Affiliated Group (defined below) has provided Confidential Information to the Executive and has an interest in protecting this information from disclosure. The Executive shall hold in a fiduciary capacity for the benefit of the Company and its Affiliates (collectively, the "Affiliated Group"), all secret or confidential information, knowledge or data relating to the Affiliated Group and its businesses (including, without limitation, any proprietary and not publicly available information concerning any processes, methods, trade secrets, research or secret data, costs, names of users or purchasers of their respective products or services, business methods, operating procedures or programs or methods of promotion and sale) that the Executive obtains during the Executive's employment that is not public knowledge (other than as a result of the Executive's violation of this Section (a)) ("Confidential Information"). The Executive shall not communicate, divulge or disseminate Confidential Information at any time during or after the Executive's employment, except with the prior written consent of the Company, or as otherwise required by law or legal process or as such disclosure or use may be required in the course of the Executive performing his duties and responsibilities with the Affiliated Group. Notwithstanding the foregoing provisions, if the Executive is required to disclose any such confidential or proprietary information pursuant to applicable law or a subpoena or court order, the Executive shall promptly notify the Company in writing of any such requirement prior to disclosure so that the Company or the appropriate member of the Affiliated Group may seek an appropriate protective order or other appropriate remedy or waive compliance with the provisions hereof. The Executive shall reasonably cooperate with the Company or the appropriate member of the Affiliated Group to obtain such a protective order or other remedy. If such order or other remedy is not obtained prior to the time the Executive is required to make the disclosure, or the Company waives compliance with the provisions hereof, the Executive shall disclose only that portion of the confidential or proprietary information which he is advised by counsel in writing (either his or the Company's) that he is legally required to so disclose. Upon his termination of employment for any reason, the Executive shall promptly return to the Company all records, files, memoranda, correspondence, notebooks, notes, reports, customer lists, drawings, plans, documents, and other documents and the like relating to the business of the Affiliated Group or containing any trade secrets relating to the Affiliated Group or that the Executive uses, prepares or comes into contact with during the course of the Executive's employment with the Affiliated Group, and all keys, credit cards and passes, and such materials shall remain the sole property of the Affiliated Group. The Executive agrees to execute any standard-form confidentiality agreements with the Company that the Company in the future generally enters into with similarly situated employees.

(b) <u>Work Product and Inventions</u>. The Affiliated Group and/or its nominees or assigns shall own all right, title and interest in and to any and all inventions, ideas, trade secrets, technology, devices, discoveries, improvements, processes, developments, designs, know how, show-how, data, computer programs, algorithms, formulae, works of authorship, works modifications, trademarks, trade names, documentation, techniques, designs, methods, trade secrets, technical specifications, technical data, concepts, expressions, patents, patent rights, copyrights, moral rights, and all other intellectual property rights or other developments whatsoever (collectively, "**Developments**"), whether or not patentable, reduced to practice or registerable under patent, copyright, trademark or other intellectual property law anywhere in the world, made, authored, discovered, reduced to practice, conceived, created, developed or otherwise obtained by the Executive (alone or jointly with others) during the Executive's employment with the Affiliated Group, and arising from or relating to such employment or the business of the Affiliated Group

(whether during business hours or otherwise, and whether on the premises of using the facilities or materials of the Affiliated Group or otherwise). The Executive shall promptly and fully disclose to the Affiliated Group and to no one else all Developments, and hereby assigns to the Affiliated Group without further compensation all right, title and interest the Executive has or may have in any Developments, and all patents, copyrights, or other intellectual property rights relating thereto, and agrees that the Executive has not acquired and shall not acquire any rights during the course of his employment with the Affiliated Group or thereafter with respect to any Developments.

- (c) <u>Company Goodwill</u>. The Executive recognizes and acknowledges that the Affiliated Group has and continues to develop goodwill of substantial value through efforts of employees, including the Executive. This goodwill includes, but is not limited to, the identity and skill sets of its employees, its relationships with employees and customers, intangible value attributable to its products created by Executive and others, and the Affiliated Group's brand and reputation within the industry. Executive shall take no action to damage the goodwill of the Affiliated Group (including disparaging the Affiliated Group or any of their respective directors officers, executives, employees, agents or other representatives) or use it for personal benefit or the benefit of competitors of the Affiliated Group.
- (d) Non-Recruitment of Affiliated Group Employees. The Executive acknowledges that employees are a significant part of the goodwill of the Affiliated Group, such as, without limitation, their relationships and contacts with customers and suppliers as well as the training and knowledge they receive from the Affiliated Group in the course of their employment. The Executive shall not, at any time during the Non-solicitation Restricted Period (as defined below), other than in the ordinary exercise of his duties while employed by the Affiliated Group, without the prior written consent of the Affiliated Group, directly or indirectly, solicit, recruit, or employ (whether as an employee, officer, agent, consultant or independent contractor) any person who is or was at any time during the previous 12 months, an employee, representative, officer or director of any member of the Affiliated Group. Further, during the Non-solicitation Restricted Period, the Executive shall not take any action that could reasonably be expected to have the effect of directly encouraging or inducing any person to cease their relationship with any member of the Affiliated Group for any reason. A general employment advertisement by an entity of which the Executive is a part will not constitute solicitation or recruitment. The "Non-solicitation Restricted Period" shall mean the period from the Date of Grant through the second anniversary of the Executive's termination of employment.
- (e) Non-Competition Solicitation of Business. The Executive recognizes and agrees that the Affiliated Group has provided Confidential Information to Executive and has an interest in protecting this information from disclosure. Executive further understands that the goodwill of the Affiliated Group is an interest worthy of protection. For the protection of these and other interests, during the Non-competition Restricted Period (as defined below), the Executive shall not, either directly or indirectly, compete with the business of the Affiliated Group by (i) becoming an officer, agent, employee, partner or director of any other corporation, partnership or other entity, or otherwise render services to or assist or hold an interest (except as a less than 3-percent shareholder of a publicly traded corporation or as a less than 5-percent shareholder of a corporation that is not publicly traded) in any Competitive Business (as defined below), or (ii) soliciting, servicing, or accepting the business of (A) any active customer of any member of the Affiliated Group, or (B) any person or entity who is or was at any time during the previous twelve months a customer of any member of the Affiliated Group, provided that such business is competitive with any significant business of any member of the Affiliated Group. "Competitive Business" shall mean any

person or entity (including any joint venture, partnership, firm, corporation, or limited liability company) that conducts a business that is competitive with any significant business of the Affiliated Group as of the date of termination (or any significant business that is being actively pursued as of the date of termination by the Affiliated Group). The Affiliated Group designs, manufactures, sells and licenses its products and technology worldwide. In addition, Competitive Businesses, as defined above, are not tied or limited to any specific geographic location. Accordingly, the scope of this Non-Competition provision is worldwide. The "Non-competition Restricted Period" shall mean the period from the Date of Grant through the second anniversary of the date of termination of the Executive's employment.

- (f) Assistance. The Executive agrees that during and after his employment by the Affiliated Group, upon request by the Company, the Executive will assist the Affiliated Group in the defense of any claims, or potential claims that may be made or threatened to be made against any member of the Affiliated Group in any action, suit or proceeding, whether civil, criminal, administrative, investigative or otherwise (a "Proceeding"), and will assist the Affiliated Group in the prosecution of any claims that may be made by any member of the Affiliated Group in any Proceeding, to the extent that such claims may relate to the Executive's employment or the period of the Executive's employment by the Affiliated Group. The Executive agrees, unless precluded by law, to promptly inform the Company if the Executive also agrees, unless precluded by law, to promptly inform the Company if the Executive is asked to assist in any investigation (whether governmental or otherwise) of any member of the Affiliated Group (or their actions), regardless of whether a lawsuit has then been filed against any member of the Affiliated Group with respect to such investigation. The Company agrees to reimburse the Executive for all of the Executive's reasonable out-of-pocket expenses associated with such assistance, including travel expenses and any attorneys' fees and shall pay a reasonable per diem fee for the Executive's service. In addition, the Executive agrees to provide such services as are reasonably requested by the Company to assist any successor to the Executive in the transition of duties and responsibilities to such successor. Any services or assistance contemplated in this Section (f) shall be at mutually agreed to and convenient times.
- (g) Remedies. The Executive acknowledges and agrees that the terms of this Exhibit A: (i) are reasonable in geographic and temporal scope, (ii) are necessary to protect legitimate proprietary and business interests of the Affiliated Group in, inter alia, near permanent customer relationships and confidential information. The Executive further acknowledges and agrees that the Executive's breach of the provisions of this Exhibit A will cause the Affiliated Group irreparable harm, which cannot be adequately compensated by money damages. The Executive consents and agrees that the forfeiture provisions contained in the Agreement are reasonable remedies in the event the Executive commits any such breach. If any of the provisions of this Exhibit A are determined to be wholly or partially unenforceable, the Executive hereby agrees that Exhibit A or any provision hereof may be reformed so that it is enforceable to the maximum extent permitted by law. If any of the provisions of this Exhibit A are determined to be wholly or partially unenforceable in any jurisdiction, such determination shall not be a bar to or in any way diminish the Affiliated Group's right to enforce any such covenant in any other jurisdiction.

FREESCALE SEMICONDUCTOR HOLDINGS 2011 OMNIBUS INCENTIVE PLAN FORM RESTRICTED SHARE UNIT AWARD AGREEMENT (Senior Management)

THIS AGREEMENT (the "**Agreement**"), is made effective as of the date indicated in the grant summary in the Freescale equity recordkeeping system (the "**Date of Grant**"), by and among Freescale Semiconductor, Ltd., a Bermuda exempted limited liability company (the "**Company**"), the recipient's employing subsidiary and the recipient of the grant (the "**Executive**"):

RECITALS:

WHEREAS, the Company has adopted the Freescale Semiconductor Holdings 2011 Omnibus Incentive Plan (the "**Plan**"), which Plan is incorporated herein by reference and made a part of this Agreement. Capitalized terms used but not otherwise defined herein shall have meanings ascribed to such terms in the Plan; and

WHEREAS, the Administrator has determined that it would be in the best interests of the Company and its shareholders to grant the Restricted Share Units provided for herein to the Executive pursuant to the Plan and the terms set forth herein.

NOW THEREFORE, in consideration of the mutual covenants hereinafter set forth, the parties agree as follows:

- 1. <u>Grant of Restricted Share Units</u>. The Company hereby grants to the Executive, on the terms and conditions hereinafter set forth, units evidencing a right to receive Common Shares as indicated in the grant summary in the Freescale equity recordkeeping system (each a "Share" and collectively, the "Shares") pursuant to the terms and conditions of this Agreement (the "Restricted Share Units" or "Restricted Share Unit Award").
 - 2. Restrictions and Vesting Period.
- (a) <u>Restrictions and Transferability</u>. The Restricted Share Unit Award may not be assigned, alienated, pledged, attached, sold or otherwise transferred or encumbered by the Executive otherwise than by will or by the laws of descent and distribution, and any such purported assignment, alienation, pledge, attachment, sale, transfer or encumbrance shall be void and unenforceable against the Company or any Affiliate; provided that the designation of a beneficiary shall not constitute an assignment, alienation, pledge, attachment, sale, transfer or encumbrance. No such permitted transfer of the Restricted Share Unit Award to heirs or legatees of the Executive shall be effective to bind the Company unless the Administrator shall have been furnished with written notice thereof and a copy of such evidence as the Administrator may deem necessary to establish the validity of the transfer and the acceptance by the transferees of the terms and conditions hereof.

(b) <u>Vesting Period</u>. Subject to the Executive's continued employment with the Company, or except as otherwise provided below, the Restricted Share Unit Award shall vest with respect to twenty-five percent (25%) of the Shares initially covered by the Restricted Share Unit Award on each of the first, second, third and fourth anniversaries of the Date of Grant. At any time, the portion of the Restricted Share Unit Award which has become vested as described above (or pursuant to Section 3 below) is hereinafter referred to as the "**Vested Portion**."

(c) Change in Control.

- (i) Notwithstanding any other provisions of the Plan or this Agreement to the contrary, in the event that the Executive's employment with the Company is terminated by the Company without Cause or by the Executive for Good Reason, in either case within twelve months following a Change in Control, all unvested Restricted Share Units shall become immediately vested. For purposes of this Agreement, "Cause" and "Good Reason" shall have the meanings set forth in the Executive's employment agreement, or if the Executive does not have an employment agreement in which these terms are defined, then Cause shall have the meaning set forth in the Plan and Good Reason shall have the meaning set forth below.
- (ii) If the Restricted Share Unit Award is not assumed or substituted in connection with a Change in Control, immediately upon the occurrence of the Change in Control, all unvested Restricted Share Units shall become immediately vested. For purposes of this Section 2(c)(ii), the Restricted Share Unit Award shall be considered assumed or substituted if, following the Change in Control, the Restricted Share Unit Award is of comparable value and remains subject to the same terms and conditions that were applicable to the Restricted Share Unit Award immediately prior to the Change in Control except that the Restricted Share Unit Award instead confers the right to receive common stock of the acquiring entity or in the case of an amalgamation, the amalgamated company or its parent.
- (iii) If the Executive does not have an employment agreement with the Company in which Good Reason is defined, "Good Reason" means, in the absence of the Executive's written consent, any of the following: (i) a material reduction by the Company in the Executive's base salary or target bonus unless the base salary or target bonus of all senior executives is reduced by a similar percentage or amount as part of company-wide cost reductions; (ii) a material reduction in the aggregate level of employee benefits made available to the Executive when compared to the benefits made available to the Executive at any time during the Executive's employment with the Company, unless the reduction is applicable to senior executives of the Company generally; (iii) a material diminution in the Executive's duties or responsibilities (other than as a result of the Executive's physical or mental incapacity which impairs his ability to materially perform his duties or responsibilities as confirmed by a doctor reasonably acceptable to the Executive or his representative and such diminution lasts only for so long as such doctor determines such incapacity impairs the Executive's ability to materially perform his duties or responsibilities). A lateral job change that does not materially diminish the Executive's duties or responsibilities and does not affect the Executive's reporting relationship will not constitute Good Reason; or (iv) the Company requiring the Executive's principal location of employment to be at any office or location more than 75 miles from the principal headquarters of the Company (other than any such change in location which is not materially adverse to the Executive, and other than to the extent agreed to or requested by the Executive) on the Date of Grant.

- (d) <u>Settlement of Restricted Share Units</u>. Shares shall be delivered (provided, that such delivery is otherwise in accordance with federal and state securities laws) with respect to the Vested Portion of the Restricted Share Unit Award as soon as practicable following the applicable vesting date, but in no event later than March 15 of the calendar year following the year of vesting.
- (e) No Shareholder Rights. The Executive shall have no rights of a shareholder of the Company with respect to the Restricted Share Units, including, but not limited to, the rights to vote and receive ordinary dividends, until the settlement date of the Restricted Share Units. In the event that the Administrator approves an adjustment to the Restricted Share Unit Award pursuant to Section 5 of the Plan, then in such event, any and all new, substituted or additional securities to which Executive is entitled by reason of the Restricted Share Unit Award shall be immediately subject to the restrictions and the Vesting Period set forth in Sections 2(a) and (b) above with the same force and effect as the Restricted Share Unit Award subject to such restrictions immediately before such event.

3. <u>Termination of Employment</u>.

- (a) <u>General</u>. If the Executive's employment is terminated for any reason, the Restricted Share Unit Award shall, to the extent not then vested (after giving effect to the provisions of Sections 2 and 3), terminate and be forfeited upon such termination of employment.
- (b) <u>For Cause</u>. The Restricted Share Unit Award (including any Vested Portion thereof) shall terminate and be forfeited upon the Company's notification to the Executive of the Executive's termination of employment by the Company for Cause.
- (c) <u>Death or Disability</u>. Upon the Executive's termination of employment due to death or due to Disability, the Restricted Share Unit Award shall become vested for an additional number of Shares equal to the number of Shares subject to the Restricted Share Unit Award (if any) that would have vested on the next anniversary of the Date of Grant if the Executive had remained employed until such date. Any portion of the Restricted Share Unit Award that is not vested after giving effect to the above provisions of this Section 3(c) shall terminate immediately and be forfeited effective as of the termination of the Executive's employment.
- (d) <u>Forfeiture</u>. Notwithstanding anything herein to the contrary, if the Executive breaches any Restrictive Covenants applicable to the Executive (including, without limitation, the Restrictive Covenants set forth in Exhibit A hereto) at any time during the two year period following the Executive's termination of employment for any reason then the Executive shall immediately repay to the Company the Fair Market Value of Shares acquired pursuant to the Restricted Share Unit Award on any vesting date within the three year period prior to termination. The Company reserves the right to reduce or waive any amounts payable to the Company pursuant to this provision, in its sole discretion.
- 4. <u>Certain Covenants</u>. The Executive hereby agrees and covenants to perform all of the obligations set forth in Exhibit A hereto (which is incorporated by reference hereby) and acknowledges that the Executive's obligations set forth in Exhibit A constitute a material inducement for the Company's grant of the Restricted Share Unit Award to the Executive.

- 5. No Right to Continued Employment. The granting of the Restricted Share Unit Award evidenced hereby and this Agreement shall impose no obligation on the Company or any Affiliate to continue the employment of the Executive and shall not lessen or affect the Company's or any Affiliate's right to terminate the employment of such Executive. The granting of the Restricted Share Unit Award does not form part of and should in no way be construed as a term or condition of employment. At all times, the Restricted Share Unit Award granted hereunder is discretionary and does not imply that additional Restricted Share Unit Awards will be awarded in the future.
- 6. <u>Restricted Share Unit Award Not Wages</u>. The value of any Restricted Share Unit Award granted to Executive does not constitute and will not be included as wages for the purposes of calculating any benefit or bonus provided by the Company or the Executive's employing subsidiary.
- 7. Withholding. The Executive will be required to pay to the Company or any Affiliate and the Company shall have the right and is hereby authorized to withhold from any payment due or transfer made under the Restricted Share Unit Award or under the Plan or from any compensation or other amount owing to the Executive the amount (in cash, Shares, other securities or other property) of any applicable withholding taxes in respect of the Restricted Share Unit Award or any payment or transfer under or with respect to the Restricted Share Unit Award or the Plan and to take such other action as may be necessary in the opinion of the Administrator to satisfy all obligations for the payment of such withholding taxes.
- 8. <u>Securities Laws</u>. The issuance of any Shares hereunder shall be subject to the Executive making or entering into such written representations, warranties and agreements as the Administrator may reasonably request in order to comply with applicable securities laws and government regulations.
- 9. No Public Offering. The Restricted Share Units awarded under the Plan and this Agreement will not be publicly issued, placed, distributed or offered. The issuance of any Restricted Share Units hereunder does not constitute a public offering of securities.
- 10. <u>Consent to Transfer of Data</u>. By accepting the Restricted Share Unit Award, Executive consents to the transfer of personal data (including but not limited to **the** employee's name, address, birth date and hire date) and to the processing of this personal data by the Company and the provider of the Freescale equity recordkeeping system.
- 11. <u>Notices</u>. Any notice necessary under this Agreement shall be addressed to the Company in care of its Secretary at the principal executive office of the Company and to the Executive at the address appearing in the personnel records of the Company for the Executive or to either party at such other address as either party hereto may hereafter designate in writing to the other. Any such notice shall be deemed effective upon receipt thereof by the addressee.

- 12. <u>Governing Law</u>. This Agreement and all claims arising out of or based upon this Agreement or relating to the subject matter hereof shall be governed by and construed in accordance with the domestic substantive laws of the State of Delaware without giving effect to any choice or conflict of laws provision or rule that would cause the application of the domestic substantive laws of any other jurisdiction.
- 13. <u>Consent to Jurisdiction</u>. All actions arising out of or relating to this Agreement shall be heard and determined exclusively in any New York state or federal court sitting in the Borough of Manhattan in The City of New York. The parties hereto hereby (a) submit to the exclusive jurisdiction of any state or federal court sitting in the Borough of Manhattan of The City of New York for the purpose of any action arising out of or relating to this Agreement brought by any party hereto, and (b) irrevocably waive, and agree not to assert by way of motion, defense, or otherwise, in any such action, any claim that it is not subject personally to the jurisdiction of the above-named courts, that its property is exempt or immune of from attachment or execution, that the action is brought in an inconvenient forum, that the venue of the action is improper, or that this Agreement or the transactions contemplated hereby may not be enforced in or by any of the above-named courts.
- 14. Restricted Share Unit Award <u>Subject to Plan</u>. By entering into this Agreement, the Executive agrees and acknowledges that the Executive has received and read a copy of the Plan. The Restricted Share Unit Award is subject to the Plan, as may be amended from time to time, and the terms and provisions of the Plan are hereby incorporated herein by reference.
- 15. <u>Acceptance</u>. This Agreement must be accepted by electronic signature of the Executive in the Freescale equity recordkeeping system or the Executive will have no right to the Restricted Share Unit Award provided for in this Agreement. By accepting this Agreement the Executive consents to the electronic delivery through the Freescale equity recordkeeping system of all documents related to this Restricted Share Unit Award.
- 16. <u>Clawback</u>. The Restricted Share Unit Award shall be subject to the Company's clawback policy, as it may be amended from time to time. The Company will amend its clawback policy, as needed, to the extent that the Securities and Exchange Commission adopts the final implementing rules regarding compensation clawbacks mandated by the Dodd-Frank Wall Street Reform and Consumer Protection Act of 2010.

Exhibit A – Restrictive Covenants

(a) Confidential Information. The Executive recognizes and agrees that the Affiliated Group (defined below) has provided Confidential Information to the Executive and has an interest in protecting this information from disclosure. The Executive shall hold in a fiduciary capacity for the benefit of the Company and its Affiliates (collectively, the "Affiliated Group"), all secret or confidential information, knowledge or data relating to the Affiliated Group and its businesses (including, without limitation, any proprietary and not publicly available information concerning any processes, methods, trade secrets, research or secret data, costs, names of users or purchasers of their respective products or services, business methods, operating procedures or programs or methods of promotion and sale) that the Executive obtains during the Executive's employment that is not public knowledge (other than as a result of the Executive's violation of this Section (a)) ("Confidential Information"). The Executive shall not communicate, divulge or disseminate Confidential Information at any time during or after the Executive's employment, except with the prior written consent of the Company, or as otherwise required by law or legal process or as such disclosure or use may be required in the course of the Executive performing his duties and responsibilities with the Affiliated Group. Notwithstanding the foregoing provisions, if the Executive is required to disclose any such confidential or proprietary information pursuant to applicable law or a subpoena or court order, the Executive shall promptly notify the Company in writing of any such requirement prior to disclosure so that the Company or the appropriate member of the Affiliated Group may seek an appropriate protective order or other appropriate remedy or waive compliance with the provisions hereof. The Executive shall reasonably cooperate with the Company or the appropriate member of the Affiliated Group to obtain such a protective order or other remedy. If such order or other remedy is not obtained prior to the time the Executive is required to make the disclosure, or the Company waives compliance with the provisions hereof, the Executive shall disclose only that portion of the confidential or proprietary information which he is advised by counsel in writing (either his or the Company's) that he is legally required to so disclose. Upon his termination of employment for any reason, the Executive shall promptly return to the Company all records, files, memoranda, correspondence, notebooks, notes, reports, customer lists, drawings, plans, documents, and other documents and the like relating to the business of the Affiliated Group or containing any trade secrets relating to the Affiliated Group or that the Executive uses, prepares or comes into contact with during the course of the Executive's employment with the Affiliated Group, and all keys, credit cards and passes, and such materials shall remain the sole property of the Affiliated Group. The Executive agrees to execute any standard-form confidentiality agreements with the Company that the Company in the future generally enters into with similarly situated employees.

(b) <u>Work Product and Inventions</u>. The Affiliated Group and/or its nominees or assigns shall own all right, title and interest in and to any and all inventions, ideas, trade secrets, technology, devices, discoveries, improvements, processes, developments, designs, know how, show-how, data, computer programs, algorithms, formulae, works of authorship, works modifications, trademarks, trade names, documentation, techniques, designs, methods, trade secrets, technical specifications, technical data, concepts, expressions, patents, patent rights, copyrights, moral rights, and all other intellectual property rights or other developments whatsoever (collectively, "**Developments**"), whether or not patentable, reduced to practice or registerable under patent, copyright, trademark or other intellectual property law anywhere in the world, made, authored, discovered, reduced to practice, conceived, created, developed or otherwise obtained by the Executive (alone or jointly with others) during the Executive's employment with the Affiliated Group, and arising from or relating to such employment or the business of the Affiliated Group

(whether during business hours or otherwise, and whether on the premises of using the facilities or materials of the Affiliated Group or otherwise). The Executive shall promptly and fully disclose to the Affiliated Group and to no one else all Developments, and hereby assigns to the Affiliated Group without further compensation all right, title and interest the Executive has or may have in any Developments, and all patents, copyrights, or other intellectual property rights relating thereto, and agrees that the Executive has not acquired and shall not acquire any rights during the course of his employment with the Affiliated Group or thereafter with respect to any Developments.

- (c) <u>Company Goodwill</u>. The Executive recognizes and acknowledges that the Affiliated Group has and continues to develop goodwill of substantial value through efforts of employees, including the Executive. This goodwill includes, but is not limited to, the identity and skill sets of its employees, its relationships with employees and customers, intangible value attributable to its products created by Executive and others, and the Affiliated Group's brand and reputation within the industry. Executive shall take no action to damage the goodwill of the Affiliated Group (including disparaging the Affiliated Group or any of their respective directors, officers, executives, employees, agents or other representatives) or use it for personal benefit or the benefit of competitors of the Affiliated Group.
- (d) Non-Recruitment of Affiliated Group Employees. The Executive acknowledges that employees are a significant part of the goodwill of the Affiliated Group, such as, without limitation, their relationships and contacts with customers and suppliers as well as the training and knowledge they receive from the Affiliated Group in the course of their employment. The Executive shall not, at any time during the Non-solicitation Restricted Period (as defined below), other than in the ordinary exercise of his duties while employed by the Affiliated Group, without the prior written consent of the Affiliated Group, directly or indirectly, solicit, recruit, or employ (whether as an employee, officer, agent, consultant or independent contractor) any person who is or was at any time during the previous 12 months, an employee, representative, officer or director of any member of the Affiliated Group. Further, during the Non-solicitation Restricted Period, the Executive shall not take any action that could reasonably be expected to have the effect of directly encouraging or inducing any person to cease their relationship with any member of the Affiliated Group for any reason. A general employment advertisement by an entity of which the Executive is a part will not constitute solicitation or recruitment. The "Non-solicitation Restricted Period" shall mean the period from the Date of Grant through the second anniversary of the Executive's termination of employment.
- (e) Non-Competition Solicitation of Business. The Executive recognizes and agrees that the Affiliated Group has provided Confidential Information to Executive and has an interest in protecting this information from disclosure. Executive further understands that the goodwill of the Affiliated Group is an interest worthy of protection. For the protection of these and other interests, during the Non-competition Restricted Period (as defined below), the Executive shall not, either directly or indirectly, compete with the business of the Affiliated Group by (i) becoming an officer, agent, employee, partner or director of any other corporation, partnership or other entity, or otherwise render services to or assist or hold an interest (except as a less than 3-percent shareholder of a publicly traded corporation or as a less than 5-percent shareholder of a corporation that is not publicly traded) in any Competitive Business (as defined below), or (ii) soliciting, servicing, or accepting the business of (A) any active customer of any member of the Affiliated Group, or (B) any person or entity who is or was at any time during the previous twelve months a customer of any member of the Affiliated Group, provided that such business is competitive with any significant business of any member of the Affiliated Group. "Competitive Business" shall mean any

person or entity (including any joint venture, partnership, firm, corporation, or limited liability company) that conducts a business that is competitive with any significant business of the Affiliated Group as of the date of termination (or any significant business that is being actively pursued as of the date of termination by the Affiliated Group). The Affiliated Group designs, manufactures, sells and licenses its products and technology worldwide. In addition, Competitive Businesses, as defined above, are not tied or limited to any specific geographic location. Accordingly, the scope of this Non-Competition provision is worldwide. The "Non-competition Restricted Period" shall mean the period from the Date of Grant through the second anniversary of the date of termination of the Executive's employment.

- (f) Assistance. The Executive agrees that during and after his employment by the Affiliated Group, upon request by the Company, the Executive will assist the Affiliated Group in the defense of any claims, or potential claims that may be made or threatened to be made against any member of the Affiliated Group in any action, suit or proceeding, whether civil, criminal, administrative, investigative or otherwise (a "Proceeding"), and will assist the Affiliated Group in the prosecution of any claims that may be made by any member of the Affiliated Group in any Proceeding, to the extent that such claims may relate to the Executive's employment or the period of the Executive's employment by the Affiliated Group. The Executive agrees, unless precluded by law, to promptly inform the Company if the Executive also agrees, unless precluded by law, to promptly inform the Company if the Executive is asked to assist in any investigation (whether governmental or otherwise) of any member of the Affiliated Group (or their actions), regardless of whether a lawsuit has then been filed against any member of the Affiliated Group with respect to such investigation. The Company agrees to reimburse the Executive for all of the Executive's reasonable out-of-pocket expenses associated with such assistance, including travel expenses and any attorneys' fees and shall pay a reasonable per diem fee for the Executive's service. In addition, the Executive agrees to provide such services as are reasonably requested by the Company to assist any successor to the Executive in the transition of duties and responsibilities to such successor. Any services or assistance contemplated in this Section (f) shall be at mutually agreed to and convenient times.
- (g) Remedies. The Executive acknowledges and agrees that the terms of this Exhibit A: (i) are reasonable in geographic and temporal scope, (ii) are necessary to protect legitimate proprietary and business interests of the Affiliated Group in, inter alia, near permanent customer relationships and confidential information. The Executive further acknowledges and agrees that the Executive's breach of the provisions of this Exhibit A will cause the Affiliated Group irreparable harm, which cannot be adequately compensated by money damages. The Executive consents and agrees that the forfeiture provisions contained in the Agreement are reasonable remedies in the event the Executive commits any such breach. If any of the provisions of this Exhibit A are determined to be wholly or partially unenforceable, the Executive hereby agrees that Exhibit A or any provision hereof may be reformed so that it is enforceable to the maximum extent permitted by law. If any of the provisions of this Exhibit A are determined to be wholly or partially unenforceable in any jurisdiction, such determination shall not be a bar to or in any way diminish the Affiliated Group's right to enforce any such covenant in any other jurisdiction.